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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	392
Number of Logic Elements/Cells	6272
Total RAM Bits	276480
Number of I/O	91
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-EQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce6e22a7n



Cyclone IV E industrial devices I7 are offered with extended operating temperature range.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone IV devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Table 1–1 lists the absolute maximum ratings for Cyclone IV devices.



Conditions beyond those listed in Table 1–1 cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time have adverse effects on the device.

Table 1–1. Absolute Maximum Ratings for Cyclone IV Devices ⁽¹⁾

Symbol	Parameter	Min	Max	Unit
V_{CCINT}	Core voltage, PCI Express® (PCIe®) hard IP block, and transceiver physical coding sublayer (PCS) power supply	–0.5	1.8	V
V_{CCA}	Phase-locked loop (PLL) analog power supply	–0.5	3.75	V
V_{CCD_PLL}	PLL digital power supply	–0.5	1.8	V
V_{CCIO}	I/O banks power supply	–0.5	3.75	V
V_{CC_CLKIN}	Differential clock input pins power supply	–0.5	4.5	V
V_{CCH_GXB}	Transceiver output buffer power supply	–0.5	3.75	V
V_{CCA_GXB}	Transceiver physical medium attachment (PMA) and auxiliary power supply	–0.5	3.75	V
V_{CCL_GXB}	Transceiver PMA and auxiliary power supply	–0.5	1.8	V
V_I	DC input voltage	–0.5	4.2	V
I_{OUT}	DC output current, per pin	–25	40	mA
T_{STG}	Storage temperature	–65	150	°C
T_J	Operating junction temperature	–40	125	°C

Note to Table 1–1:

(1) Supply voltage specifications apply to voltage readings taken at the device pins with respect to ground, not at the power supply.

Maximum Allowed Overshoot or Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to –2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns. Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device.

Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices ^{(1), (2)} (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Diode}	Magnitude of DC current across PCI-clamp diode when enable	—	—	—	10	mA

Notes to Table 1–3:

- (1) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades.
- (2) V_{CCIO} for all I/O banks must be powered up during device operation. All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- (3) V_{CC} must rise monotonically.
- (4) V_{CCIO} powers all input buffers.
- (5) The POR time for Standard POR ranges between 50 and 200 ms. Each individual power supply must reach the recommended operating range within 50 ms.
- (6) The POR time for Fast POR ranges between 3 and 9 ms. Each individual power supply must reach the recommended operating range within 3 ms.

Table 1–4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 1 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCINT} ⁽³⁾	Core voltage, PCIe hard IP block, and transceiver PCS power supply	—	1.16	1.2	1.24	V
V_{CCA} ^{(1), (3)}	PLL analog power supply	—	2.375	2.5	2.625	V
V_{CCD_PLL} ⁽²⁾	PLL digital power supply	—	1.16	1.2	1.24	V
V_{CCIO} ^{(3), (4)}	I/O banks power supply for 3.3-V operation	—	3.135	3.3	3.465	V
	I/O banks power supply for 3.0-V operation	—	2.85	3	3.15	V
	I/O banks power supply for 2.5-V operation	—	2.375	2.5	2.625	V
	I/O banks power supply for 1.8-V operation	—	1.71	1.8	1.89	V
	I/O banks power supply for 1.5-V operation	—	1.425	1.5	1.575	V
	I/O banks power supply for 1.2-V operation	—	1.14	1.2	1.26	V
V_{CC_CLKIN} ^{(3), (5), (6)}	Differential clock input pins power supply for 3.3-V operation	—	3.135	3.3	3.465	V
	Differential clock input pins power supply for 3.0-V operation	—	2.85	3	3.15	V
	Differential clock input pins power supply for 2.5-V operation	—	2.375	2.5	2.625	V
	Differential clock input pins power supply for 1.8-V operation	—	1.71	1.8	1.89	V
	Differential clock input pins power supply for 1.5-V operation	—	1.425	1.5	1.575	V
	Differential clock input pins power supply for 1.2-V operation	—	1.14	1.2	1.26	V
V_{CCH_GXB}	Transceiver output buffer power supply	—	2.375	2.5	2.625	V

Table 1-4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA_GXB}	Transceiver PMA and auxiliary power supply	—	2.375	2.5	2.625	V
V_{CCL_GXB}	Transceiver PMA and auxiliary power supply	—	1.16	1.2	1.24	V
V_I	DC input voltage	—	-0.5	—	3.6	V
V_O	DC output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	-40	—	100	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR) ⁽⁷⁾	50 μ s	—	50 ms	—
		Fast POR ⁽⁸⁾	50 μ s	—	3 ms	—
I_{Diode}	Magnitude of DC current across PCI-clamp diode when enabled	—	—	—	10	mA

Notes to Table 1-4:

- (1) All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- (2) You must connect V_{CCD_PLL} to V_{CCINT} through a decoupling capacitor and ferrite bead.
- (3) Power supplies must rise monotonically.
- (4) V_{CCIO} for all I/O banks must be powered up during device operation. Configurations pins are powered up by V_{CCIO} of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support V_{CCIO} of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the V_{CCIO} level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.
- (5) You must set V_{CC_CLKIN} to 2.5 V if you use $CLKIN$ as a high-speed serial interface (HSSI) $refclk$ or as a $DIFFCLK$ input.
- (6) The $CLKIN$ pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.
- (7) The POR time for Standard POR ranges between 50 and 200 ms. V_{CCINT} , V_{CCA} , and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.
- (8) The POR time for Fast POR ranges between 3 and 9 ms. V_{CCINT} , V_{CCA} , and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1-5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

Table 1-5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os

Symbol	Parameter	Passing Voltage	Unit
V_{ESDHBM}	ESD voltage using the HBM (GPIOs) ⁽¹⁾	± 2000	V
	ESD using the HBM (HSSI I/Os) ⁽²⁾	± 1000	V
V_{ESDCDM}	ESD using the CDM (GPIOs)	± 500	V
	ESD using the CDM (HSSI I/Os) ⁽²⁾	± 250	V

Notes to Table 1-5:

- (1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is ± 1000 V.
- (2) This value is applicable only to Cyclone IV GX devices.

DC Characteristics

This section lists the I/O leakage current, pin capacitance, on-chip termination (OCT) tolerance, and bus hold specifications for Cyclone IV devices.

Supply Current

The device supply current requirement is the minimum current drawn from the power supply pins that can be used as a reference for power size planning. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary greatly with the resources used. Table 1-6 lists the I/O pin leakage current for Cyclone IV devices.

Table 1-6. I/O Pin Leakage Current for Cyclone IV Devices ^{(1), (2)}

Symbol	Parameter	Conditions	Device	Min	Typ	Max	Unit
I_I	Input pin leakage current	$V_I = 0\text{ V to }V_{CCIO\text{MAX}}$	—	-10	—	10	μA
I_{OZ}	Tristated I/O pin leakage current	$V_O = 0\text{ V to }V_{CCIO\text{MAX}}$	—	-10	—	10	μA

Notes to Table 1-6:

- (1) This value is specified for normal device operation. The value varies during device power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).
- (2) The 10 μA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

Bus Hold

The bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1-7 lists bus hold specifications for Cyclone IV devices.

Table 1-7. Bus Hold Parameter for Cyclone IV Devices (Part 1 of 2) ⁽¹⁾

Parameter	Condition	V _{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus hold low, sustaining current	V _{IN} > V _{IL} (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	μA
Bus hold high, sustaining current	V _{IN} < V _{IL} (minimum)	−8	—	−12	—	−30	—	−50	—	−70	—	−70	—	μA
Bus hold low, overdrive current	0 V < V _{IN} < V _{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	μA
Bus hold high, overdrive current	0 V < V _{IN} < V _{CCIO}	—	−125	—	−175	—	−200	—	−300	—	−500	—	−500	μA

Schmitt Trigger Input

Cyclone IV devices support Schmitt trigger input on the TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rate. Table 1–14 lists the hysteresis specifications across the supported V_{CCIO} range for Schmitt trigger inputs in Cyclone IV devices.

Table 1–14. Hysteresis Specifications for Schmitt Trigger Input in Cyclone IV Devices

Symbol	Parameter	Conditions (V)	Minimum	Unit
$V_{SCHMITT}$	Hysteresis for Schmitt trigger input	$V_{CCIO} = 3.3$	200	mV
		$V_{CCIO} = 2.5$	200	mV
		$V_{CCIO} = 1.8$	140	mV
		$V_{CCIO} = 1.5$	110	mV

I/O Standard Specifications

The following tables list input voltage sensitivities (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}), for various I/O standards supported by Cyclone IV devices. Table 1–15 through Table 1–20 provide the I/O standard specifications for Cyclone IV devices.

Table 1–15. Single-Ended I/O Standard Specifications for Cyclone IV Devices ^{(1), (2)}

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA) (4)	I_{OH} (mA) (4)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTTL ⁽³⁾	3.135	3.3	3.465	—	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS ⁽³⁾	3.135	3.3	3.465	—	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	2	–2
3.0-V LVTTTL ⁽³⁾	2.85	3.0	3.15	–0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.45	2.4	4	–4
3.0-V LVCMOS ⁽³⁾	2.85	3.0	3.15	–0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.2	$V_{CCIO} - 0.2$	0.1	–0.1
2.5 V ⁽³⁾	2.375	2.5	2.625	–0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.4	2.0	1	–1
1.8 V	1.71	1.8	1.89	–0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	2.25	0.45	$V_{CCIO} - 0.45$	2	–2
1.5 V	1.425	1.5	1.575	–0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	–2
1.2 V	1.14	1.2	1.26	–0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	–2
3.0-V PCI	2.85	3.0	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	–0.5
3.0-V PCI-X	2.85	3.0	3.15	—	$0.35 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	–0.5

Notes to Table 1–15:

- (1) For voltage-referenced receiver input waveform and explanation of terms used in Table 1–15, refer to “Glossary” on page 1–37.
- (2) AC load $CL = 10$ pF
- (3) For more information about interfacing Cyclone IV devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O standards, refer to *AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O Systems*.
- (4) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the **3.3-V LVTTTL** specification (4 mA), set the current strength settings to 4 mA or higher. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the handbook.

For more information about receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *I/O Features in Cyclone IV Devices* chapter.

Table 1–18. Differential SSTL I/O Standard Specifications for Cyclone IV Devices ⁽¹⁾

I/O Standard	V_{CCIO} (V)			$V_{Swing(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{Swing(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.7	V_{CCIO}	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$
SSTL-18 Class I, II	1.7	1.8	1.90	0.25	V_{CCIO}	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	V_{CCIO}	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$

Note to Table 1–18:(1) Differential SSTL requires a V_{REF} input.**Table 1–19. Differential HSTL I/O Standard Specifications for Cyclone IV Devices ⁽¹⁾**

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	$0.48 \times V_{CCIO}$	—	$0.52 \times V_{CCIO}$	$0.48 \times V_{CCIO}$	—	$0.52 \times V_{CCIO}$	0.3	$0.48 \times V_{CCIO}$

Note to Table 1–19:(1) Differential HSTL requires a V_{REF} input.**Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices ⁽¹⁾ (Part 1 of 2)**

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) ⁽²⁾			V_{OD} (mV) ⁽³⁾			V_{OS} (V) ⁽³⁾		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (Row I/Os) ⁽⁶⁾	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq 500$ Mbps	1.80	—	—	—	—	—	—
						0.55	$500 \text{ Mbps} \leq D_{MAX} \leq 700$ Mbps	1.80						
						1.05	$D_{MAX} > 700$ Mbps	1.55						
LVPECL (Column I/Os) ⁽⁶⁾	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq 500$ Mbps	1.80	—	—	—	—	—	—
						0.55	$500 \text{ Mbps} \leq D_{MAX} \leq 700$ Mbps	1.80						
						1.05	$D_{MAX} > 700$ Mbps	1.55						
LVDS (Row I/Os)	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq 500$ Mbps	1.80	247	—	600	1.125	1.25	1.375
						0.55	$500 \text{ Mbps} \leq D_{MAX} \leq 700$ Mbps	1.80						
						1.05	$D_{MAX} > 700$ Mbps	1.55						

Power Consumption

Use the following methods to estimate power for a design:

- the Excel-based EPE
- the Quartus® II PowerPlay power analyzer feature

The interactive Excel-based EPE is used prior to designing the device to get a magnitude estimate of the device power. The Quartus II PowerPlay power analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay power analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, combined with detailed circuit models, can yield very accurate power estimates.



For more information about power estimation tools, refer to the *Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of Cyclone IV core and periphery blocks for commercial grade devices.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The upper-right hand corner of these tables show the designation as “Preliminary”.
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

Table 1-21 lists the Cyclone IV GX transceiver specifications.

Table 1-21. Transceiver Specification for Cyclone IV GX Devices (Part 1 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	1.2 V PCML, 1.5 V PCML, 3.3 V PCML, Differential LVPECL, LVDS, HCSL										
Input frequency from REFCLK input pins	—	50	—	156.25	50	—	156.25	50	—	156.25	MHz
Spread-spectrum modulating clock frequency	Physical interface for PCI Express (PIPE) mode	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PIPE mode	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
Peak-to-peak differential input voltage	—	0.1	—	1.6	0.1	—	1.6	0.1	—	1.6	V
V _{ICM} (AC coupled)	—	1100 ± 5%			1100 ± 5%			1100 ± 5%			mV
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise ⁽¹⁾	Frequency offset = 1 MHz – 8 MHz	—	—	–123	—	—	–123	—	—	–123	dBc/Hz
Transmitter REFCLK Total Jitter ⁽¹⁾		—	—	42.3	—	—	42.3	—	—	42.3	ps
R _{ref}	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clock											
cal_blk_clk clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5/37.5 ⁽²⁾	—	50	2.5/37.5 ⁽²⁾	—	50	2.5/37.5 ⁽²⁾	—	50	MHz
Delta time between reconfig_clk	—	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum power-down pulse width	—	—	1	—	—	1	—	—	1	—	μs

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 4 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PLD-Transceiver Interface											
Interface speed (F324 and smaller package)	—	25	—	125	25	—	125	25	—	125	MHz
Interface speed (F484 and larger package)	—	25	—	156.25	25	—	156.25	25	—	156.25	MHz
Digital reset pulse width	—	Minimum is 2 parallel clock cycles									

Notes to Table 1–21:

- (1) This specification is valid for transmitter output jitter specification with a maximum total jitter value of 112 ps, typically for 3.125 Gbps SRIO and XAUI protocols.
- (2) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter Only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver Only** or **Receiver and Transmitter** mode.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The rate matcher supports only up to ± 300 parts per million (ppm).
- (5) Supported for the F169 and F324 device packages only.
- (6) Supported for the F484, F672, and F896 device packages only. Pending device characterization.
- (7) To support CDR ppm tolerance greater than ± 300 ppm, implement ppm detector in user logic and configure CDR to Manual Lock Mode.
- (8) Asynchronous spread-spectrum clocking is not supported.
- (9) For the EP4CGX30 (F484 package only), EP4CGX50, and EP4CGX75 devices, the CDR ppl tolerance is ± 200 ppm.
- (10) Time taken until `p11_locked` goes high after `p11_powerdown` deasserts.
- (11) Time that the CDR must be kept in lock-to-reference mode after `rx_analogreset` deasserts and before `rx_locktodata` is asserted in manual mode.
- (12) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode (Figure 1–2), or after `rx_freqlocked` signal goes high in automatic mode (Figure 1–3).
- (13) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode.
- (14) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode.
- (15) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Figure 1-2 shows the lock time parameters in manual mode.


 LTD = lock-to-data. LTR = lock-to-reference.

Figure 1-2. Lock Time Parameters for Manual Mode

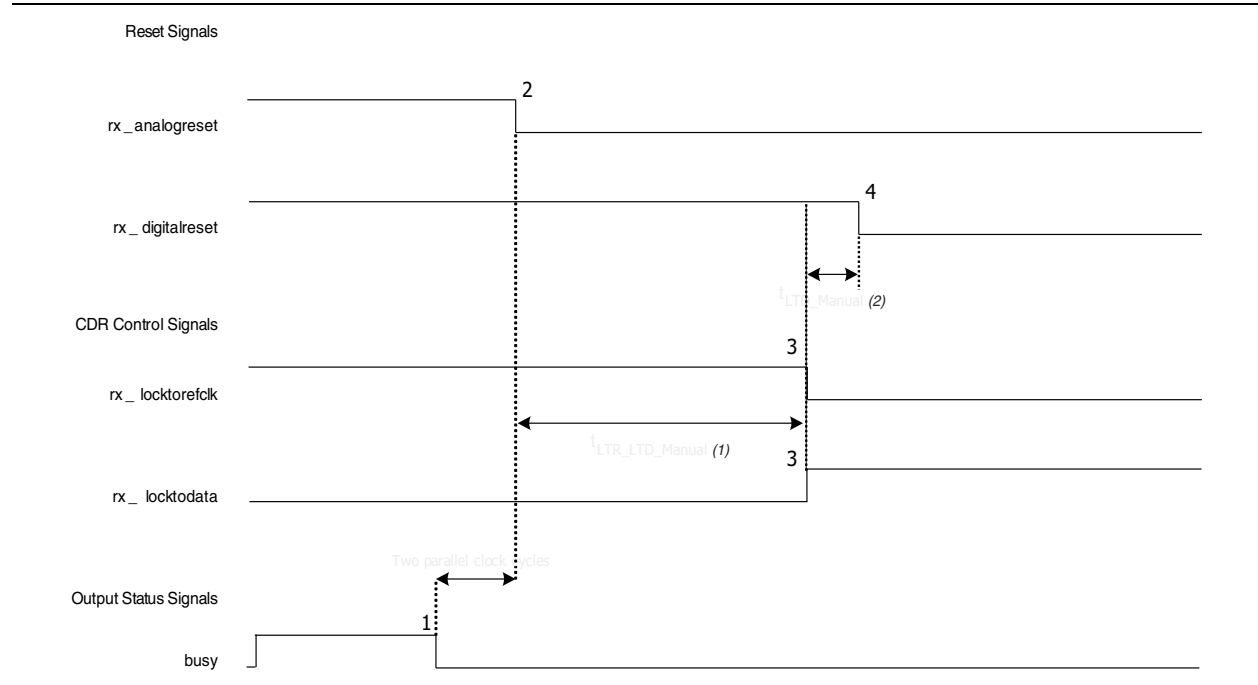


Figure 1-3 shows the lock time parameters in automatic mode.

Figure 1-3. Lock Time Parameters for Automatic Mode

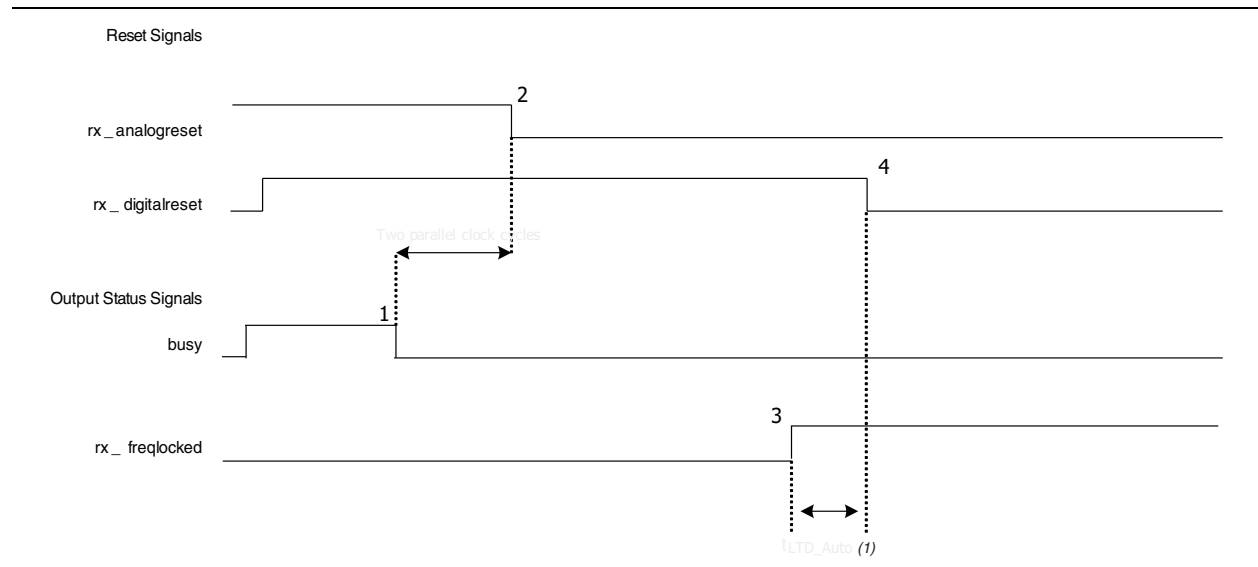


Table 1–23 lists the Cyclone IV GX transceiver block AC specifications.

Table 1–23. Transceiver Block AC Specification for Cyclone IV GX Devices ^{(1), (2)}

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PCIe Transmit Jitter Generation ⁽³⁾											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	—	—	0.25	—	—	0.25	—	—	0.25	UI
PCIe Receiver Jitter Tolerance ⁽³⁾											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	> 0.6			> 0.6			> 0.6			UI
GIGE Transmit Jitter Generation ⁽⁴⁾											
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance ⁽⁴⁾											
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI

Notes to Table 1–23:

- (1) Dedicated `refclk` pins were used to drive the input reference clocks.
- (2) The jitter numbers specified are valid for the stated conditions only.
- (3) The jitter numbers for PIPE are compliant to the PCIe Base Specification 2.0.
- (4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.

Core Performance Specifications

The following sections describe the clock tree specifications, PLLs, embedded multiplier, memory block, and configuration specifications for Cyclone IV Devices.

Clock Tree Specifications

Table 1–24 lists the clock tree specifications for Cyclone IV devices.

Table 1–24. Clock Tree Performance for Cyclone IV Devices (Part 1 of 2)

Device	Performance								Unit
	C6	C7	C8	C8L ⁽¹⁾	C9L ⁽¹⁾	I7	I8L ⁽¹⁾	A7	
EP4CE6	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE10	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE15	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE22	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE30	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE40	500	437.5	402	362	265	437.5	362	402	MHz

Table 1–25. PLL Specifications for Cyclone IV Devices ^{(1), (2)} (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or \overline{areset} is deasserted)	—	—	1	ms
$t_{OUTJITTER_PERIOD_DEDCLK}^{(6)}$	Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER_CCJ_DEDCLK}^{(6)}$	Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER_PERIOD_IO}^{(6)}$	Regular I/O period jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER_CCJ_IO}^{(6)}$	Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	± 50	ps
t_{ARESET}	Minimum pulse width on \overline{areset} signal.	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	3.5 ⁽⁷⁾	—	SCANCLK cycles
$f_{SCANCLK}$	$scanclk$ frequency	—	—	100	MHz
$t_{CASC_OUTJITTER_PERIOD_DEDCLK}^{(8), (9)}$	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	425	ps
	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz)	—	—	42.5	mUI

Notes to Table 1–25:

- (1) This table is applicable for general purpose PLLs and multipurpose PLLs.
- (2) You must connect V_{CCD_PLL} to V_{CCINT} through the decoupling capacitor and ferrite bead.
- (3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (4) The V_{CO} frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the V_{CO} post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.
- (6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.
- (7) With 100-MHz $scanclk$ frequency.
- (8) The cascaded PLLs specification is applicable only with the following conditions:
 - Upstream PLL— $0.59 \text{ MHz} \leq \text{Upstream PLL bandwidth} < 1 \text{ MHz}$
 - Downstream PLL—Downstream PLL bandwidth $> 2 \text{ MHz}$
- (9) PLL cascading is not supported for transceiver applications.

I/O Timing

Use the following methods to determine I/O timing:

- the Excel-based I/O Timing
- the Quartus II timing analyzer

The Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get a timing budget estimation as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.



The Excel-based I/O Timing spreadsheet is downloadable from Cyclone IV Devices Literature website.

Glossary

Table 1-46 lists the glossary for this chapter.

Table 1-46. Glossary (Part 1 of 5)

Letter	Term	Definitions
A	—	—
B	—	—
C	—	—
D	—	—
E	—	—
F	f_{HSCLK}	High-speed I/O block: High-speed receiver/transmitter input and output clock frequency.
G	GCLK	Input pin directly to Global Clock network.
	GCLK PLL	Input pin to Global Clock network through the PLL.
H	HSIODR	High-speed I/O block: Maximum/minimum LVDS data transfer rate ($\text{HSIODR} = 1/\text{TUI}$).
I	Input Waveforms for the SSTL Differential I/O Standard	

Table 1-46. Glossary (Part 2 of 5)

Letter	Term	Definitions
J	JTAG Waveform	<p>The diagram illustrates the JTAG waveform with the following timing parameters:</p> <ul style="list-style-type: none"> t_{JCP}: Time from TCK rising edge to TDI setup. t_{JCH}: Time from TCK rising edge to TDI hold. t_{JCL}: Time from TCK falling edge to TDI setup. t_{JCH}: Time from TCK falling edge to TDI hold. t_{JPSU_TDI}: Setup time for TDI before TCK rising edge. t_{JPSU_TMS}: Setup time for TMS before TCK rising edge. t_{JPH}: Hold time for TMS after TCK rising edge. t_{JPZX}: Time from TCK rising edge to TDO setup. t_{JPCO}: Time from TCK rising edge to TDO output. t_{JPXZ}: Time from TCK rising edge to TDO hold. t_{JSSU}: Setup time for Signal to be Captured before TCK rising edge. t_{JSH}: Hold time for Signal to be Captured after TCK rising edge. t_{JSZX}: Time from TCK rising edge to Signal to be Driven setup. t_{JSCO}: Time from TCK rising edge to Signal to be Driven output. t_{JSXZ}: Time from TCK rising edge to Signal to be Driven hold.
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	PLL Block	<p>The following highlights the PLL specification parameters:</p> <p>The diagram shows the internal structure of the PLL block. It includes a Core Clock input, a Switchover block, a Divider (N), a Phase-Locked Loop (PLL) block containing a Phase-Frequency Detector (PFD), Charge Pump (CP), Loop Filter (LF), and Voltage-Controlled Oscillator (VCO). The output of the VCO is f_{VCO}, which is divided by a Counter (C0..C4) to produce f_{OUT_EXT} and f_{OUT}. A Phase tap is also shown. A Key indicates that components in grey boxes are Reconfigurable in User Mode.</p>
Q	—	—

Table 1-46. Glossary (Part 3 of 5)

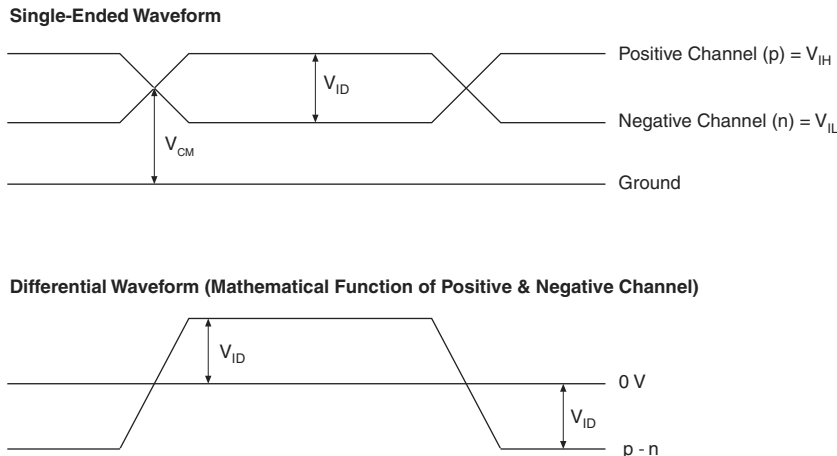
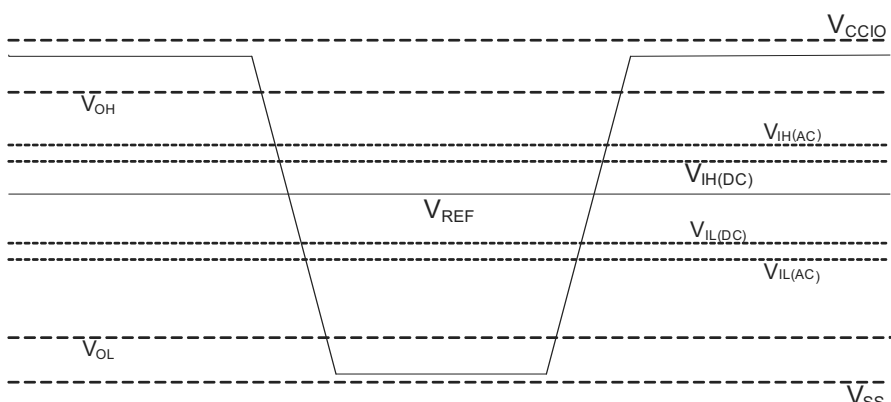
Letter	Term	Definitions
R	R_L	Receiver differential input discrete resistor (external to Cyclone IV devices).
	Receiver Input Waveform	<p>Receiver input waveform for LVDS and LVPECL differential standards:</p> 
	Receiver input skew margin (RSKM)	High-speed I/O block: The total margin left after accounting for the sampling window and TCCS. $RSKM = (TUI - SW - TCCS) / 2$.
S	Single-ended voltage-referenced I/O Standard	 <p>The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform <i>ringing</i>.</p>
	SW (Sampling Window)	High-speed I/O block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window.

Table 1-46. Glossary (Part 4 of 5)

Letter	Term	Definitions
T	t_C	High-speed receiver and transmitter input and output clock period.
	Channel-to-channel-skew (TCCS)	High-speed I/O block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
	t_{cin}	Delay from the clock pad to the I/O input register.
	t_{CO}	Delay from the clock pad to the I/O output.
	t_{cout}	Delay from the clock pad to the I/O output register.
	t_{DUTY}	High-speed I/O block: Duty cycle on high-speed transmitter output clock.
	t_{FALL}	Signal high-to-low transition time (80–20%).
	t_H	Input register hold time.
	Timing Unit Interval (TUI)	High-speed I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency Multiplication Factor}) = t_C/w$).
	$t_{INJITTER}$	Period jitter on the PLL clock input.
	$t_{OUTJITTER_DEDCLK}$	Period jitter on the dedicated clock output driven by a PLL.
	$t_{OUTJITTER_IO}$	Period jitter on the general purpose I/O driven by a PLL.
	t_{pllcin}	Delay from the PLL inclk pad to the I/O input register.
	$t_{pllcout}$	Delay from the PLL inclk pad to the I/O output register.
	Transmitter Output Waveform	<p>Transmitter output waveforms for the LVDS, mini-LVDS, PPDS and RSDS Differential I/O Standards:</p> <p>Single-Ended Waveform</p> <p>Positive Channel (p) = V_{OH}</p> <p>Negative Channel (n) = V_{OL}</p> <p>Ground</p> <p>V_{OD}</p> <p>V_{OS}</p> <p>Differential Waveform (Mathematical Function of Positive & Negative Channel)</p> <p>V_{OD}</p> <p>0 V</p> <p>V_{OD}</p> <p>p - n</p>
	t_{RISE}	Signal low-to-high transition time (20–80%).
	t_{SU}	Input register setup time.
U	—	—

Table 1-46. Glossary (Part 5 of 5)

Letter	Term	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	$V_{DIF(AC)}$	AC differential input voltage: The minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage: The minimum DC input differential voltage required for switching.
	V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V_{IH}	Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage.
	$V_{IH(DC)}$	High-level DC input voltage.
	V_{IL}	Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage.
	$V_{IL(DC)}$	Low-level DC input voltage.
	V_{IN}	DC input voltage.
	V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} - V_{OL}$.
	V_{OH}	Voltage output high: The maximum positive voltage from an output that the device considers is accepted as the minimum positive high level.
	V_{OL}	Voltage output low: The maximum positive voltage from an output that the device considers is accepted as the maximum positive low level.
	V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
	$V_{OX(AC)}$	AC differential output cross point voltage: the voltage at which the differential output signals must cross.
	V_{REF}	Reference voltage for the SSTL and HSTL I/O standards.
	$V_{REF(AC)}$	AC input reference voltage for the SSTL and HSTL I/O standards. $V_{REF(AC)} = V_{REF(DC)} + \text{noise}$. The peak-to-peak AC noise on V_{REF} must not exceed 2% of $V_{REF(DC)}$.
	$V_{REF(DC)}$	DC input reference voltage for the SSTL and HSTL I/O standards.
	$V_{SWING(AC)}$	AC differential input voltage: AC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	$V_{SWING(DC)}$	DC differential input voltage: DC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	V_{TT}	Termination voltage for the SSTL and HSTL I/O standards.
	$V_X(AC)$	AC differential input cross point voltage: The voltage at which the differential input signals must cross.
W	—	—
X	—	—
Y	—	—
Z	—	—

Document Revision History

Table 1-47 lists the revision history for this chapter.

Table 1-47. Document Revision History

Date	Version	Changes
March 2016	2.0	Updated note (5) in Table 1-21 to remove support for the N148 package.
October 2014	1.9	Updated maximum value for V_{CCD_PLL} in Table 1-1. Removed extended temperature note in Table 1-3.
December 2013	1.8	Updated Table 1-21 by adding Note (15).
May 2013	1.7	Updated Table 1-15 by adding Note (4).
October 2012	1.6	<ul style="list-style-type: none"> ■ Updated the maximum value for V_I, V_{CCD_PLL}, V_{CCIO}, V_{CC_CLKIN}, V_{CCH_GXB}, and V_{CCA_GXB} in Table 1-1. ■ Updated Table 1-11 and Table 1-22. ■ Updated Table 1-21 to include peak-to-peak differential input voltage for the Cyclone IV GX transceiver input reference clock. ■ Updated Table 1-29 to include the typical $DCLK$ value. ■ Updated the minimum f_{HCLK} value in Table 1-31, Table 1-32, Table 1-33, Table 1-34, and Table 1-35.
November 2011	1.5	<ul style="list-style-type: none"> ■ Updated “Maximum Allowed Overshoot or Undershoot Voltage”, “Operating Conditions”, and “PLL Specifications” sections. ■ Updated Table 1-2, Table 1-3, Table 1-4, Table 1-5, Table 1-8, Table 1-9, Table 1-15, Table 1-18, Table 1-19, and Table 1-21. ■ Updated Figure 1-1.
December 2010	1.4	<ul style="list-style-type: none"> ■ Updated for the Quartus II software version 10.1 release. ■ Updated Table 1-21 and Table 1-25. ■ Minor text edits.
July 2010	1.3	<p>Updated for the Quartus II software version 10.0 release:</p> <ul style="list-style-type: none"> ■ Updated Table 1-3, Table 1-4, Table 1-21, Table 1-25, Table 1-28, Table 1-30, Table 1-40, Table 1-41, Table 1-42, Table 1-43, Table 1-44, and Table 1-45. ■ Updated Figure 1-2 and Figure 1-3. ■ Removed SW Requirement and TCCS for Cyclone IV Devices tables. ■ Minor text edits.
March 2010	1.2	<p>Updated to include automotive devices:</p> <ul style="list-style-type: none"> ■ Updated the “Operating Conditions” and “PLL Specifications” sections. ■ Updated Table 1-1, Table 1-8, Table 1-9, Table 1-21, Table 1-26, Table 1-27, Table 1-31, Table 1-32, Table 1-33, Table 1-34, Table 1-35, Table 1-36, Table 1-37, Table 1-38, Table 1-40, Table 1-42, and Table 1-43. ■ Added Table 1-5 to include ESD for Cyclone IV devices GPIOs and HSSI I/Os. ■ Added Table 1-44 and Table 1-45 to include IOE programmable delay for Cyclone IV E 1.2 V core voltage devices. ■ Minor text edits.

Table 1–47. Document Revision History

Date	Version	Changes
February 2010	1.1	<ul style="list-style-type: none">■ Updated Table 1–3 through Table 1–44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release.■ Minor text edits.
November 2009	1.0	Initial release.

