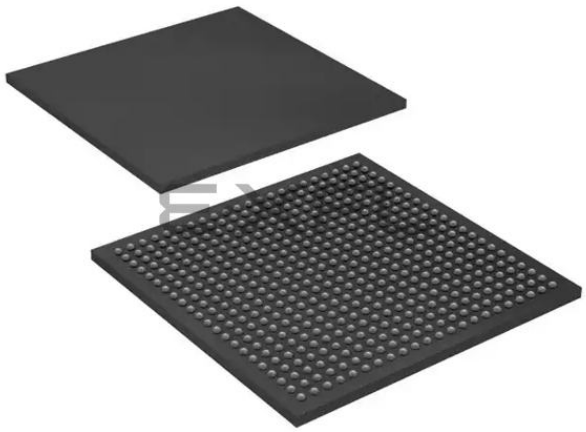

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 4713 |
| Number of Logic Elements/Cells | 75408 |
| Total RAM Bits | 2810880 |
| Number of I/O | 292 |
| Number of Gates | - |
| Voltage - Supply | 1.15V ~ 1.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep4ce75f23c6n |

## Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone IV devices. Table 1–3 and Table 1–4 list the steady-state voltage and current values expected from Cyclone IV E and Cyclone IV GX devices. All supplies must be strictly monotonic without plateaus.

**Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices (1), (2) (Part 1 of 2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CCINT}$ (3) | Supply voltage for internal logic, 1.2-V operation | — | 1.15 | 1.2 | 1.25 | V |
| | Supply voltage for internal logic, 1.0-V operation | — | 0.97 | 1.0 | 1.03 | V |
| $V_{CCIO}$ (3), (4) | Supply voltage for output buffers, 3.3-V operation | — | 3.135 | 3.3 | 3.465 | V |
| | Supply voltage for output buffers, 3.0-V operation | — | 2.85 | 3 | 3.15 | V |
| | Supply voltage for output buffers, 2.5-V operation | — | 2.375 | 2.5 | 2.625 | V |
| | Supply voltage for output buffers, 1.8-V operation | — | 1.71 | 1.8 | 1.89 | V |
| | Supply voltage for output buffers, 1.5-V operation | — | 1.425 | 1.5 | 1.575 | V |
| | Supply voltage for output buffers, 1.2-V operation | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CCA}$ (3) | Supply (analog) voltage for PLL regulator | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCD\_PLL}$ (3) | Supply (digital) voltage for PLL, 1.2-V operation | — | 1.15 | 1.2 | 1.25 | V |
| | Supply (digital) voltage for PLL, 1.0-V operation | — | 0.97 | 1.0 | 1.03 | V |
| $V_I$ | Input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | For commercial use | 0 | — | 85 | °C |
| | | For industrial use | –40 | — | 100 | °C |
| | | For extended temperature | –40 | — | 125 | °C |
| | | For automotive use | –40 | — | 125 | °C |
| $t_{RAMP}$ | Power supply ramp time | Standard power-on reset (POR) (5) | 50 µs | — | 50 ms | — |
| | | Fast POR (6) | 50 µs | — | 3 ms | — |

**Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices (1), (2) (Part 2 of 2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{Diode}$ | Magnitude of DC current across PCI-clamp diode when enable | — | — | — | 10 | mA |

**Notes to Table 1–3:**

(1) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades.

(2) $V_{CCIO}$ for all I/O banks must be powered up during device operation. All VCCA pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.

(3) $V_{CC}$ must rise monotonically.

(4) $V_{CCIO}$ powers all input buffers.

(5) The POR time for Standard POR ranges between 50 and 200 ms. Each individual power supply must reach the recommended operating range within 50 ms.

(6) The POR time for Fast POR ranges between 3 and 9 ms. Each individual power supply must reach the recommended operating range within 3 ms.

**Table 1–4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 1 of 2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CCINT}$ (3) | Core voltage, PCIe hard IP block, and transceiver PCS power supply | — | 1.16 | 1.2 | 1.24 | V |
| $V_{CCA}$ (1), (3) | PLL analog power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCD\_PLL}$ (2) | PLL digital power supply | — | 1.16 | 1.2 | 1.24 | V |
| $V_{CCIO}$ (3), (4) | I/O banks power supply for 3.3-V operation | — | 3.135 | 3.3 | 3.465 | V |
| | I/O banks power supply for 3.0-V operation | — | 2.85 | 3 | 3.15 | V |
| | I/O banks power supply for 2.5-V operation | — | 2.375 | 2.5 | 2.625 | V |
| | I/O banks power supply for 1.8-V operation | — | 1.71 | 1.8 | 1.89 | V |
| | I/O banks power supply for 1.5-V operation | — | 1.425 | 1.5 | 1.575 | V |
| | I/O banks power supply for 1.2-V operation | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CC\_CLKIN}$ (3), (5), (6) | Differential clock input pins power supply for 3.3-V operation | — | 3.135 | 3.3 | 3.465 | V |
| | Differential clock input pins power supply for 3.0-V operation | — | 2.85 | 3 | 3.15 | V |
| | Differential clock input pins power supply for 2.5-V operation | — | 2.375 | 2.5 | 2.625 | V |
| | Differential clock input pins power supply for 1.8-V operation | — | 1.71 | 1.8 | 1.89 | V |
| | Differential clock input pins power supply for 1.5-V operation | — | 1.425 | 1.5 | 1.575 | V |
| | Differential clock input pins power supply for 1.2-V operation | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CCH\_GXB}$ | Transceiver output buffer power supply | — | 2.375 | 2.5 | 2.625 | V |

**Table 1–4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CCA\_GXB}$ | Transceiver PMA and auxiliary power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCL\_GXB}$ | Transceiver PMA and auxiliary power supply | — | 1.16 | 1.2 | 1.24 | V |
| $V_I$ | DC input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | DC output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | For commercial use | 0 | — | 85 | °C |
| | | For industrial use | –40 | — | 100 | °C |
| $t_{RAMP}$ | Power supply ramp time | Standard power-on reset (POR) *(7)* | 50 µs | — | 50 ms | — |
| | | Fast POR *(8)* | 50 µs | — | 3 ms | — |
| $I_{Diode}$ | Magnitude of DC current across PCI-clamp diode when enabled | — | — | — | 10 | mA |

**Notes to Table 1–4:**

(1) All VCCA pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.

(2) You must connect $V_{CCD\_PLL}$ to $V_{CCINT}$ through a decoupling capacitor and ferrite bead.

(3) Power supplies must rise monotonically.

(4) $V_{CCIO}$ for all I/O banks must be powered up during device operation. Configurations pins are powered up by $V_{CCIO}$ of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support $V_{CCIO}$ of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the $V_{CCIO}$ level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.

(5) You must set $V_{CC\_CLKIN}$ to 2.5 V if you use CLKIN as a high-speed serial interface (HSSI) refclk or as a DIFFCLK input.

(6) The CLKIN pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.

(7) The POR time for Standard POR ranges between 50 and 200 ms. $V_{CCINT}$, $V_{CCA}$, and $V_{CCIO}$ of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.

(8) The POR time for Fast POR ranges between 3 and 9 ms. $V_{CCINT}$, $V_{CCA}$, and $V_{CCIO}$ of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

## ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1–5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

**Table 1–5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os**

| Symbol | Parameter | Passing Voltage | Unit |
|---|---|---|---|
| $V_{ESDHBM}$ | ESD voltage using the HBM (GPIOs) *(1)* | ± 2000 | V |
| | ESD using the HBM (HSSI I/Os) *(2)* | ± 1000 | V |
| $V_{ESDCDM}$ | ESD using the CDM (GPIOs) | ± 500 | V |
| | ESD using the CDM (HSSI I/Os) *(2)* | ± 250 | V |

**Notes to Table 1–5:**

(1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is ±1000V.

(2) This value is applicable only to Cyclone IV GX devices.

# DC Characteristics

This section lists the I/O leakage current, pin capacitance, on-chip termination (OCT) tolerance, and bus hold specifications for Cyclone IV devices.

## Supply Current

The device supply current requirement is the minimum current drawn from the power supply pins that can be used as a reference for power size planning. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary greatly with the resources used. Table 1–6 lists the I/O pin leakage current for Cyclone IV devices.

**Table 1–6. I/O Pin Leakage Current for Cyclone IV Devices** *(1), (2)*

| Symbol | Parameter | Conditions | Device | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current | $V_I$ = 0 V to $V_{CCIOMAX}$ | — | –10 | — | 10 | µA |
| $I_{OZ}$ | Tristated I/O pin leakage current | $V_O$ = 0 V to $V_{CCIOMAX}$ | — | –10 | — | 10 | µA |

**Notes to Table 1–6:**

(1) This value is specified for normal device operation. The value varies during device power-up. This applies for all $V_{CCIO}$ settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) The 10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

## Bus Hold

The bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1–7 lists bus hold specifications for Cyclone IV devices.

**Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 1 of 2)** *(1)*

| Parameter | Condition | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus hold low, sustaining current | $V_{IN} > V_{IL}$ (maximum) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | µA |
| Bus hold high, sustaining current | $V_{IN} < V_{IL}$ (minimum) | –8 | — | –12 | — | –30 | — | –50 | — | –70 | — | –70 | — | µA |
| Bus hold low, overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | µA |
| Bus hold high, overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | –125 | — | –175 | — | –200 | — | –300 | — | –500 | — | –500 | µA |

**Table 1–16. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Cyclone IV Devices** *(1)*

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) *(2)* | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 1.19 | 1.25 | 1.31 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.7 | 1.8 | 1.9 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | 0.85 | 0.9 | 0.95 |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.71 | 0.75 | 0.79 | 0.71 | 0.75 | 0.79 |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.48 x $V_{CCIO}$ *(3)* | 0.5 x $V_{CCIO}$ *(3)* | 0.52 x $V_{CCIO}$ *(3)* | — | 0.5 x $V_{CCIO}$ | — |
| | | | | 0.47 x $V_{CCIO}$ *(4)* | 0.5 x $V_{CCIO}$ *(4)* | 0.53 x $V_{CCIO}$ *(4)* | | | |

**Notes to Table 1–16:**

(1) For an explanation of terms used in Table 1–16, refer to "Glossary" on page 1–37.
(2) $V_{TT}$ of the transmitting device must track $V_{REF}$ of the receiving device.
(3) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.
(4) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

**Table 1–17. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone IV Devices**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | | $V_{IH(AC)}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Max | Min | | |
| SSTL-2 Class I | — | $V_{REF}$ – 0.18 | $V_{REF}$ + 0.18 | — | — | $V_{REF}$ – 0.35 | $V_{REF}$ + 0.35 | — | $V_{TT}$ – 0.57 | $V_{TT}$ + 0.57 | 8.1 | –8.1 |
| SSTL-2 Class II | — | $V_{REF}$ – 0.18 | $V_{REF}$ + 0.18 | — | — | $V_{REF}$ – 0.35 | $V_{REF}$ + 0.35 | — | $V_{TT}$ – 0.76 | $V_{TT}$ + 0.76 | 16.4 | –16.4 |
| SSTL-18 Class I | — | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | — | — | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | — | $V_{TT}$ – 0.475 | $V_{TT}$ + 0.475 | 6.7 | –6.7 |
| SSTL-18 Class II | — | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | — | — | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | — | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |
| HSTL-18 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-18 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-12 Class I | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | –0.24 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.24 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 8 | –8 |
| HSTL-12 Class II | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | –0.24 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.24 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 14 | –14 |

**Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 2 of 4)**

| Symbol/ Description | Conditions | C6 | | | C7, I7 | | | C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Receiver** | | | | | | | | | | | |
| Supported I/O Standards | 1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS | | | | | | | | | | |
| Data rate (F324 and smaller package) *(15)* | — | 600 | — | 2500 | 600 | — | 2500 | 600 | — | 2500 | Mbps |
| Data rate (F484 and larger package) *(15)* | — | 600 | — | 3125 | 600 | — | 3125 | 600 | — | 2500 | Mbps |
| Absolute $V_{MAX}$ for a receiver pin *(3)* | — | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| Operational $V_{MAX}$ for a receiver pin | — | — | — | 1.5 | — | — | 1.5 | — | — | 1.5 | V |
| Absolute $V_{MIN}$ for a receiver pin | — | –0.4 | — | — | –0.4 | — | — | –0.4 | — | — | V |
| Peak-to-peak differential input voltage $V_{ID}$ (diff p-p) | $V_{ICM}$ = 0.82 V setting, Data Rate = 600 Mbps to 3.125 Gbps | 0.1 | — | 2.7 | 0.1 | — | 2.7 | 0.1 | — | 2.7 | V |
| $V_{ICM}$ | $V_{ICM}$ = 0.82 V setting | — | 820 ± 10% | — | — | 820 ± 10% | — | — | 820 ± 10% | — | mV |
| Differential on-chip termination resistors | 100–Ω setting | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| | 150–Ω setting | — | 150 | — | — | 150 | — | — | 150 | — | Ω |
| Differential and common mode return loss | PIPE, Serial Rapid I/O SR, SATA, CPRI LV, SDI, XAUI | Compliant | | | | | | | | | — |
| Programmable ppm detector *(4)* | — | ± 62.5, 100, 125, 200, 250, 300 | | | | | | | | | ppm |
| Clock data recovery (CDR) ppm tolerance (without spread-spectrum clocking enabled) | — | — | — | ±300 *(5)*, ±350 *(6)*, *(7)* | — | — | ±300 *(5)*, ±350 *(6)*, *(7)* | — | — | ±300 *(5)*, ±350 *(6)*, *(7)* | ppm |
| CDR ppm tolerance (with synchronous spread-spectrum clocking enabled) *(8)* | — | — | — | 350 to –5350 *(7)*, *(9)* | — | — | 350 to –5350 *(7)*, *(9)* | — | — | 350 to –5350 *(7)*, *(9)* | ppm |
| Run length | — | — | 80 | — | — | 80 | — | — | 80 | — | UI |
| Programmable equalization | No Equalization | — | — | 1.5 | — | — | 1.5 | — | — | 1.5 | dB |
| | Medium Low | — | — | 4.5 | — | — | 4.5 | — | — | 4.5 | dB |
| | Medium High | — | — | 5.5 | — | — | 5.5 | — | — | 5.5 | dB |
| | High | — | — | 7 | — | — | 7 | — | — | 7 | dB |

Table 1–23 lists the Cyclone IV GX transceiver block AC specifications.

**Table 1–23. Transceiver Block AC Specification for Cyclone IV GX Devices** *(1), (2)*

| Symbol/ Description | Conditions | C6 | | | C7, I7 | | | C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **PCIe Transmit Jitter Generation** *(3)* | | | | | | | | | | | |
| Total jitter at 2.5 Gbps (Gen1) | Compliance pattern | — | — | 0.25 | — | — | 0.25 | — | — | 0.25 | UI |
| **PCIe Receiver Jitter Tolerance** *(3)* | | | | | | | | | | | |
| Total jitter at 2.5 Gbps (Gen1) | Compliance pattern | > 0.6 | | | > 0.6 | | | > 0.6 | | | UI |
| **GIGE Transmit Jitter Generation** *(4)* | | | | | | | | | | | |
| Deterministic jitter (peak-to-peak) | Pattern = CRPAT | — | — | 0.14 | — | — | 0.14 | — | — | 0.14 | UI |
| Total jitter (peak-to-peak) | Pattern = CRPAT | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | UI |
| **GIGE Receiver Jitter Tolerance** *(4)* | | | | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Pattern = CJPAT | > 0.4 | | | > 0.4 | | | > 0.4 | | | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Pattern = CJPAT | > 0.66 | | | > 0.66 | | | > 0.66 | | | UI |

**Notes to Table 1–23:**

(1) Dedicated `refclk` pins were used to drive the input reference clocks.
(2) The jitter numbers specified are valid for the stated conditions only.
(3) The jitter numbers for PIPE are compliant to the PCIe Base Specification 2.0.
(4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.

# Core Performance Specifications

The following sections describe the clock tree specifications, PLLs, embedded multiplier, memory block, and configuration specifications for Cyclone IV Devices.

## Clock Tree Specifications

Table 1–24 lists the clock tree specifications for Cyclone IV devices.

**Table 1–24. Clock Tree Performance for Cyclone IV Devices** ***(Part 1 of 2)***

| Device | Performance | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | C6 | C7 | C8 | C8L *(1)* | C9L *(1)* | I7 | I8L *(1)* | A7 | |
| EP4CE6 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | 402 | MHz |
| EP4CE10 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | 402 | MHz |
| EP4CE15 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | 402 | MHz |
| EP4CE22 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | 402 | MHz |
| EP4CE30 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | 402 | MHz |
| EP4CE40 | 500 | 437.5 | 402 | 362 | 265 | 437.5 | 362 | 402 | MHz |

**Table 1–25. PLL Specifications for Cyclone IV Devices (1), (2) (Part 2 of 2)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or areset is deasserted) | — | — | 1 | ms |
| $t_{OUTJITTER\_PERIOD\_DEDCLK}$ (6) | Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz | — | — | 300 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 30 | mUI |
| $t_{OUTJITTER\_CCJ\_DEDCLK}$ (6) | Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz | — | — | 300 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 30 | mUI |
| $t_{OUTJITTER\_PERIOD\_IO}$ (6) | Regular I/O period jitter $F_{OUT} \geq 100$ MHz | — | — | 650 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 75 | mUI |
| $t_{OUTJITTER\_CCJ\_IO}$ (6) | Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz | — | — | 650 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 75 | mUI |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on areset signal. | 10 | — | — | ns |
| $t_{CONFIGPLL}$ | Time required to reconfigure scan chains for PLLs | — | 3.5 (7) | — | SCANCLK cycles |
| $f_{SCANCLK}$ | scanclk frequency | — | — | 100 | MHz |
| $t_{CASC\_OUTJITTER\_PERIOD\_DEDCLK}$ (8), (9) | Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz) | — | — | 425 | ps |
| | Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz) | — | — | 42.5 | mUI |

**Notes to Table 1–25:**

(1) This table is applicable for general purpose PLLs and multipurpose PLLs.

(2) You must connect $V_{CCD\_PLL}$ to $V_{CCINT}$ through the decoupling capacitor and ferrite bead.

(3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(4) The $V_{CO}$ frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the $V_{CO}$ post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.

(6) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.

(7) With 100-MHz scanclk frequency.

(8) The cascaded PLLs specification is applicable only with the following conditions:

- Upstream PLL—0.59 MHz ≤ Upstream PLL bandwidth < 1 MHz
- Downstream PLL—Downstream PLL bandwidth > 2 MHz

(9) PLL cascading is not supported for transceiver applications.

For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interfaces Handbook*.

Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specifications

Table 1–31 through Table 1–36 list the high-speed I/O timing for Cyclone IV devices. For definitions of high-speed timing specifications, refer to "Glossary" on page 1–37.

**Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4) (Part 1 of 2)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×8 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×7 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×4 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×2 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×1 | 5 | — | 360 | 5 | — | 311 | 5 | — | 311 | 5 | — | 311 | 5 | — | 265 | MHz |
| Device operation in Mbps | ×10 | 100 | — | 360 | 100 | — | 311 | 100 | — | 311 | 100 | — | 311 | 100 | — | 265 | Mbps |
| | ×8 | 80 | — | 360 | 80 | — | 311 | 80 | — | 311 | 80 | — | 311 | 80 | — | 265 | Mbps |
| | ×7 | 70 | — | 360 | 70 | — | 311 | 70 | — | 311 | 70 | — | 311 | 70 | — | 265 | Mbps |
| | ×4 | 40 | — | 360 | 40 | — | 311 | 40 | — | 311 | 40 | — | 311 | 40 | — | 265 | Mbps |
| | ×2 | 20 | — | 360 | 20 | — | 311 | 20 | — | 311 | 20 | — | 311 | 20 | — | 265 | Mbps |
| | ×1 | 10 | — | 360 | 10 | — | 311 | 10 | — | 311 | 10 | — | 311 | 10 | — | 265 | Mbps |
| $t_{DUTY}$ | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| Transmitter channel-to-channel skew (TCCS) | — | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 550 | — | — | 600 | — | — | 700 | ps |
| $t_{RISE}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |

**Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 2 of 2)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{LOCK}$ (2) | — | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | ms |

**Notes to Table 1–32:**

(1) Emulated RSDS_E_1R transmitter is supported at the output pin of all I/O Banks of Cyclone IV E devices and I/O Banks 3, 4, 5, 6, 7, 8, and 9 of Cyclone IV GX devices.

(2) $t_{LOCK}$ is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

**Table 1–33. Mini-LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×8 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×7 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×4 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×2 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×1 | 5 | — | 400 | 5 | — | 311 | 5 | — | 311 | 5 | — | 311 | 5 | — | 265 | MHz |
| Device operation in Mbps | ×10 | 100 | — | 400 | 100 | — | 311 | 100 | — | 311 | 100 | — | 311 | 100 | — | 265 | Mbps |
| | ×8 | 80 | — | 400 | 80 | — | 311 | 80 | — | 311 | 80 | — | 311 | 80 | — | 265 | Mbps |
| | ×7 | 70 | — | 400 | 70 | — | 311 | 70 | — | 311 | 70 | — | 311 | 70 | — | 265 | Mbps |
| | ×4 | 40 | — | 400 | 40 | — | 311 | 40 | — | 311 | 40 | — | 311 | 40 | — | 265 | Mbps |
| | ×2 | 20 | — | 400 | 20 | — | 311 | 20 | — | 311 | 20 | — | 311 | 20 | — | 265 | Mbps |
| | ×1 | 10 | — | 400 | 10 | — | 311 | 10 | — | 311 | 10 | — | 311 | 10 | — | 265 | Mbps |
| $t_{DUTY}$ | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS | — | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 550 | — | — | 600 | — | — | 700 | ps |
| $t_{RISE}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ (3) | — | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | ms |

**Notes to Table 1–33:**

(1) Applicable for true and emulated mini-LVDS transmitter.

(2) Cyclone IV E—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated mini-LVDS transmitter is supported at the output pin of all I/O banks.
Cyclone IV GX—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(3) $t_{LOCK}$ is the time required for the PLL to lock from the end-of-device configuration.

(4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

**Table 1–34. True LVDS Transmitter Timing Specifications for Cyclone IV Devices** *(1), (3)*

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | C8L, I8L | | C9L | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | 420 | 5 | 370 | 5 | 320 | 5 | 320 | 5 | 250 | MHz |
| | ×8 | 5 | 420 | 5 | 370 | 5 | 320 | 5 | 320 | 5 | 250 | MHz |
| | ×7 | 5 | 420 | 5 | 370 | 5 | 320 | 5 | 320 | 5 | 250 | MHz |
| | ×4 | 5 | 420 | 5 | 370 | 5 | 320 | 5 | 320 | 5 | 250 | MHz |
| | ×2 | 5 | 420 | 5 | 370 | 5 | 320 | 5 | 320 | 5 | 250 | MHz |
| | ×1 | 5 | 420 | 5 | 402.5 | 5 | 402.5 | 5 | 362 | 5 | 265 | MHz |
| HSIODR | ×10 | 100 | 840 | 100 | 740 | 100 | 640 | 100 | 640 | 100 | 500 | Mbps |
| | ×8 | 80 | 840 | 80 | 740 | 80 | 640 | 80 | 640 | 80 | 500 | Mbps |
| | ×7 | 70 | 840 | 70 | 740 | 70 | 640 | 70 | 640 | 70 | 500 | Mbps |
| | ×4 | 40 | 840 | 40 | 740 | 40 | 640 | 40 | 640 | 40 | 500 | Mbps |
| | ×2 | 20 | 840 | 20 | 740 | 20 | 640 | 20 | 640 | 20 | 500 | Mbps |
| | ×1 | 10 | 420 | 10 | 402.5 | 10 | 402.5 | 10 | 362 | 10 | 265 | Mbps |
| $t_{DUTY}$ | — | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |
| TCCS | — | — | 200 | — | 200 | — | 200 | — | 200 | — | 200 | ps |
| Output jitter (peak to peak) | — | — | 500 | — | 500 | — | 550 | — | 600 | — | 700 | ps |
| $t_{LOCK}$ *(2)* | — | — | 1 | — | 1 | — | 1 | — | 1 | — | 1 | ms |

**Notes to Table 1–34:**

(1) Cyclone IV E—true LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6.
Cyclone IV GX—true LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6.

(2) $t_{LOCK}$ is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

**Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices** *(1), (3)* **(Part 1 of 2)**

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | C8L, I8L | | C9L | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | 320 | 5 | 320 | 5 | 275 | 5 | 275 | 5 | 250 | MHz |
| | ×8 | 5 | 320 | 5 | 320 | 5 | 275 | 5 | 275 | 5 | 250 | MHz |
| | ×7 | 5 | 320 | 5 | 320 | 5 | 275 | 5 | 275 | 5 | 250 | MHz |
| | ×4 | 5 | 320 | 5 | 320 | 5 | 275 | 5 | 275 | 5 | 250 | MHz |
| | ×2 | 5 | 320 | 5 | 320 | 5 | 275 | 5 | 275 | 5 | 250 | MHz |
| | ×1 | 5 | 402.5 | 5 | 402.5 | 5 | 402.5 | 5 | 362 | 5 | 265 | MHz |
| HSIODR | ×10 | 100 | 640 | 100 | 640 | 100 | 550 | 100 | 550 | 100 | 500 | Mbps |
| | ×8 | 80 | 640 | 80 | 640 | 80 | 550 | 80 | 550 | 80 | 500 | Mbps |
| | ×7 | 70 | 640 | 70 | 640 | 70 | 550 | 70 | 550 | 70 | 500 | Mbps |
| | ×4 | 40 | 640 | 40 | 640 | 40 | 550 | 40 | 550 | 40 | 500 | Mbps |
| | ×2 | 20 | 640 | 20 | 640 | 20 | 550 | 20 | 550 | 20 | 500 | Mbps |
| | ×1 | 10 | 402.5 | 10 | 402.5 | 10 | 402.5 | 10 | 362 | 10 | 265 | Mbps |

**Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 2 of 2)**

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | C8L, I8L | | C9L | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{DUTY}$ | — | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |
| TCCS | — | — | 200 | — | 200 | — | 200 | — | 200 | — | 200 | ps |
| Output jitter (peak to peak) | — | — | 500 | — | 500 | — | 550 | — | 600 | — | 700 | ps |
| $t_{LOCK}$ (2) | — | — | 1 | — | 1 | — | 1 | — | 1 | — | 1 | ms |

**Notes to Table 1–35:**

(1) Cyclone IV E—emulated LVDS transmitter is supported at the output pin of all I/O Banks.
Cyclone IV GX—emulated LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(2) $t_{LOCK}$ is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

**Table 1–36. LVDS Receiver Timing Specifications for Cyclone IV Devices (1), (3)**

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | C8L, I8L | | C9L | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×8 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×7 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×4 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×2 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×1 | 10 | 437.5 | 10 | 402.5 | 10 | 402.5 | 10 | 362 | 10 | 265 | MHz |
| HSIODR | ×10 | 100 | 875 | 100 | 740 | 100 | 640 | 100 | 640 | 100 | 500 | Mbps |
| | ×8 | 80 | 875 | 80 | 740 | 80 | 640 | 80 | 640 | 80 | 500 | Mbps |
| | ×7 | 70 | 875 | 70 | 740 | 70 | 640 | 70 | 640 | 70 | 500 | Mbps |
| | ×4 | 40 | 875 | 40 | 740 | 40 | 640 | 40 | 640 | 40 | 500 | Mbps |
| | ×2 | 20 | 875 | 20 | 740 | 20 | 640 | 20 | 640 | 20 | 500 | Mbps |
| | ×1 | 10 | 437.5 | 10 | 402.5 | 10 | 402.5 | 10 | 362 | 10 | 265 | Mbps |
| SW | — | — | 400 | — | 400 | — | 400 | — | 550 | — | 640 | ps |
| Input jitter tolerance | — | — | 500 | — | 500 | — | 550 | — | 600 | — | 700 | ps |
| $t_{LOCK}$ (2) | — | — | 1 | — | 1 | — | 1 | — | 1 | — | 1 | ms |

**Notes to Table 1–36:**

(1) Cyclone IV E—LVDS receiver is supported at all I/O Banks.
Cyclone IV GX—LVDS receiver is supported at I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(2) $t_{LOCK}$ is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

## External Memory Interface Specifications

The external memory interfaces for Cyclone IV devices are auto-calibrating and easy to implement.

## IOE Programmable Delay

Table 1–40 and Table 1–41 list the IOE programmable delay for Cyclone IV E 1.0 V core voltage devices.

**Table 1–40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | |
| | | | | C8L | I8L | C8L | C9L | I8L | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 2.054 | 1.924 | 3.387 | 4.017 | 3.411 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 2.010 | 1.875 | 3.341 | 4.252 | 3.367 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.641 | 0.631 | 1.111 | 1.377 | 1.124 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.971 | 0.931 | 1.684 | 2.298 | 1.684 | ns |

**Notes to Table 1–40:**

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–41. IOE Programmable Delay on Row Pins for Cyclone IV E 1.0 V Core Voltage Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | |
| | | | | C8L | I8L | C8L | C9L | I8L | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 2.057 | 1.921 | 3.389 | 4.146 | 3.412 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 2.059 | 1.919 | 3.420 | 4.374 | 3.441 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.670 | 0.623 | 1.160 | 1.420 | 1.168 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.960 | 0.919 | 1.656 | 2.258 | 1.656 | ns |

**Notes to Table 1–41:**

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

**Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | | Slow Corner | | | | | |
| | | | | C6 | I7 | A7 | C6 | C7 | C8 | I7 | A7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.314 | 1.211 | 1.211 | 2.177 | 2.340 | 2.433 | 2.388 | 2.508 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.307 | 1.203 | 1.203 | 2.19 | 2.387 | 2.540 | 2.430 | 2.545 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.437 | 0.402 | 0.402 | 0.747 | 0.820 | 0.880 | 0.834 | 0.873 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.693 | 0.665 | 0.665 | 1.200 | 1.379 | 1.532 | 1.393 | 1.441 | ns |

**Notes to Table 1–42:**

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | | Slow Corner | | | | | |
| | | | | C6 | I7 | A7 | C6 | C7 | C8 | I7 | A7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.314 | 1.209 | 1.209 | 2.201 | 2.386 | 2.510 | 2.429 | 2.548 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.312 | 1.207 | 1.207 | 2.202 | 2.402 | 2.558 | 2.447 | 2.557 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.458 | 0.419 | 0.419 | 0.783 | 0.861 | 0.924 | 0.875 | 0.915 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.686 | 0.657 | 0.657 | 1.185 | 1.360 | 1.506 | 1.376 | 1.422 | ns |

**Notes to Table 1–43:**

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

**Table 1–44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Settings | Min Offset | Max Offset | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | | |
| | | | | C6 | I7 | C6 | C7 | C8 | I7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.313 | 1.209 | 2.184 | 2.336 | 2.451 | 2.387 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.312 | 1.208 | 2.200 | 2.399 | 2.554 | 2.446 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.438 | 0.404 | 0.751 | 0.825 | 0.886 | 0.839 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.713 | 0.682 | 1.228 | 1.41 | 1.566 | 1.424 | ns |

**Notes to Table 1–44:**

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Settings | Min Offset | Max Offset | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | | |
| | | | | C6 | I7 | C6 | C7 | C8 | I7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.314 | 1.210 | 2.209 | 2.398 | 2.526 | 2.443 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.313 | 1.208 | 2.205 | 2.406 | 2.563 | 2.450 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.461 | 0.421 | 0.789 | 0.869 | 0.933 | 0.884 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.712 | 0.682 | 1.225 | 1.407 | 1.562 | 1.421 | ns |

**Notes to Table 1–45:**

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software

# I/O Timing

Use the following methods to determine I/O timing:

- the Excel-based I/O Timing
- the Quartus II timing analyzer

The Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get a timing budget estimation as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.

The Excel-based I/O Timing spreadsheet is downloadable from Cyclone IV Devices Literature website.

# Glossary

Table 1–46 lists the glossary for this chapter.

**Table 1–46. Glossary (Part 1 of 5)**

| Letter | Term | Definitions |
|---|---|---|
| A | — | — |
| B | — | — |
| C | — | — |
| D | — | — |
| E | — | — |
| F | $f_{HSCLK}$ | High-speed I/O block: High-speed receiver/transmitter input and output clock frequency. |
| G | GCLK | Input pin directly to Global Clock network. |
| | GCLK PLL | Input pin to Global Clock network through the PLL. |
| H | HSIODR | High-speed I/O block: Maximum/minimum LVDS data transfer rate (HSIODR = 1/TUI). |
| I | Input Waveforms for the SSTL Differential I/O Standard |  |

**Table 1–46. Glossary (Part 2 of 5)**

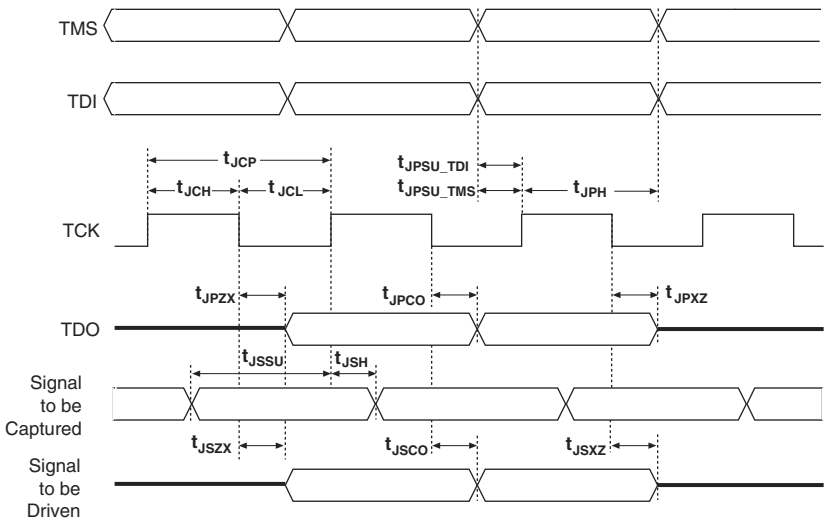
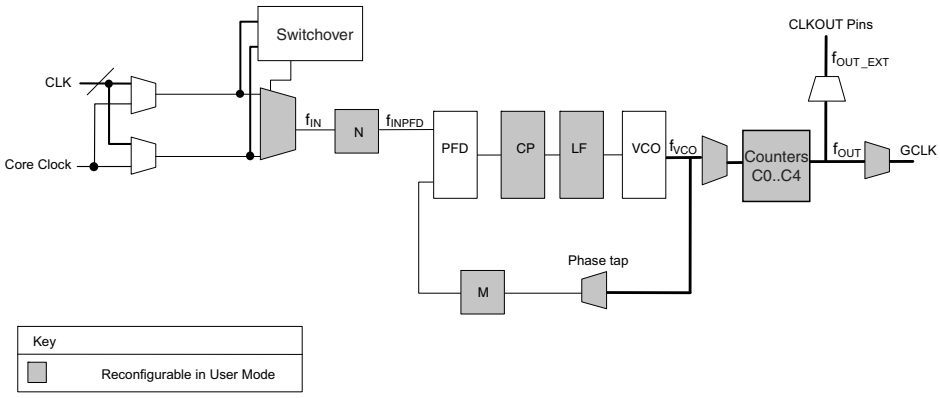
| Letter | Term | Definitions |
|---|---|---|
| J | JTAG Waveform |  |
| K | — | — |
| L | — | — |
| M | — | — |
| N | — | — |
| O | — | — |
| P | PLL Block | The following highlights the PLL specification parameters:  |
| Q | — | — |

**Table 1–46. Glossary (Part 3 of 5)**

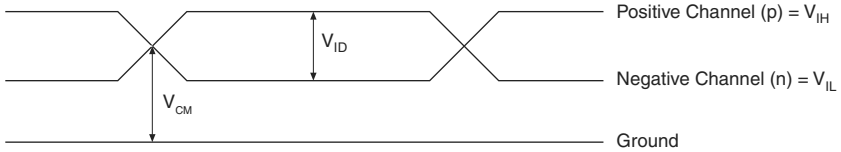
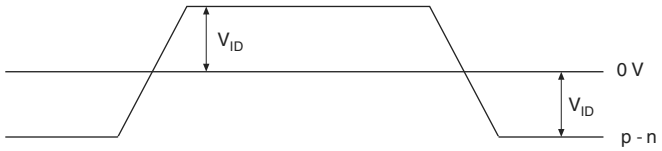
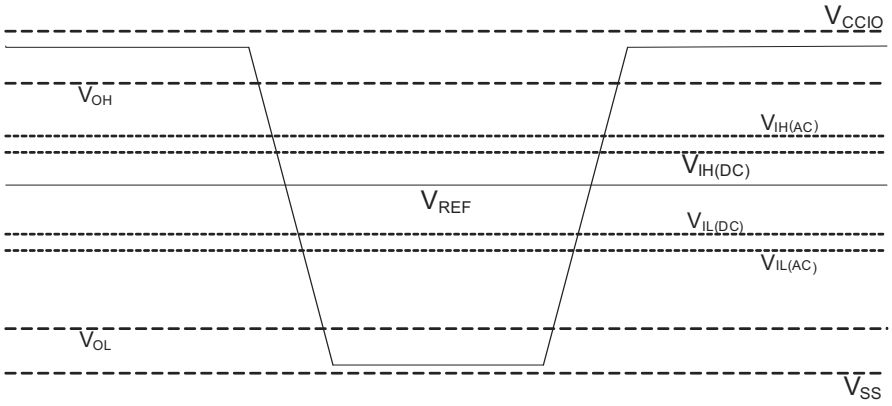
| Letter | Term | Definitions |
|---|---|---|
| R | $R_L$ | Receiver differential input discrete resistor (external to Cyclone IV devices). |
| | Receiver Input Waveform | Receiver input waveform for LVDS and LVPECL differential standards:<br>**Single-Ended Waveform**<br>  <br><br>**Differential Waveform (Mathematical Function of Positive & Negative Channel)**<br>  <br> |
| | Receiver input skew margin (RSKM) | High-speed I/O block: The total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2. |
| S | Single-ended voltage-referenced I/O Standard |  <br><br>The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform *ringing*. |
| | SW (Sampling Window) | High-speed I/O block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window. |

**Table 1–47. Document Revision History**

| Date | Version | Changes |
|---|---|---|
| February 2010 | 1.1 | ■ Updated Table 1–3 through Table 1–44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release.<br>■ Minor text edits. |
| November 2009 | 1.0 | Initial release. |