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Details

Product Status	Active
Number of LABs/CLBs	6839
Number of Logic Elements/Cells	109424
Total RAM Bits	5621760
Number of I/O	475
Number of Gates	-
Voltage - Supply	1.16V ~ 1.24V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4cgx110df31i7n

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone IV devices. Table 1–3 and Table 1–4 list the steady-state voltage and current values expected from Cyclone IV E and Cyclone IV GX devices. All supplies must be strictly monotonic without plateaus.

Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices ⁽¹⁾, ⁽²⁾ (Part 1 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CCINT}^{(3)}$	Supply voltage for internal logic, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply voltage for internal logic, 1.0-V operation	—	0.97	1.0	1.03	V
$V_{CCIO}^{(3), (4)}$	Supply voltage for output buffers, 3.3-V operation	—	3.135	3.3	3.465	V
	Supply voltage for output buffers, 3.0-V operation	—	2.85	3	3.15	V
	Supply voltage for output buffers, 2.5-V operation	—	2.375	2.5	2.625	V
	Supply voltage for output buffers, 1.8-V operation	—	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	—	1.425	1.5	1.575	V
	Supply voltage for output buffers, 1.2-V operation	—	1.14	1.2	1.26	V
$V_{CCA}^{(3)}$	Supply (analog) voltage for PLL regulator	—	2.375	2.5	2.625	V
$V_{CCD_PLL}^{(3)}$	Supply (digital) voltage for PLL, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply (digital) voltage for PLL, 1.0-V operation	—	0.97	1.0	1.03	V
V_I	Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
		For extended temperature	–40	—	125	°C
		For automotive use	–40	—	125	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR) ⁽⁵⁾	50 μ s	—	50 ms	—
		Fast POR ⁽⁶⁾	50 μ s	—	3 ms	—

Table 1-4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CCA_GXB}	Transceiver PMA and auxiliary power supply	—	2.375	2.5	2.625	V
V _{CCL_GXB}	Transceiver PMA and auxiliary power supply	—	1.16	1.2	1.24	V
V _I	DC input voltage	—	−0.5	—	3.6	V
V _O	DC output voltage	—	0	—	V _{CCIO}	V
T _J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	−40	—	100	°C
t _{RAMP}	Power supply ramp time	Standard power-on reset (POR) ⁽⁷⁾	50 μs	—	50 ms	—
		Fast POR ⁽⁸⁾	50 μs	—	3 ms	—
I _{Diode}	Magnitude of DC current across PCI-clamp diode when enabled	—	—	—	10	mA

Notes to Table 1-4:

- (1) All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- (2) You must connect V_{CCD_PLL} to V_{CCINT} through a decoupling capacitor and ferrite bead.
- (3) Power supplies must rise monotonically.
- (4) V_{CCIO} for all I/O banks must be powered up during device operation. Configurations pins are powered up by V_{CCIO} of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support V_{CCIO} of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the V_{CCIO} level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.
- (5) You must set V_{CC_CLKIN} to 2.5 V if you use CLKIN as a high-speed serial interface (HSSI) refclk or as a DIFFCLK input.
- (6) The CLKIN pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.
- (7) The POR time for Standard POR ranges between 50 and 200 ms. V_{CCINT}, V_{CCA}, and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.
- (8) The POR time for Fast POR ranges between 3 and 9 ms. V_{CCINT}, V_{CCA}, and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1-5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

Table 1-5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os

Symbol	Parameter	Passing Voltage	Unit
V _{ESDHBM}	ESD voltage using the HBM (GPIOs) ⁽¹⁾	± 2000	V
	ESD using the HBM (HSSI I/Os) ⁽²⁾	± 1000	V
V _{ESDCDM}	ESD using the CDM (GPIOs)	± 500	V
	ESD using the CDM (HSSI I/Os) ⁽²⁾	± 250	V

Notes to Table 1-5:

- (1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is ±1000V.
- (2) This value is applicable only to Cyclone IV GX devices.

Example 1–1 shows how to calculate the change of 50-Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

Example 1–1. Impedance Change

$$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$$

$$\Delta R_T = (85 - 25) \times 0.262 = 15.72$$

Because ΔR_V is negative,

$$MF_V = 1 / (3.83/100 + 1) = 0.963$$

Because ΔR_T is positive,

$$MF_T = 15.72/100 + 1 = 1.157$$

$$MF = 0.963 \times 1.157 = 1.114$$

$$R_{\text{final}} = 50 \times 1.114 = 55.71 \, \Omega$$

Pin Capacitance

Table 1–11 lists the pin capacitance for Cyclone IV devices.

Table 1–11. Pin Capacitance for Cyclone IV Devices ⁽¹⁾

Symbol	Parameter	Typical – Quad Flat Pack (QFP)	Typical – Quad Flat No Leads (QFN)	Typical – Ball-Grid Array (BGA)	Unit
C _{IOTB}	Input capacitance on top and bottom I/O pins	7	7	6	pF
C _{IOLR}	Input capacitance on right I/O pins	7	7	5	pF
C _{LVDSLR}	Input capacitance on right I/O pins with dedicated LVDS output	8	8	7	pF
C _{VREFLR} (2)	Input capacitance on right dual-purpose V _{REF} pin when used as V _{REF} or user I/O pin	21	21	21	pF
C _{VREFTB} (2)	Input capacitance on top and bottom dual-purpose V _{REF} pin when used as V _{REF} or user I/O pin	23 (3)	23	23	pF
C _{CLKTB}	Input capacitance on top and bottom dedicated clock input pins	7	7	6	pF
C _{CLKLR}	Input capacitance on right dedicated clock input pins	6	6	5	pF

Notes to Table 1–11:

- (1) The pin capacitance applies to FBGA, UBGA, and MBGA packages.
- (2) When you use the V_{REF} pin as a regular input or output, you can expect a reduced performance of toggle rate and t_{CO} because of higher pin capacitance.
- (3) C_{VREFTB} for the EP4CE22 device is 30 pF.

Power Consumption

Use the following methods to estimate power for a design:

- the Excel-based EPE
- the Quartus® II PowerPlay power analyzer feature

The interactive Excel-based EPE is used prior to designing the device to get a magnitude estimate of the device power. The Quartus II PowerPlay power analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay power analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, combined with detailed circuit models, can yield very accurate power estimates.



For more information about power estimation tools, refer to the *Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of Cyclone IV core and periphery blocks for commercial grade devices.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The upper-right hand corner of these tables show the designation as “Preliminary”.
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

Table 1-21 lists the Cyclone IV GX transceiver specifications.

Table 1-21. Transceiver Specification for Cyclone IV GX Devices (Part 1 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	1.2 V PCML, 1.5 V PCML, 3.3 V PCML, Differential LVPECL, LVDS, HCSL										
Input frequency from REFCLK input pins	—	50	—	156.25	50	—	156.25	50	—	156.25	MHz
Spread-spectrum modulating clock frequency	Physical interface for PCI Express (PIPE) mode	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PIPE mode	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
Peak-to-peak differential input voltage	—	0.1	—	1.6	0.1	—	1.6	0.1	—	1.6	V
V _{ICM} (AC coupled)	—	1100 ± 5%			1100 ± 5%			1100 ± 5%			mV
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise ⁽¹⁾	Frequency offset = 1 MHz – 8 MHz	—	—	–123	—	—	–123	—	—	–123	dBc/Hz
Transmitter REFCLK Total Jitter ⁽¹⁾		—	—	42.3	—	—	42.3	—	—	42.3	ps
R _{ref}	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clock											
cal_blk_clk clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5/37.5 ⁽²⁾	—	50	2.5/37.5 ⁽²⁾	—	50	2.5/37.5 ⁽²⁾	—	50	MHz
Delta time between reconfig_clk	—	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum power-down pulse width	—	—	1	—	—	1	—	—	1	—	μs

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 2 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										
Data rate (F324 and smaller package) ⁽¹⁵⁾	—	600	—	2500	600	—	2500	600	—	2500	Mbps
Data rate (F484 and larger package) ⁽¹⁵⁾	—	600	—	3125	600	—	3125	600	—	2500	Mbps
Absolute V _{MAX} for a receiver pin ⁽³⁾	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V _{MAX} for a receiver pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V _{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Peak-to-peak differential input voltage V _{ID} (diff p-p)	V _{ICM} = 0.82 V setting, Data Rate = 600 Mbps to 3.125 Gbps	0.1	—	2.7	0.1	—	2.7	0.1	—	2.7	V
V _{ICM}	V _{ICM} = 0.82 V setting	—	820 ± 10%	—	—	820 ± 10%	—	—	820 ± 10%	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	Ω
	150–Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PIPE, Serial Rapid I/O SR, SATA, CPRI LV, SDI, XAUI	Compliant									—
Programmable ppm detector ⁽⁴⁾	—	± 62.5, 100, 125, 200, 250, 300									ppm
Clock data recovery (CDR) ppm tolerance (without spread-spectrum clocking enabled)	—	—	—	±300 ⁽⁵⁾ , ±350 ^{(6), (7)}	—	—	±300 ⁽⁵⁾ , ±350 ^{(6), (7)}	—	—	±300 ⁽⁵⁾ , ±350 ^{(6), (7)}	ppm
CDR ppm tolerance (with synchronous spread-spectrum clocking enabled) ⁽⁸⁾	—	—	—	350 to –5350 ^{(7), (9)}	—	—	350 to –5350 ^{(7), (9)}	—	—	350 to –5350 ^{(7), (9)}	ppm
Run length	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	No Equalization	—	—	1.5	—	—	1.5	—	—	1.5	dB
	Medium Low	—	—	4.5	—	—	4.5	—	—	4.5	dB
	Medium High	—	—	5.5	—	—	5.5	—	—	5.5	dB
	High	—	—	7	—	—	7	—	—	7	dB

Table 1-21. Transceiver Specification for Cyclone IV GX Devices (Part 3 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Signal detect/loss threshold	PIPE mode	65	—	175	65	—	175	65	—	175	mV
t_{LTR} ⁽¹⁰⁾	—	—	—	75	—	—	75	—	—	75	μs
$t_{LTR-LTD_Manual}$ ⁽¹¹⁾	—	15	—	—	15	—	—	15	—	—	μs
t_{LTD} ⁽¹²⁾	—	0	100	4000	0	100	4000	0	100	4000	ns
t_{LTD_Manual} ⁽¹³⁾	—	—	—	4000	—	—	4000	—	—	4000	ns
t_{LTD_Auto} ⁽¹⁴⁾	—	—	—	4000	—	—	4000	—	—	4000	ns
Receiver buffer and CDR offset cancellation time (per channel)	—	—	—	17000	—	—	17000	—	—	17000	recon fig_c lk cycles
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	—	6	—	dB
Transmitter											
Supported I/O Standards	1.5 V PCML										
Data rate (F324 and smaller package)	—	600	—	2500	600	—	2500	600	—	2500	Mbps
Data rate (F484 and larger package)	—	600	—	3125	600	—	3125	600	—	2500	Mbps
V_{OCM}	0.65 V setting	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PIPE, CPRI LV, Serial Rapid I/O SR, SDI, XAUI, SATA	Compliant									—
Rise time	—	50	—	200	50	—	200	50	—	200	ps
Fall time	—	50	—	200	50	—	200	50	—	200	ps
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block skew	—	—	—	120	—	—	120	—	—	120	ps

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 4 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PLD-Transceiver Interface											
Interface speed (F324 and smaller package)	—	25	—	125	25	—	125	25	—	125	MHz
Interface speed (F484 and larger package)	—	25	—	156.25	25	—	156.25	25	—	156.25	MHz
Digital reset pulse width	—	Minimum is 2 parallel clock cycles									

Notes to Table 1–21:

- (1) This specification is valid for transmitter output jitter specification with a maximum total jitter value of 112 ps, typically for 3.125 Gbps SRIO and XAUI protocols.
- (2) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter Only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver Only** or **Receiver and Transmitter** mode.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The rate matcher supports only up to ± 300 parts per million (ppm).
- (5) Supported for the F169 and F324 device packages only.
- (6) Supported for the F484, F672, and F896 device packages only. Pending device characterization.
- (7) To support CDR ppm tolerance greater than ± 300 ppm, implement ppm detector in user logic and configure CDR to Manual Lock Mode.
- (8) Asynchronous spread-spectrum clocking is not supported.
- (9) For the EP4CGX30 (F484 package only), EP4CGX50, and EP4CGX75 devices, the CDR ppl tolerance is ± 200 ppm.
- (10) Time taken until `p11_locked` goes high after `p11_powerdown` deasserts.
- (11) Time that the CDR must be kept in lock-to-reference mode after `rx_analogreset` deasserts and before `rx_locktodata` is asserted in manual mode.
- (12) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode (Figure 1–2), or after `rx_freqlocked` signal goes high in automatic mode (Figure 1–3).
- (13) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode.
- (14) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode.
- (15) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1–23 lists the Cyclone IV GX transceiver block AC specifications.

Table 1–23. Transceiver Block AC Specification for Cyclone IV GX Devices ^{(1), (2)}

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PCIe Transmit Jitter Generation ⁽³⁾											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	—	—	0.25	—	—	0.25	—	—	0.25	UI
PCIe Receiver Jitter Tolerance ⁽³⁾											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	> 0.6			> 0.6			> 0.6			UI
GIGE Transmit Jitter Generation ⁽⁴⁾											
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance ⁽⁴⁾											
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI

Notes to Table 1–23:

- (1) Dedicated `refclk` pins were used to drive the input reference clocks.
- (2) The jitter numbers specified are valid for the stated conditions only.
- (3) The jitter numbers for PIPE are compliant to the PCIe Base Specification 2.0.
- (4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.

Core Performance Specifications

The following sections describe the clock tree specifications, PLLs, embedded multiplier, memory block, and configuration specifications for Cyclone IV Devices.

Clock Tree Specifications

Table 1–24 lists the clock tree specifications for Cyclone IV devices.

Table 1–24. Clock Tree Performance for Cyclone IV Devices (Part 1 of 2)


Device	Performance								Unit
	C6	C7	C8	C8L ⁽¹⁾	C9L ⁽¹⁾	I7	I8L ⁽¹⁾	A7	
EP4CE6	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE10	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE15	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE22	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE30	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE40	500	437.5	402	362	265	437.5	362	402	MHz


Table 1–25. PLL Specifications for Cyclone IV Devices ^{(1), (2)} (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or \overline{areset} is deasserted)	—	—	1	ms
$t_{OUTJITTER_PERIOD_DEDCLK}^{(6)}$	Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER_CCJ_DEDCLK}^{(6)}$	Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER_PERIOD_IO}^{(6)}$	Regular I/O period jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER_CCJ_IO}^{(6)}$	Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	± 50	ps
t_{ARESET}	Minimum pulse width on \overline{areset} signal.	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	3.5 ⁽⁷⁾	—	SCANCLK cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
$t_{CASC_OUTJITTER_PERIOD_DEDCLK}^{(8), (9)}$	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	425	ps
	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz)	—	—	42.5	mUI

Notes to Table 1–25:

- (1) This table is applicable for general purpose PLLs and multipurpose PLLs.
- (2) You must connect V_{CCD_PLL} to V_{CCINT} through the decoupling capacitor and ferrite bead.
- (3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (4) The V_{CO} frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the V_{CO} post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.
- (6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.
- (7) With 100-MHz scanclk frequency.
- (8) The cascaded PLLs specification is applicable only with the following conditions:
 - Upstream PLL— $0.59 \text{ MHz} \leq \text{Upstream PLL bandwidth} < 1 \text{ MHz}$
 - Downstream PLL—Downstream PLL bandwidth $> 2 \text{ MHz}$
- (9) PLL cascading is not supported for transceiver applications.

 For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interfaces Handbook*.

 Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 1–31 through Table 1–36 list the high-speed I/O timing for Cyclone IV devices. For definitions of high-speed timing specifications, refer to “Glossary” on page 1–37.

Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices ⁽¹⁾, ⁽²⁾, ⁽⁴⁾ (Part 1 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×8	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×7	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×4	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×2	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×1	5	—	360	5	—	311	5	—	311	5	—	311	5	—	265	MHz
Device operation in Mbps	×10	100	—	360	100	—	311	100	—	311	100	—	311	100	—	265	Mbps
	×8	80	—	360	80	—	311	80	—	311	80	—	311	80	—	265	Mbps
	×7	70	—	360	70	—	311	70	—	311	70	—	311	70	—	265	Mbps
	×4	40	—	360	40	—	311	40	—	311	40	—	311	40	—	265	Mbps
	×2	20	—	360	20	—	311	20	—	311	20	—	311	20	—	265	Mbps
	×1	10	—	360	10	—	311	10	—	311	10	—	311	10	—	265	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
Transmitter channel-to-channel skew (TCCS)	—	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	—	—	700	ps
t_{RISE}	20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps

Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 2 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{LOCK} ⁽²⁾	—	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–32:

- (1) Emulated RSDS_E_1R transmitter is supported at the output pin of all I/O Banks of Cyclone IV E devices and I/O Banks 3, 4, 5, 6, 7, 8, and 9 of Cyclone IV GX devices.
- (2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–33. Mini-LVDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (2), (4)}

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×8	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×7	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×4	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×2	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×1	5	—	400	5	—	311	5	—	311	5	—	311	5	—	265	MHz
Device operation in Mbps	×10	100	—	400	100	—	311	100	—	311	100	—	311	100	—	265	Mbps
	×8	80	—	400	80	—	311	80	—	311	80	—	311	80	—	265	Mbps
	×7	70	—	400	70	—	311	70	—	311	70	—	311	70	—	265	Mbps
	×4	40	—	400	40	—	311	40	—	311	40	—	311	40	—	265	Mbps
	×2	20	—	400	20	—	311	20	—	311	20	—	311	20	—	265	Mbps
	×1	10	—	400	10	—	311	10	—	311	10	—	311	10	—	265	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	—	—	700	ps
t_{RISE}	20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{LOCK} ⁽³⁾	—	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–33:

- (1) Applicable for true and emulated mini-LVDS transmitter.
- (2) Cyclone IV E—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated mini-LVDS transmitter is supported at the output pin of all I/O banks.
Cyclone IV GX—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (3) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–34. True LVDS Transmitter Timing Specifications for Cyclone IV Devices ⁽¹⁾, ⁽³⁾

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{HCLK} (input clock frequency)	×10	5	420	5	370	5	320	5	320	5	250	MHz
	×8	5	420	5	370	5	320	5	320	5	250	MHz
	×7	5	420	5	370	5	320	5	320	5	250	MHz
	×4	5	420	5	370	5	320	5	320	5	250	MHz
	×2	5	420	5	370	5	320	5	320	5	250	MHz
	×1	5	420	5	402.5	5	402.5	5	362	5	265	MHz
HSIODR	×10	100	840	100	740	100	640	100	640	100	500	Mbps
	×8	80	840	80	740	80	640	80	640	80	500	Mbps
	×7	70	840	70	740	70	640	70	640	70	500	Mbps
	×4	40	840	40	740	40	640	40	640	40	500	Mbps
	×2	20	840	20	740	20	640	20	640	20	500	Mbps
	×1	10	420	10	402.5	10	402.5	10	362	10	265	Mbps
t_{DUTY}	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	—	600	—	700	ps
t_{LOCK} ⁽²⁾	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1–34:

- (1) Cyclone IV E—true LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6.
Cyclone IV GX—true LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6.
- (2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices ⁽¹⁾, ⁽³⁾ (Part 1 of 2)

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{HCLK} (input clock frequency)	×10	5	320	5	320	5	275	5	275	5	250	MHz
	×8	5	320	5	320	5	275	5	275	5	250	MHz
	×7	5	320	5	320	5	275	5	275	5	250	MHz
	×4	5	320	5	320	5	275	5	275	5	250	MHz
	×2	5	320	5	320	5	275	5	275	5	250	MHz
	×1	5	402.5	5	402.5	5	402.5	5	362	5	265	MHz
HSIODR	×10	100	640	100	640	100	550	100	550	100	500	Mbps
	×8	80	640	80	640	80	550	80	550	80	500	Mbps
	×7	70	640	70	640	70	550	70	550	70	500	Mbps
	×4	40	640	40	640	40	550	40	550	40	500	Mbps
	×2	20	640	20	640	20	550	20	550	20	500	Mbps
	×1	10	402.5	10	402.5	10	402.5	10	362	10	265	Mbps

Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 2 of 2)

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{DUTY}	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	—	600	—	700	ps
t _{LOCK} ⁽²⁾	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1–35:

- (1) Cyclone IV E—emulated LVDS transmitter is supported at the output pin of all I/O Banks.
Cyclone IV GX—emulated LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–36. LVDS Receiver Timing Specifications for Cyclone IV Devices ^{(1), (3)}

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f _{HCLK} (input clock frequency)	×10	10	437.5	10	370	10	320	10	320	10	250	MHz
	×8	10	437.5	10	370	10	320	10	320	10	250	MHz
	×7	10	437.5	10	370	10	320	10	320	10	250	MHz
	×4	10	437.5	10	370	10	320	10	320	10	250	MHz
	×2	10	437.5	10	370	10	320	10	320	10	250	MHz
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	MHz
HSIODR	×10	100	875	100	740	100	640	100	640	100	500	Mbps
	×8	80	875	80	740	80	640	80	640	80	500	Mbps
	×7	70	875	70	740	70	640	70	640	70	500	Mbps
	×4	40	875	40	740	40	640	40	640	40	500	Mbps
	×2	20	875	20	740	20	640	20	640	20	500	Mbps
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	Mbps
SW	—	—	400	—	400	—	400	—	550	—	640	ps
Input jitter tolerance	—	—	500	—	500	—	550	—	600	—	700	ps
t _{LOCK} ⁽²⁾	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1–36:

- (1) Cyclone IV E—LVDS receiver is supported at all I/O Banks.
Cyclone IV GX—LVDS receiver is supported at I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

External Memory Interface Specifications

The external memory interfaces for Cyclone IV devices are auto-calibrating and easy to implement.

For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interface Handbook*.

Table 1–37 lists the memory output clock jitter specifications for Cyclone IV devices.

Table 1–37. Memory Output Clock Jitter Specifications for Cyclone IV Devices ^{(1), (2)}

Parameter	Symbol	Min	Max	Unit
Clock period jitter	$t_{JIT(per)}$	–125	125	ps
Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–200	200	ps
Duty cycle jitter	$t_{JIT(duty)}$	–150	150	ps

Notes to Table 1–37:

- (1) Memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2 standard.
- (2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock (GCLK) network.

Duty Cycle Distortion Specifications

Table 1–38 lists the worst case duty cycle distortion for Cyclone IV devices.

Table 1–38. Duty Cycle Distortion on Cyclone IV Devices I/O Pins ^{(1), (2), (3)}

Symbol	C6		C7, I7		C8, I8L, A7		C9L		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Notes to Table 1–38:

- (1) The duty cycle distortion specification applies to clock outputs from the PLLs, global clock tree, and IOE driving the dedicated and general purpose I/O pins.
- (2) Cyclone IV devices meet the specified duty cycle distortion at the maximum output toggle rate for each combination of I/O standard and current strength.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

OCT Calibration Timing Specification

Table 1–39 lists the duration of calibration for series OCT with calibration at device power-up for Cyclone IV devices.

Table 1–39. Timing Specification for Series OCT with Calibration at Device Power-Up for Cyclone IV Devices ⁽¹⁾

Symbol	Description	Maximum	Units
t_{OCTCAL}	Duration of series OCT with calibration at device power-up	20	μs

Note to Table 1–39:

- (1) OCT calibration takes place after device configuration and before entering user mode.

I/O Timing

Use the following methods to determine I/O timing:

- the Excel-based I/O Timing
- the Quartus II timing analyzer

The Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get a timing budget estimation as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.



The Excel-based I/O Timing spreadsheet is downloadable from Cyclone IV Devices Literature website.

Glossary

Table 1–46 lists the glossary for this chapter.

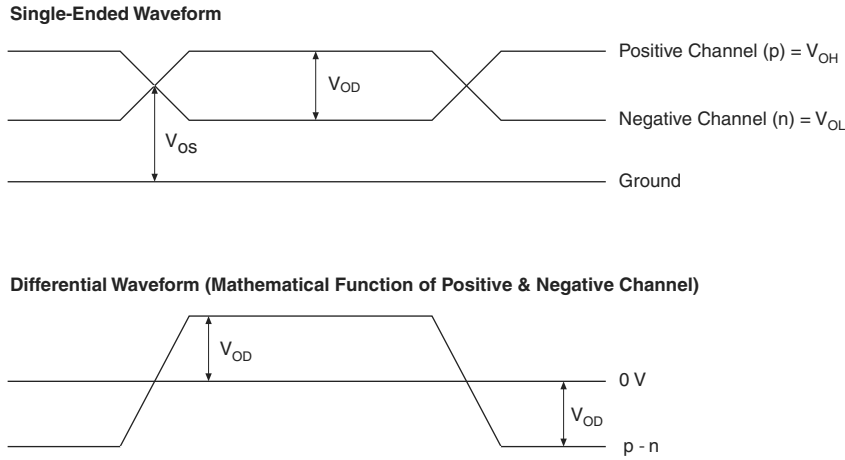
Table 1–46. Glossary (Part 1 of 5)

Letter	Term	Definitions
A	—	—
B	—	—
C	—	—
D	—	—
E	—	—
F	f_{HSCLK}	High-speed I/O block: High-speed receiver/transmitter input and output clock frequency.
G	GCLK	Input pin directly to Global Clock network.
	GCLK PLL	Input pin to Global Clock network through the PLL.
H	HSIODR	High-speed I/O block: Maximum/minimum LVDS data transfer rate ($\text{HSIODR} = 1/\text{TUI}$).
I	Input Waveforms for the SSTL Differential I/O Standard	

Table 1-46. Glossary (Part 2 of 5)

Letter	Term	Definitions
J	JTAG Waveform	<p>The diagram illustrates the JTAG waveform with the following timing parameters:</p> <ul style="list-style-type: none"> t_{JCP}: Time from TCK rising edge to TDI setup. t_{JCH}: Time from TCK rising edge to TDI hold. t_{JCL}: Time from TCK falling edge to TDI setup. t_{JPSU_TDI}: Time from TCK rising edge to TDI setup. t_{JPSU_TMS}: Time from TCK rising edge to TMS setup. t_{JPH}: Time from TCK rising edge to TDI hold. t_{JPZX}: Time from TCK rising edge to TDO setup. t_{JPCO}: Time from TCK rising edge to TDO setup. t_{JPXZ}: Time from TCK rising edge to TDO hold. t_{JSSU}: Time from TCK rising edge to TDO setup. t_{JSH}: Time from TCK rising edge to TDO hold. t_{JSZX}: Time from TCK rising edge to TDO setup. t_{JSCO}: Time from TCK rising edge to TDO setup. t_{JSXZ}: Time from TCK rising edge to TDO hold.
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	PLL Block	<p>The following highlights the PLL specification parameters:</p> <p>Key:</p> <ul style="list-style-type: none"> Reconfigurable in User Mode
Q	—	—

Table 1-46. Glossary (Part 4 of 5)

Letter	Term	Definitions
T	t_C	High-speed receiver and transmitter input and output clock period.
	Channel-to-channel-skew (TCCS)	High-speed I/O block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
	t_{cin}	Delay from the clock pad to the I/O input register.
	t_{CO}	Delay from the clock pad to the I/O output.
	t_{cout}	Delay from the clock pad to the I/O output register.
	t_{DUTY}	High-speed I/O block: Duty cycle on high-speed transmitter output clock.
	t_{FALL}	Signal high-to-low transition time (80–20%).
	t_H	Input register hold time.
	Timing Unit Interval (TUI)	High-speed I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency Multiplication Factor}) = t_C/w$).
	$t_{INJITTER}$	Period jitter on the PLL clock input.
	$t_{OUTJITTER_DEDCLK}$	Period jitter on the dedicated clock output driven by a PLL.
	$t_{OUTJITTER_IO}$	Period jitter on the general purpose I/O driven by a PLL.
	t_{pllcin}	Delay from the PLL inclk pad to the I/O input register.
	$t_{pllcout}$	Delay from the PLL inclk pad to the I/O output register.
	Transmitter Output Waveform	<p>Transmitter output waveforms for the LVDS, mini-LVDS, PPDS and RSDS Differential I/O Standards:</p> 
	t_{RISE}	Signal low-to-high transition time (20–80%).
	t_{SU}	Input register setup time.
U	—	—

Document Revision History

Table 1–47 lists the revision history for this chapter.

Table 1–47. Document Revision History

Date	Version	Changes
March 2016	2.0	Updated note (5) in Table 1–21 to remove support for the N148 package.
October 2014	1.9	Updated maximum value for V_{CCD_PLL} in Table 1–1. Removed extended temperature note in Table 1–3.
December 2013	1.8	Updated Table 1–21 by adding Note (15).
May 2013	1.7	Updated Table 1–15 by adding Note (4).
October 2012	1.6	<ul style="list-style-type: none"> ■ Updated the maximum value for V_I, V_{CCD_PLL}, V_{CCIO}, V_{CC_CLKIN}, V_{CCH_GXB}, and V_{CCA_GXB} in Table 1–1. ■ Updated Table 1–11 and Table 1–22. ■ Updated Table 1–21 to include peak-to-peak differential input voltage for the Cyclone IV GX transceiver input reference clock. ■ Updated Table 1–29 to include the typical $DCLK$ value. ■ Updated the minimum f_{HSCLK} value in Table 1–31, Table 1–32, Table 1–33, Table 1–34, and Table 1–35.
November 2011	1.5	<ul style="list-style-type: none"> ■ Updated “Maximum Allowed Overshoot or Undershoot Voltage”, “Operating Conditions”, and “PLL Specifications” sections. ■ Updated Table 1–2, Table 1–3, Table 1–4, Table 1–5, Table 1–8, Table 1–9, Table 1–15, Table 1–18, Table 1–19, and Table 1–21. ■ Updated Figure 1–1.
December 2010	1.4	<ul style="list-style-type: none"> ■ Updated for the Quartus II software version 10.1 release. ■ Updated Table 1–21 and Table 1–25. ■ Minor text edits.
July 2010	1.3	<p>Updated for the Quartus II software version 10.0 release:</p> <ul style="list-style-type: none"> ■ Updated Table 1–3, Table 1–4, Table 1–21, Table 1–25, Table 1–28, Table 1–30, Table 1–40, Table 1–41, Table 1–42, Table 1–43, Table 1–44, and Table 1–45. ■ Updated Figure 1–2 and Figure 1–3. ■ Removed SW Requirement and TCCS for Cyclone IV Devices tables. ■ Minor text edits.
March 2010	1.2	<p>Updated to include automotive devices:</p> <ul style="list-style-type: none"> ■ Updated the “Operating Conditions” and “PLL Specifications” sections. ■ Updated Table 1–1, Table 1–8, Table 1–9, Table 1–21, Table 1–26, Table 1–27, Table 1–31, Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–36, Table 1–37, Table 1–38, Table 1–40, Table 1–42, and Table 1–43. ■ Added Table 1–5 to include ESD for Cyclone IV devices GPIOs and HSSI I/Os. ■ Added Table 1–44 and Table 1–45 to include IOE programmable delay for Cyclone IV E 1.2 V core voltage devices. ■ Minor text edits.

Table 1–47. Document Revision History

Date	Version	Changes
February 2010	1.1	<ul style="list-style-type: none">■ Updated Table 1–3 through Table 1–44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release.■ Minor text edits.
November 2009	1.0	Initial release.