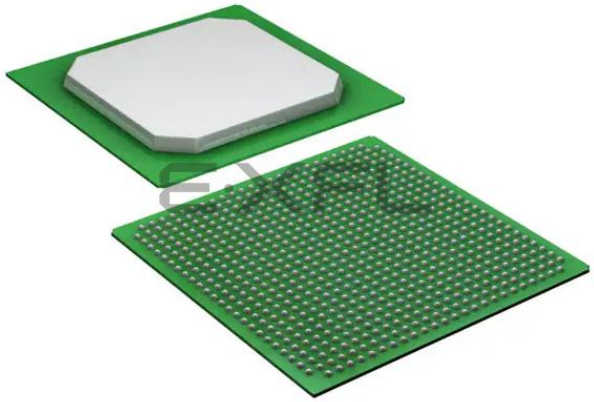

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 9360 |
| Number of Logic Elements/Cells | 149760 |
| Total RAM Bits | 6635520 |
| Number of I/O | 393 |
| Number of Gates | - |
| Voltage - Supply | 1.16V ~ 1.24V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BGA |
| Supplier Device Package | 672-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep4cgx150df27c7n |

Cyclone IV E industrial devices I7 are offered with extended operating temperature range.

## Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone IV devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Table 1–1 lists the absolute maximum ratings for Cyclone IV devices.

CAUTION

Conditions beyond those listed in Table 1–1 cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time have adverse effects on the device.

**Table 1–1. Absolute Maximum Ratings for Cyclone IV Devices** *(1)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CCINT}$ | Core voltage, PCI Express® (PCIe®) hard IP block, and transceiver physical coding sublayer (PCS) power supply | –0.5 | 1.8 | V |
| $V_{CCA}$ | Phase-locked loop (PLL) analog power supply | –0.5 | 3.75 | V |
| $V_{CCD\_PLL}$ | PLL digital power supply | –0.5 | 1.8 | V |
| $V_{CCIO}$ | I/O banks power supply | –0.5 | 3.75 | V |
| $V_{CC\_CLKIN}$ | Differential clock input pins power supply | –0.5 | 4.5 | V |
| $V_{CCH\_GXB}$ | Transceiver output buffer power supply | –0.5 | 3.75 | V |
| $V_{CCA\_GXB}$ | Transceiver physical medium attachment (PMA) and auxiliary power supply | –0.5 | 3.75 | V |
| $V_{CCL\_GXB}$ | Transceiver PMA and auxiliary power supply | –0.5 | 1.8 | V |
| $V_I$ | DC input voltage | –0.5 | 4.2 | V |
| $I_{OUT}$ | DC output current, per pin | –25 | 40 | mA |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C |
| $T_J$ | Operating junction temperature | –40 | 125 | °C |

**Note to Table 1–1:**

(1) Supply voltage specifications apply to voltage readings taken at the device pins with respect to ground, not at the power supply.

### Maximum Allowed Overshoot or Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to –2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns. Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device.

# DC Characteristics

This section lists the I/O leakage current, pin capacitance, on-chip termination (OCT) tolerance, and bus hold specifications for Cyclone IV devices.

## Supply Current

The device supply current requirement is the minimum current drawn from the power supply pins that can be used as a reference for power size planning. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary greatly with the resources used. Table 1–6 lists the I/O pin leakage current for Cyclone IV devices.

**Table 1–6. I/O Pin Leakage Current for Cyclone IV Devices** *(1), (2)*

| Symbol | Parameter | Conditions | Device | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current | $V_I$ = 0 V to $V_{CCIOMAX}$ | — | –10 | — | 10 | µA |
| $I_{OZ}$ | Tristated I/O pin leakage current | $V_O$ = 0 V to $V_{CCIOMAX}$ | — | –10 | — | 10 | µA |

**Notes to Table 1–6:**

(1) This value is specified for normal device operation. The value varies during device power-up. This applies for all $V_{CCIO}$ settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) The 10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

## Bus Hold

The bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1–7 lists bus hold specifications for Cyclone IV devices.

**Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 1 of 2)** *(1)*

| Parameter | Condition | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus hold low, sustaining current | $V_{IN} > V_{IL}$ (maximum) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | µA |
| Bus hold high, sustaining current | $V_{IN} < V_{IL}$ (minimum) | –8 | — | –12 | — | –30 | — | –50 | — | –70 | — | –70 | — | µA |
| Bus hold low, overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | µA |
| Bus hold high, overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | –125 | — | –175 | — | –200 | — | –300 | — | –500 | — | –500 | µA |

### Schmitt Trigger Input

Cyclone IV devices support Schmitt trigger input on the TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rate. Table 1–14 lists the hysteresis specifications across the supported $V_{CCIO}$ range for Schmitt trigger inputs in Cyclone IV devices.

**Table 1–14. Hysteresis Specifications for Schmitt Trigger Input in Cyclone IV Devices**

| Symbol | Parameter | Conditions (V) | Minimum | Unit |
|---|---|---|---|---|
| $V_{SCHMITT}$ | Hysteresis for Schmitt trigger input | $V_{CCIO}$ = 3.3 | 200 | mV |
| | | $V_{CCIO}$ = 2.5 | 200 | mV |
| | | $V_{CCIO}$ = 1.8 | 140 | mV |
| | | $V_{CCIO}$ = 1.5 | 110 | mV |

## I/O Standard Specifications

The following tables list input voltage sensitivities ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$), for various I/O standards supported by Cyclone IV devices. Table 1–15 through Table 1–20 provide the I/O standard specifications for Cyclone IV devices.

**Table 1–15. Single-Ended I/O Standard Specifications for Cyclone IV Devices (1), (2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) (4) | $I_{OH}$ (mA) (4) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 3.3-V LVTTL (3) | 3.135 | 3.3 | 3.465 | — | 0.8 | 1.7 | 3.6 | 0.45 | 2.4 | 4 | –4 |
| 3.3-V LVCMOS (3) | 3.135 | 3.3 | 3.465 | — | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 2 | –2 |
| 3.0-V LVTTL (3) | 2.85 | 3.0 | 3.15 | –0.3 | 0.8 | 1.7 | $V_{CCIO}$ + 0.3 | 0.45 | 2.4 | 4 | –4 |
| 3.0-V LVCMOS (3) | 2.85 | 3.0 | 3.15 | –0.3 | 0.8 | 1.7 | $V_{CCIO}$ + 0.3 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 2.5 V (3) | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | $V_{CCIO}$ + 0.3 | 0.4 | 2.0 | 1 | –1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 x $V_{CCIO}$ | 0.65 x $V_{CCIO}$ | 2.25 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 x $V_{CCIO}$ | 0.65 x $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 x $V_{CCIO}$ | 0.75 x $V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 x $V_{CCIO}$ | 0.65 x $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 x $V_{CCIO}$ | 0.75 x $V_{CCIO}$ | 2 | –2 |
| 3.0-V PCI | 2.85 | 3.0 | 3.15 | — | 0.3 x $V_{CCIO}$ | 0.5 x $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.1 x $V_{CCIO}$ | 0.9 x $V_{CCIO}$ | 1.5 | –0.5 |
| 3.0-V PCI-X | 2.85 | 3.0 | 3.15 | — | 0.35 x $V_{CCIO}$ | 0.5 x $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.1 x $V_{CCIO}$ | 0.9 x $V_{CCIO}$ | 1.5 | –0.5 |

**Notes to Table 1–15:**

(1) For voltage-referenced receiver input waveform and explanation of terms used in Table 1–15, refer to "Glossary" on page 1–37.

(2) AC load CL = 10 pF

(3) For more information about interfacing Cyclone IV devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards, refer to *AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*.

(4) To meet the $I_{OL}$ and $I_{OH}$ specifications, you must set the current strength settings accordingly. For example, to meet the **3.3-V LVTTL** specification (4 mA), set the current strength settings to 4 mA or higher. Setting at lower current strength may not meet the $I_{OL}$ and $I_{OH}$ specifications in the handbook.

**Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices (1) (Part 2 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV) | | $V_{ICM}$ (V) (2) | | | $V_{OD}$ (mV) (3) | | | $V_{OS}$ (V) (3) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| LVDS (Column I/Os) | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX} \leq$ 500 Mbps | 1.80 | 247 | — | 600 | 1.125 | 1.25 | 1.375 |
| | | | | | | 0.55 | 500 Mbps $\leq D_{MAX} \leq$ 700 Mbps | 1.80 | | | | | | |
| | | | | | | 1.05 | $D_{MAX}$ > 700 Mbps | 1.55 | | | | | | |
| BLVDS (Row I/Os) (4) | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — |
| BLVDS (Column I/Os) (4) | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — |
| mini-LVDS (Row I/Os) (5) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 300 | — | 600 | 1.0 | 1.2 | 1.4 |
| mini-LVDS (Column I/Os) (5) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 300 | — | 600 | 1.0 | 1.2 | 1.4 |
| RSDS® (Row I/Os) (5) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.5 |
| RSDS (Column I/Os) (5) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.5 |
| PPDS (Row I/Os) (5) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.4 |
| PPDS (Column I/Os) (5) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.4 |

**Notes to Table 1–20:**

(1) For an explanation of terms used in Table 1–20, refer to "Glossary" on page 1–37.

(2) $V_{IN}$ range: 0 V $\leq V_{IN} \leq$ 1.85 V.

(3) $R_L$ range: 90 $\leq R_L \leq$ 110 Ω.

(4) There are no fixed $V_{IN}$, $V_{OD}$, and $V_{OS}$ specifications for BLVDS. They depend on the system topology.

(5) The Mini-LVDS, RSDS, and PPDS standards are only supported at the output pins.

(6) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported for output pins.

## Transceiver Performance Specifications

Table 1–21 lists the Cyclone IV GX transceiver specifications.

**Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 1 of 4)**

| Symbol/ Description | Conditions | C6 | | | C7, I7 | | | C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Reference Clock** | | | | | | | | | | | |
| Supported I/O Standards | 1.2 V PCML, 1.5 V PCML, 3.3 V PCML, Differential LVPECL, LVDS, HCSL | | | | | | | | | | |
| Input frequency from REFCLK input pins | — | 50 | — | 156.25 | 50 | — | 156.25 | 50 | — | 156.25 | MHz |
| Spread-spectrum modulating clock frequency | Physical interface for PCI Express (PIPE) mode | 30 | — | 33 | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PIPE mode | — | 0 to –0.5% | — | — | 0 to –0.5% | — | — | 0 to –0.5% | — | — |
| Peak-to-peak differential input voltage | — | 0.1 | — | 1.6 | 0.1 | — | 1.6 | 0.1 | — | 1.6 | V |
| $V_{ICM}$ (AC coupled) | — | 1100 ± 5% | | | 1100 ± 5% | | | 1100 ± 5% | | | mV |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise *(1)* | Frequency offset = 1 MHz – 8 MHZ | — | — | –123 | — | — | –123 | — | — | –123 | dBc/Hz |
| Transmitter REFCLK Total Jitter *(1)* | | — | — | 42.3 | — | — | 42.3 | — | — | 42.3 | ps |
| $R_{ref}$ | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | Ω |
| **Transceiver Clock** | | | | | | | | | | | |
| cal_blk_clk clock frequency | — | 10 | — | 125 | 10 | — | 125 | 10 | — | 125 | MHz |
| fixedclk clock frequency | PCIe Receiver Detect | — | 125 | — | — | 125 | — | — | 125 | — | MHz |
| reconfig_clk clock frequency | Dynamic reconfiguration clock frequency | 2.5/ 37.5 *(2)* | — | 50 | 2.5/ 37.5 *(2)* | — | 50 | 2.5/ 37.5 *(2)* | — | 50 | MHz |
| Delta time between reconfig_clk | — | — | — | 2 | — | — | 2 | — | — | 2 | ms |
| Transceiver block minimum power-down pulse width | — | — | 1 | — | — | 1 | — | — | 1 | — | µs |

Figure 1–2 shows the lock time parameters in manual mode.

LTD = lock-to-data. LTR = lock-to-reference.

**Figure 1–2. Lock Time Parameters for Manual Mode**

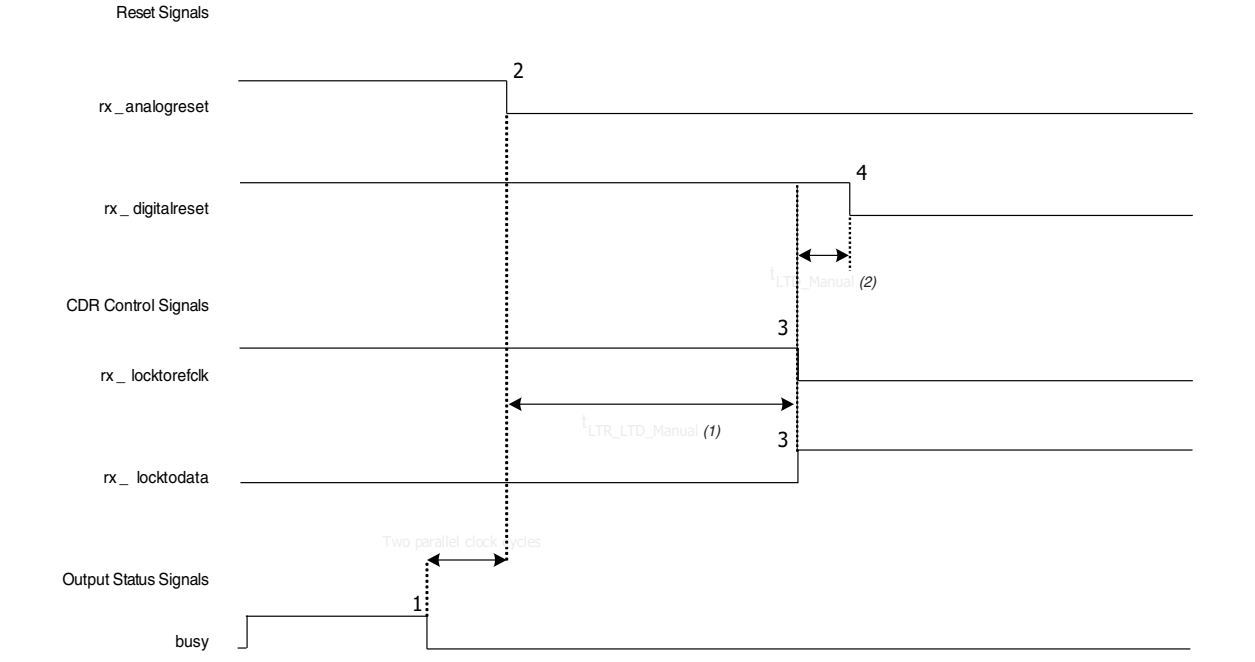



Figure 1–3 shows the lock time parameters in automatic mode.

**Figure 1–3. Lock Time Parameters for Automatic Mode**

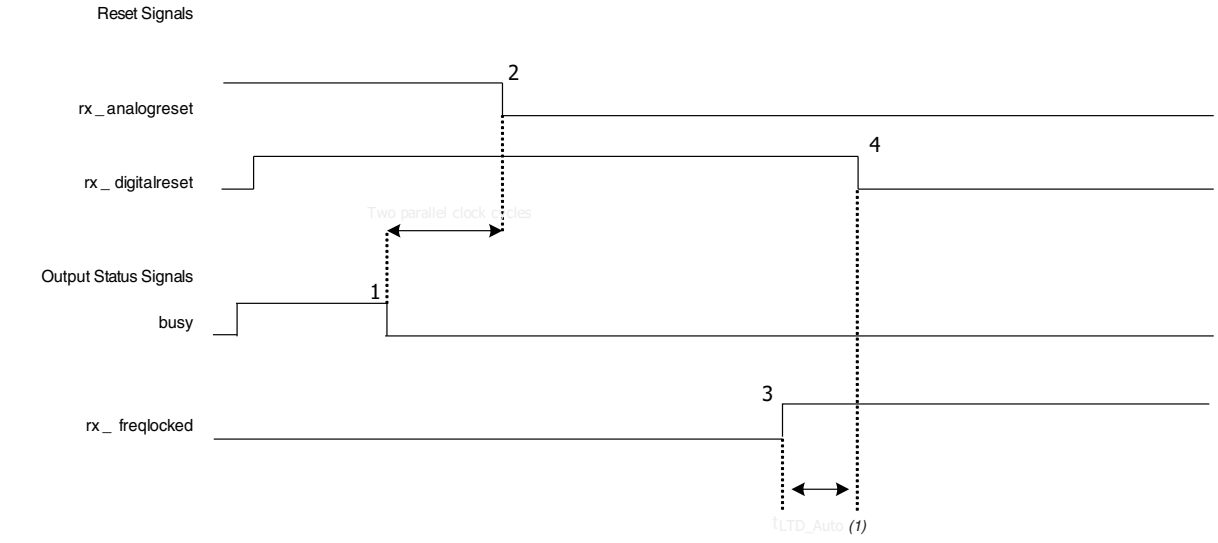


**Table 1–25. PLL Specifications for Cyclone IV Devices (1), (2) (Part 2 of 2)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or areset is deasserted) | — | — | 1 | ms |
| $t_{OUTJITTER\_PERIOD\_DEDCLK}$ (6) | Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz | — | — | 300 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 30 | mUI |
| $t_{OUTJITTER\_CCJ\_DEDCLK}$ (6) | Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz | — | — | 300 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 30 | mUI |
| $t_{OUTJITTER\_PERIOD\_IO}$ (6) | Regular I/O period jitter $F_{OUT} \geq 100$ MHz | — | — | 650 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 75 | mUI |
| $t_{OUTJITTER\_CCJ\_IO}$ (6) | Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz | — | — | 650 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 75 | mUI |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on areset signal. | 10 | — | — | ns |
| $t_{CONFIGPLL}$ | Time required to reconfigure scan chains for PLLs | — | 3.5 (7) | — | SCANCLK cycles |
| $f_{SCANCLK}$ | scanclk frequency | — | — | 100 | MHz |
| $t_{CASC\_OUTJITTER\_PERIOD\_DEDCLK}$ (8), (9) | Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz) | — | — | 425 | ps |
| | Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz) | — | — | 42.5 | mUI |

**Notes to Table 1–25:**

(1) This table is applicable for general purpose PLLs and multipurpose PLLs.

(2) You must connect $V_{CCD\_PLL}$ to $V_{CCINT}$ through the decoupling capacitor and ferrite bead.

(3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(4) The $V_{CO}$ frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the $V_{CO}$ post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.

(6) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.

(7) With 100-MHz scanclk frequency.

(8) The cascaded PLLs specification is applicable only with the following conditions:

- Upstream PLL—0.59 MHz ≤ Upstream PLL bandwidth < 1 MHz
- Downstream PLL—Downstream PLL bandwidth > 2 MHz

(9) PLL cascading is not supported for transceiver applications.

## Embedded Multiplier Specifications

Table 1–26 lists the embedded multiplier specifications for Cyclone IV devices.

**Table 1–26. Embedded Multiplier Specifications for Cyclone IV Devices**

| Mode | Resources Used | Performance | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | Number of Multipliers | C6 | C7, I7, A7 | C8 | C8L, I8L | C9L | |
| 9 × 9-bit multiplier | 1 | 340 | 300 | 260 | 240 | 175 | MHz |
| 18 × 18-bit multiplier | 1 | 287 | 250 | 200 | 185 | 135 | MHz |

## Memory Block Specifications

Table 1–27 lists the M9K memory block specifications for Cyclone IV devices.

**Table 1–27. Memory Block Performance Specifications for Cyclone IV Devices**

| Memory | Mode | Resources Used | | Performance | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | LEs | M9K Memory | C6 | C7, I7, A7 | C8 | C8L, I8L | C9L | |
| M9K Block | FIFO 256 × 36 | 47 | 1 | 315 | 274 | 238 | 200 | 157 | MHz |
| | Single-port 256 × 36 | 0 | 1 | 315 | 274 | 238 | 200 | 157 | MHz |
| | Simple dual-port 256 × 36 CLK | 0 | 1 | 315 | 274 | 238 | 200 | 157 | MHz |
| | True dual port 512 × 18 single CLK | 0 | 1 | 315 | 274 | 238 | 200 | 157 | MHz |

## Configuration and JTAG Specifications

Table 1–28 lists the configuration mode specifications for Cyclone IV devices.

**Table 1–28. Passive Configuration Mode Specifications for Cyclone IV Devices (1)**

| Programming Mode | $V_{CCINT}$ Voltage Level (V) | DCLK $f_{MAX}$ | Unit |
|---|---|---|---|
| Passive Serial (PS) | 1.0 (3) | 66 | MHz |
| | 1.2 | 133 | MHz |
| Fast Passive Parallel (FPP) (2) | 1.0 (3) | 66 | MHz |
| | 1.2 (4) | 100 | MHz |

**Notes to Table 1–28:**

(1) For more information about PS and FPP configuration timing parameters, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter.

(2) FPP configuration mode supports all Cyclone IV E devices (except for E144 package devices) and EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 only.

(3) $V_{CCINT}$ = 1.0 V is only supported for Cyclone IV E 1.0 V core voltage devices.

(4) Cyclone IV E devices support 1.2 V $V_{CCINT}$. Cyclone IV E 1.2 V core voltage devices support 133 MHz DCLK $f_{MAX}$ for EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, and EP4CE40 only.

Table 1–29 lists the active configuration mode specifications for Cyclone IV devices.

**Table 1–29. Active Configuration Mode Specifications for Cyclone IV Devices**

| Programming Mode | DCLK Range | Typical DCLK | Unit |
|---|---|---|---|
| Active Parallel (AP) *(1)* | 20 to 40 | 33 | MHz |
| Active Serial (AS) | 20 to 40 | 33 | MHz |

**Note to Table 1–29:**

(1) AP configuration mode is only supported for Cyclone IV E devices.

Table 1–30 lists the JTAG timing parameters and values for Cyclone IV devices.

**Table 1–30. JTAG Timing Parameters for Cyclone IV Devices *(1)***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 40 | — | ns |
| $t_{JCH}$ | TCK clock high time | 19 | — | ns |
| $t_{JCL}$ | TCK clock low time | 19 | — | ns |
| $t_{JPSU\_TDI}$ | JTAG port setup time for TDI | 1 | — | ns |
| $t_{JPSU\_TMS}$ | JTAG port setup time for TMS | 3 | — | ns |
| $t_{JPH}$ | JTAG port hold time | 10 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output *(2), (3)* | — | 15 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output *(2), (3)* | — | 15 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance *(2), (3)* | — | 15 | ns |
| $t_{JSSU}$ | Capture register setup time | 5 | — | ns |
| $t_{JSH}$ | Capture register hold time | 10 | — | ns |
| $t_{JSCO}$ | Update register clock to output | — | 25 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | — | 25 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | — | 25 | ns |

**Notes to Table 1–30:**

(1) For more information about JTAG waveforms, refer to "JTAG Waveform" in "Glossary" on page 1–37.

(2) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 16 ns.

(3) For EP4CGX22, EP4CGX30 (F324 and smaller package), EP4CGX110, and EP4CGX150 devices, the output time specification for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins is 16 ns. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 18 ns.

## Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/Os using the SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speeds. I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-LVTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.

**Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4) (Part 2 of 2)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{LOCK}$ (3) | — | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | ms |

**Notes to Table 1–31:**

(1) Applicable for true RSDS and emulated RSDS_E_3R transmitter.

(2) Cyclone IV E devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated RSDS transmitter is supported at the output pin of all I/O Banks.
Cyclone IV GX devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(3) $t_{LOCK}$ is the time required for the PLL to lock from the end-of-device configuration.

(4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

**Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 1 of 2)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 72.5 | MHz |
| | ×8 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 72.5 | MHz |
| | ×7 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 72.5 | MHz |
| | ×4 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 72.5 | MHz |
| | ×2 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 72.5 | MHz |
| | ×1 | 5 | — | 170 | 5 | — | 170 | 5 | — | 170 | 5 | — | 170 | 5 | — | 145 | MHz |
| Device operation in Mbps | ×10 | 100 | — | 170 | 100 | — | 170 | 100 | — | 170 | 100 | — | 170 | 100 | — | 145 | Mbps |
| | ×8 | 80 | — | 170 | 80 | — | 170 | 80 | — | 170 | 80 | — | 170 | 80 | — | 145 | Mbps |
| | ×7 | 70 | — | 170 | 70 | — | 170 | 70 | — | 170 | 70 | — | 170 | 70 | — | 145 | Mbps |
| | ×4 | 40 | — | 170 | 40 | — | 170 | 40 | — | 170 | 40 | — | 170 | 40 | — | 145 | Mbps |
| | ×2 | 20 | — | 170 | 20 | — | 170 | 20 | — | 170 | 20 | — | 170 | 20 | — | 145 | Mbps |
| | ×1 | 10 | — | 170 | 10 | — | 170 | 10 | — | 170 | 10 | — | 170 | 10 | — | 145 | Mbps |
| $t_{DUTY}$ | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS | — | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 550 | — | — | 600 | — | — | 700 | ps |
| $t_{RISE}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |

**Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 2 of 2)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{LOCK}$ (2) | — | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | ms |

**Notes to Table 1–32:**

(1) Emulated RSDS_E_1R transmitter is supported at the output pin of all I/O Banks of Cyclone IV E devices and I/O Banks 3, 4, 5, 6, 7, 8, and 9 of Cyclone IV GX devices.

(2) $t_{LOCK}$ is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

**Table 1–33. Mini-LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×8 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×7 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×4 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×2 | 5 | — | 200 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×1 | 5 | — | 400 | 5 | — | 311 | 5 | — | 311 | 5 | — | 311 | 5 | — | 265 | MHz |
| Device operation in Mbps | ×10 | 100 | — | 400 | 100 | — | 311 | 100 | — | 311 | 100 | — | 311 | 100 | — | 265 | Mbps |
| | ×8 | 80 | — | 400 | 80 | — | 311 | 80 | — | 311 | 80 | — | 311 | 80 | — | 265 | Mbps |
| | ×7 | 70 | — | 400 | 70 | — | 311 | 70 | — | 311 | 70 | — | 311 | 70 | — | 265 | Mbps |
| | ×4 | 40 | — | 400 | 40 | — | 311 | 40 | — | 311 | 40 | — | 311 | 40 | — | 265 | Mbps |
| | ×2 | 20 | — | 400 | 20 | — | 311 | 20 | — | 311 | 20 | — | 311 | 20 | — | 265 | Mbps |
| | ×1 | 10 | — | 400 | 10 | — | 311 | 10 | — | 311 | 10 | — | 311 | 10 | — | 265 | Mbps |
| $t_{DUTY}$ | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS | — | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 550 | — | — | 600 | — | — | 700 | ps |
| $t_{RISE}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ (3) | — | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | ms |

**Notes to Table 1–33:**

(1) Applicable for true and emulated mini-LVDS transmitter.

(2) Cyclone IV E—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated mini-LVDS transmitter is supported at the output pin of all I/O banks.
Cyclone IV GX—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(3) $t_{LOCK}$ is the time required for the PLL to lock from the end-of-device configuration.

(4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

**Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 2 of 2)**

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | C8L, I8L | | C9L | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{DUTY}$ | — | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |
| TCCS | — | — | 200 | — | 200 | — | 200 | — | 200 | — | 200 | ps |
| Output jitter (peak to peak) | — | — | 500 | — | 500 | — | 550 | — | 600 | — | 700 | ps |
| $t_{LOCK}$ (2) | — | — | 1 | — | 1 | — | 1 | — | 1 | — | 1 | ms |

**Notes to Table 1–35:**

(1) Cyclone IV E—emulated LVDS transmitter is supported at the output pin of all I/O Banks.
Cyclone IV GX—emulated LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(2) $t_{LOCK}$ is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

**Table 1–36. LVDS Receiver Timing Specifications for Cyclone IV Devices (1), (3)**

| Symbol | Modes | C6 | | C7, I7 | | C8, A7 | | C8L, I8L | | C9L | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×8 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×7 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×4 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×2 | 10 | 437.5 | 10 | 370 | 10 | 320 | 10 | 320 | 10 | 250 | MHz |
| | ×1 | 10 | 437.5 | 10 | 402.5 | 10 | 402.5 | 10 | 362 | 10 | 265 | MHz |
| HSIODR | ×10 | 100 | 875 | 100 | 740 | 100 | 640 | 100 | 640 | 100 | 500 | Mbps |
| | ×8 | 80 | 875 | 80 | 740 | 80 | 640 | 80 | 640 | 80 | 500 | Mbps |
| | ×7 | 70 | 875 | 70 | 740 | 70 | 640 | 70 | 640 | 70 | 500 | Mbps |
| | ×4 | 40 | 875 | 40 | 740 | 40 | 640 | 40 | 640 | 40 | 500 | Mbps |
| | ×2 | 20 | 875 | 20 | 740 | 20 | 640 | 20 | 640 | 20 | 500 | Mbps |
| | ×1 | 10 | 437.5 | 10 | 402.5 | 10 | 402.5 | 10 | 362 | 10 | 265 | Mbps |
| SW | — | — | 400 | — | 400 | — | 400 | — | 550 | — | 640 | ps |
| Input jitter tolerance | — | — | 500 | — | 500 | — | 550 | — | 600 | — | 700 | ps |
| $t_{LOCK}$ (2) | — | — | 1 | — | 1 | — | 1 | — | 1 | — | 1 | ms |

**Notes to Table 1–36:**

(1) Cyclone IV E—LVDS receiver is supported at all I/O Banks.
Cyclone IV GX—LVDS receiver is supported at I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(2) $t_{LOCK}$ is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

## External Memory Interface Specifications

The external memory interfaces for Cyclone IV devices are auto-calibrating and easy to implement.

## IOE Programmable Delay

Table 1–40 and Table 1–41 list the IOE programmable delay for Cyclone IV E 1.0 V core voltage devices.

**Table 1–40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | |
| | | | | C8L | I8L | C8L | C9L | I8L | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 2.054 | 1.924 | 3.387 | 4.017 | 3.411 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 2.010 | 1.875 | 3.341 | 4.252 | 3.367 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.641 | 0.631 | 1.111 | 1.377 | 1.124 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.971 | 0.931 | 1.684 | 2.298 | 1.684 | ns |

**Notes to Table 1–40:**

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–41. IOE Programmable Delay on Row Pins for Cyclone IV E 1.0 V Core Voltage Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | |
| | | | | C8L | I8L | C8L | C9L | I8L | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 2.057 | 1.921 | 3.389 | 4.146 | 3.412 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 2.059 | 1.919 | 3.420 | 4.374 | 3.441 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.670 | 0.623 | 1.160 | 1.420 | 1.168 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.960 | 0.919 | 1.656 | 2.258 | 1.656 | ns |

**Notes to Table 1–41:**

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

**Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | | Slow Corner | | | | | |
| | | | | C6 | I7 | A7 | C6 | C7 | C8 | I7 | A7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.314 | 1.211 | 1.211 | 2.177 | 2.340 | 2.433 | 2.388 | 2.508 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.307 | 1.203 | 1.203 | 2.19 | 2.387 | 2.540 | 2.430 | 2.545 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.437 | 0.402 | 0.402 | 0.747 | 0.820 | 0.880 | 0.834 | 0.873 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.693 | 0.665 | 0.665 | 1.200 | 1.379 | 1.532 | 1.393 | 1.441 | ns |

**Notes to Table 1–42:**

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | | Slow Corner | | | | | |
| | | | | C6 | I7 | A7 | C6 | C7 | C8 | I7 | A7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.314 | 1.209 | 1.209 | 2.201 | 2.386 | 2.510 | 2.429 | 2.548 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.312 | 1.207 | 1.207 | 2.202 | 2.402 | 2.558 | 2.447 | 2.557 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.458 | 0.419 | 0.419 | 0.783 | 0.861 | 0.924 | 0.875 | 0.915 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.686 | 0.657 | 0.657 | 1.185 | 1.360 | 1.506 | 1.376 | 1.422 | ns |

**Notes to Table 1–43:**

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

**Table 1–44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Settings | Min Offset | Max Offset | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | | |
| | | | | C6 | I7 | C6 | C7 | C8 | I7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.313 | 1.209 | 2.184 | 2.336 | 2.451 | 2.387 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.312 | 1.208 | 2.200 | 2.399 | 2.554 | 2.446 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.438 | 0.404 | 0.751 | 0.825 | 0.886 | 0.839 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.713 | 0.682 | 1.228 | 1.41 | 1.566 | 1.424 | ns |

**Notes to Table 1–44:**

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices** *(1), (2)*

| Parameter | Paths Affected | Number of Settings | Min Offset | Max Offset | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | | |
| | | | | C6 | I7 | C6 | C7 | C8 | I7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.314 | 1.210 | 2.209 | 2.398 | 2.526 | 2.443 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.313 | 1.208 | 2.205 | 2.406 | 2.563 | 2.450 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.461 | 0.421 | 0.789 | 0.869 | 0.933 | 0.884 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.712 | 0.682 | 1.225 | 1.407 | 1.562 | 1.421 | ns |

**Notes to Table 1–45:**

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software

**Table 1–46. Glossary (Part 2 of 5)**

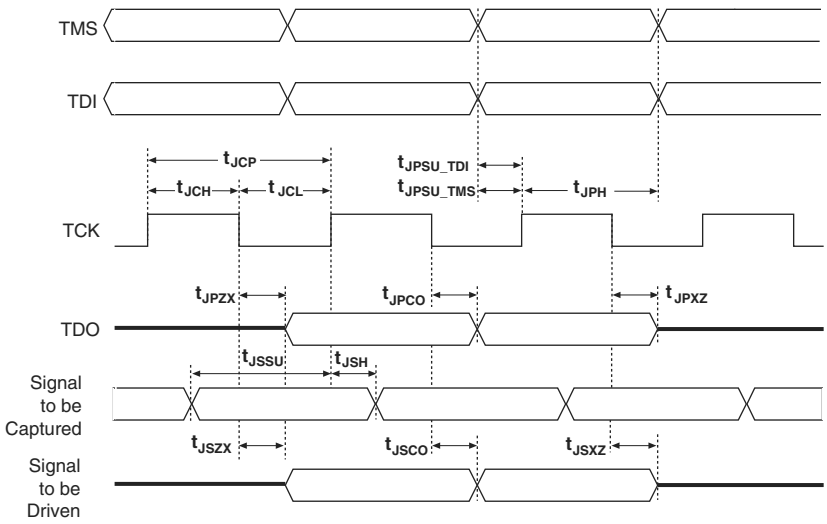
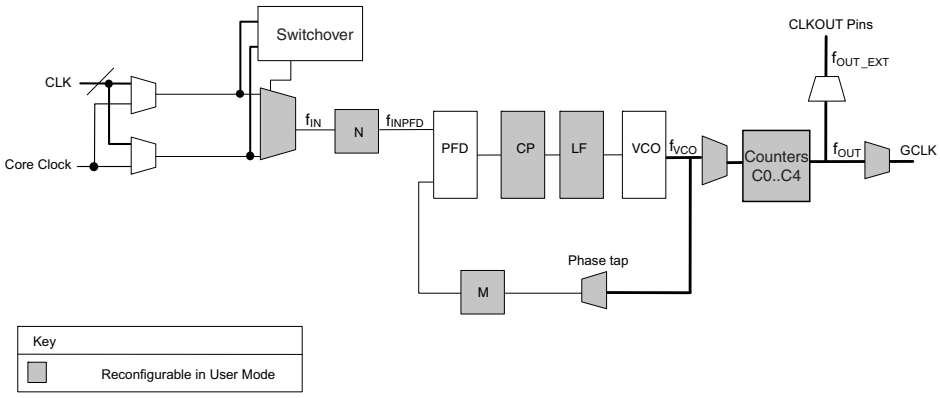
| Letter | Term | Definitions |
|---|---|---|
| J | JTAG Waveform |  |
| K | — | — |
| L | — | — |
| M | — | — |
| N | — | — |
| O | — | — |
| P | PLL Block | The following highlights the PLL specification parameters:  |
| Q | — | — |

**Table 1–46. Glossary (Part 3 of 5)**

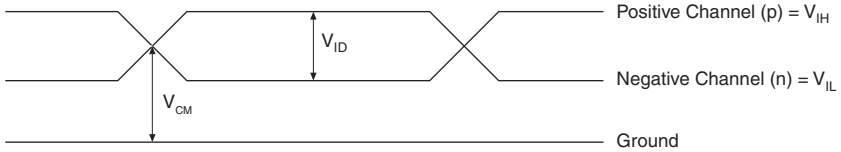
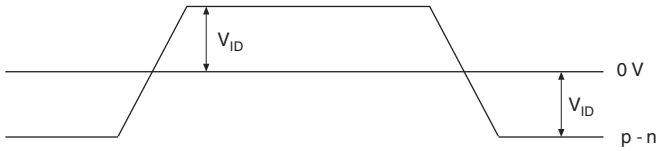
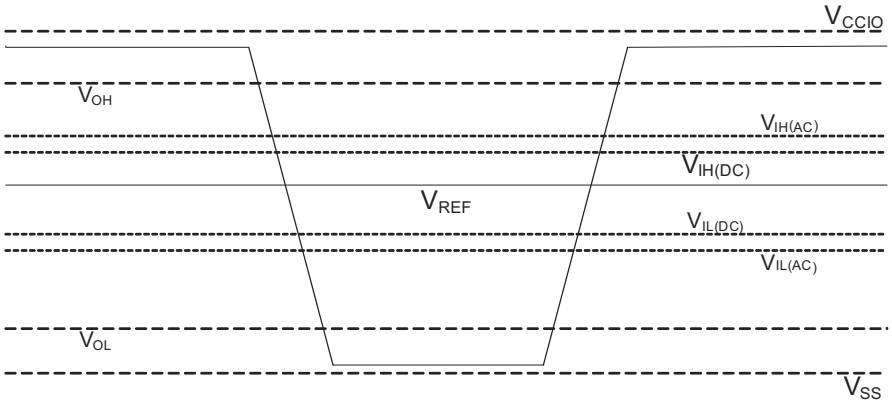
| Letter | Term | Definitions |
|---|---|---|
| R | $R_L$ | Receiver differential input discrete resistor (external to Cyclone IV devices). |
| | Receiver Input Waveform | Receiver input waveform for LVDS and LVPECL differential standards:<br>**Single-Ended Waveform**<br>  <br><br>**Differential Waveform (Mathematical Function of Positive & Negative Channel)**<br>  <br> |
| | Receiver input skew margin (RSKM) | High-speed I/O block: The total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2. |
| S | Single-ended voltage-referenced I/O Standard |  <br><br>The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform *ringing*. |
| | SW (Sampling Window) | High-speed I/O block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window. |

**Table 1–46. Glossary (Part 4 of 5)**

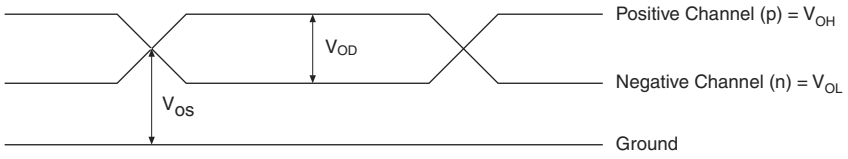
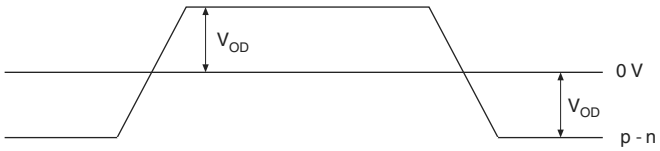
| Letter | Term | Definitions |
|---|---|---|
| T | $t_C$ | High-speed receiver and transmitter input and output clock period. |
| | Channel-to-channel-skew (TCCS) | High-speed I/O block: The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew. The clock is included in the TCCS measurement. |
| | $t_{cin}$ | Delay from the clock pad to the I/O input register. |
| | $t_{CO}$ | Delay from the clock pad to the I/O output. |
| | $t_{cout}$ | Delay from the clock pad to the I/O output register. |
| | $t_{DUTY}$ | High-speed I/O block: Duty cycle on high-speed transmitter output clock. |
| | $t_{FALL}$ | Signal high-to-low transition time (80–20%). |
| | $t_H$ | Input register hold time. |
| | Timing Unit Interval (TUI) | High-speed I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = $t_C$/w). |
| | $t_{INJITTER}$ | Period jitter on the PLL clock input. |
| | $t_{OUTJITTER\_DEDCLK}$ | Period jitter on the dedicated clock output driven by a PLL. |
| | $t_{OUTJITTER\_IO}$ | Period jitter on the general purpose I/O driven by a PLL. |
| | $t_{plicin}$ | Delay from the PLL inclk pad to the I/O input register. |
| | $t_{plicout}$ | Delay from the PLL inclk pad to the I/O output register. |
| | Transmitter Output Waveform | Transmitter output waveforms for the LVDS, mini-LVDS, PPDS and RSDS Differential I/O Standards:<br>**Single-Ended Waveform**<br>  <br><br>**Differential Waveform (Mathematical Function of Positive & Negative Channel)**<br>  <br> |
| | $t_{RISE}$ | Signal low-to-high transition time (20–80%). |
| | $t_{SU}$ | Input register setup time. |
| U | — | — |

**Table 1–46. Glossary (Part 5 of 5)**

| Letter | Term | Definitions |
|---|---|---|
| V | $V_{CM(DC)}$ | DC common mode input voltage. |
| | $V_{DIF(AC)}$ | AC differential input voltage: The minimum AC input differential voltage required for switching. |
| | $V_{DIF(DC)}$ | DC differential input voltage: The minimum DC input differential voltage required for switching. |
| | $V_{ICM}$ | Input common mode voltage: The common mode of the differential signal at the receiver. |
| | $V_{ID}$ | Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | $V_{IH}$ | Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high. |
| | $V_{IH(AC)}$ | High-level AC input voltage. |
| | $V_{IH(DC)}$ | High-level DC input voltage. |
| | $V_{IL}$ | Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low. |
| | $V_{IL\ (AC)}$ | Low-level AC input voltage. |
| | $V_{IL\ (DC)}$ | Low-level DC input voltage. |
| | $V_{IN}$ | DC input voltage. |
| | $V_{OCM}$ | Output common mode voltage: The common mode of the differential signal at the transmitter. |
| | $V_{OD}$ | Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} – V_{OL}$. |
| | $V_{OH}$ | Voltage output high: The maximum positive voltage from an output that the device considers is accepted as the minimum positive high level. |
| | $V_{OL}$ | Voltage output low: The maximum positive voltage from an output that the device considers is accepted as the maximum positive low level. |
| | $V_{OS}$ | Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$. |
| | $V_{OX\ (AC)}$ | AC differential output cross point voltage: the voltage at which the differential output signals must cross. |
| | $V_{REF}$ | Reference voltage for the SSTL and HSTL I/O standards. |
| | $V_{REF\ (AC)}$ | AC input reference voltage for the SSTL and HSTL I/O standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise. The peak-to-peak AC noise on $V_{REF}$ must not exceed 2% of $V_{REF(DC)}$. |
| | $V_{REF\ (DC)}$ | DC input reference voltage for the SSTL and HSTL I/O standards. |
| | $V_{SWING\ (AC)}$ | AC differential input voltage: AC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms. |
| | $V_{SWING\ (DC)}$ | DC differential input voltage: DC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms. |
| | $V_{TT}$ | Termination voltage for the SSTL and HSTL I/O standards. |
| | $V_{X\ (AC)}$ | AC differential input cross point voltage: The voltage at which the differential input signals must cross. |
| W | — | — |
| X | — | — |
| Y | — | — |
| Z | — | — |

**Table 1–47. Document Revision History**

| Date | Version | Changes |
|---|---|---|
| February 2010 | 1.1 | ■ Updated Table 1–3 through Table 1–44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release.<br>■ Minor text edits. |
| November 2009 | 1.0 | Initial release. |