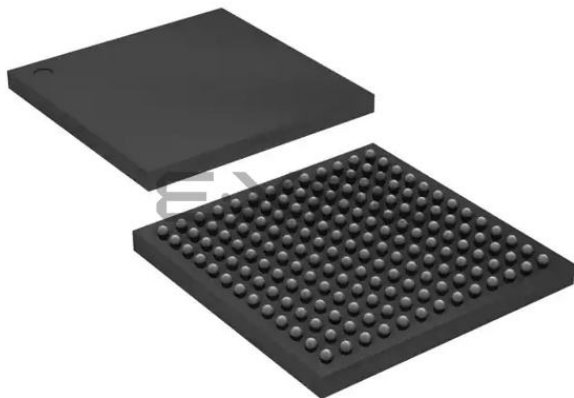




Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                   |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Active                                                                                                                            |
| Number of LABs/CLBs            | 900                                                                                                                               |
| Number of Logic Elements/Cells | 14400                                                                                                                             |
| Total RAM Bits                 | 552960                                                                                                                            |
| Number of I/O                  | 72                                                                                                                                |
| Number of Gates                | -                                                                                                                                 |
| Voltage - Supply               | 1.16V ~ 1.24V                                                                                                                     |
| Mounting Type                  | Surface Mount                                                                                                                     |
| Operating Temperature          | 0°C ~ 85°C (TJ)                                                                                                                   |
| Package / Case                 | 169-LBGA                                                                                                                          |
| Supplier Device Package        | 169-FBGA (14x14)                                                                                                                  |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/ep4cgx15bf14c6">https://www.e-xfl.com/product-detail/intel/ep4cgx15bf14c6</a> |

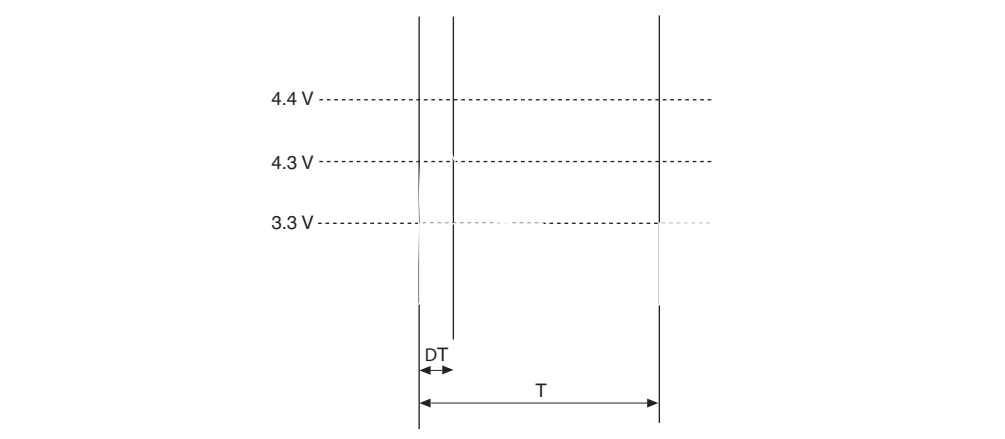
 A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

**Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices**

| Symbol | Parameter        | Condition (V) | Overshoot Duration as % of High Time | Unit |
|--------|------------------|---------------|--------------------------------------|------|
| $V_i$  | AC Input Voltage | $V_i = 4.20$  | 100                                  | %    |
|        |                  | $V_i = 4.25$  | 98                                   | %    |
|        |                  | $V_i = 4.30$  | 65                                   | %    |
|        |                  | $V_i = 4.35$  | 43                                   | %    |
|        |                  | $V_i = 4.40$  | 29                                   | %    |
|        |                  | $V_i = 4.45$  | 20                                   | %    |
|        |                  | $V_i = 4.50$  | 13                                   | %    |
|        |                  | $V_i = 4.55$  | 9                                    | %    |
|        |                  | $V_i = 4.60$  | 6                                    | %    |

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as  $([\Delta T]/T) \times 100$ . This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

**Figure 1–1. Cyclone IV Devices Overshoot Duration**



**Table 1-3. Recommended Operating Conditions for Cyclone IV E Devices <sup>(1), (2)</sup> (Part 2 of 2)**

| Symbol      | Parameter                                                  | Conditions | Min | Typ | Max | Unit |
|-------------|------------------------------------------------------------|------------|-----|-----|-----|------|
| $I_{Diode}$ | Magnitude of DC current across PCI-clamp diode when enable | —          | —   | —   | 10  | mA   |

**Notes to Table 1-3:**

- (1) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades.
- (2)  $V_{CCIO}$  for all I/O banks must be powered up during device operation. All  $V_{CCA}$  pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- (3)  $V_{CC}$  must rise monotonically.
- (4)  $V_{CCIO}$  powers all input buffers.
- (5) The POR time for Standard POR ranges between 50 and 200 ms. Each individual power supply must reach the recommended operating range within 50 ms.
- (6) The POR time for Fast POR ranges between 3 and 9 ms. Each individual power supply must reach the recommended operating range within 3 ms.

**Table 1-4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 1 of 2)**

| Symbol                                   | Parameter                                                          | Conditions | Min   | Typ | Max   | Unit |
|------------------------------------------|--------------------------------------------------------------------|------------|-------|-----|-------|------|
| $V_{CCINT}$ <sup>(3)</sup>               | Core voltage, PCIe hard IP block, and transceiver PCS power supply | —          | 1.16  | 1.2 | 1.24  | V    |
| $V_{CCA}$ <sup>(1), (3)</sup>            | PLL analog power supply                                            | —          | 2.375 | 2.5 | 2.625 | V    |
| $V_{CCD\_PLL}$ <sup>(2)</sup>            | PLL digital power supply                                           | —          | 1.16  | 1.2 | 1.24  | V    |
| $V_{CCIO}$ <sup>(3), (4)</sup>           | I/O banks power supply for 3.3-V operation                         | —          | 3.135 | 3.3 | 3.465 | V    |
|                                          | I/O banks power supply for 3.0-V operation                         | —          | 2.85  | 3   | 3.15  | V    |
|                                          | I/O banks power supply for 2.5-V operation                         | —          | 2.375 | 2.5 | 2.625 | V    |
|                                          | I/O banks power supply for 1.8-V operation                         | —          | 1.71  | 1.8 | 1.89  | V    |
|                                          | I/O banks power supply for 1.5-V operation                         | —          | 1.425 | 1.5 | 1.575 | V    |
|                                          | I/O banks power supply for 1.2-V operation                         | —          | 1.14  | 1.2 | 1.26  | V    |
| $V_{CC\_CLKIN}$ <sup>(3), (5), (6)</sup> | Differential clock input pins power supply for 3.3-V operation     | —          | 3.135 | 3.3 | 3.465 | V    |
|                                          | Differential clock input pins power supply for 3.0-V operation     | —          | 2.85  | 3   | 3.15  | V    |
|                                          | Differential clock input pins power supply for 2.5-V operation     | —          | 2.375 | 2.5 | 2.625 | V    |
|                                          | Differential clock input pins power supply for 1.8-V operation     | —          | 1.71  | 1.8 | 1.89  | V    |
|                                          | Differential clock input pins power supply for 1.5-V operation     | —          | 1.425 | 1.5 | 1.575 | V    |
|                                          | Differential clock input pins power supply for 1.2-V operation     | —          | 1.14  | 1.2 | 1.26  | V    |
| $V_{CCH\_GXB}$                           | Transceiver output buffer power supply                             | —          | 2.375 | 2.5 | 2.625 | V    |

**Table 1-4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)**

| Symbol         | Parameter                                                   | Conditions                                   | Min        | Typ | Max        | Unit |
|----------------|-------------------------------------------------------------|----------------------------------------------|------------|-----|------------|------|
| $V_{CCA\_GXB}$ | Transceiver PMA and auxiliary power supply                  | —                                            | 2.375      | 2.5 | 2.625      | V    |
| $V_{CCL\_GXB}$ | Transceiver PMA and auxiliary power supply                  | —                                            | 1.16       | 1.2 | 1.24       | V    |
| $V_I$          | DC input voltage                                            | —                                            | -0.5       | —   | 3.6        | V    |
| $V_O$          | DC output voltage                                           | —                                            | 0          | —   | $V_{CCIO}$ | V    |
| $T_J$          | Operating junction temperature                              | For commercial use                           | 0          | —   | 85         | °C   |
|                |                                                             | For industrial use                           | -40        | —   | 100        | °C   |
| $t_{RAMP}$     | Power supply ramp time                                      | Standard power-on reset (POR) <sup>(7)</sup> | 50 $\mu$ s | —   | 50 ms      | —    |
|                |                                                             | Fast POR <sup>(8)</sup>                      | 50 $\mu$ s | —   | 3 ms       | —    |
| $I_{Diode}$    | Magnitude of DC current across PCI-clamp diode when enabled | —                                            | —          | —   | 10         | mA   |

**Notes to Table 1-4:**

- (1) All  $V_{CCA}$  pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- (2) You must connect  $V_{CCD\_PLL}$  to  $V_{CCINT}$  through a decoupling capacitor and ferrite bead.
- (3) Power supplies must rise monotonically.
- (4)  $V_{CCIO}$  for all I/O banks must be powered up during device operation. Configurations pins are powered up by  $V_{CCIO}$  of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support  $V_{CCIO}$  of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the  $V_{CCIO}$  level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.
- (5) You must set  $V_{CC\_CLKIN}$  to 2.5 V if you use  $CLKIN$  as a high-speed serial interface (HSSI)  $refclk$  or as a  $DIFFCLK$  input.
- (6) The  $CLKIN$  pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.
- (7) The POR time for Standard POR ranges between 50 and 200 ms.  $V_{CCINT}$ ,  $V_{CCA}$ , and  $V_{CCIO}$  of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.
- (8) The POR time for Fast POR ranges between 3 and 9 ms.  $V_{CCINT}$ ,  $V_{CCA}$ , and  $V_{CCIO}$  of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

## ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1-5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

**Table 1-5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os**

| Symbol       | Parameter                                        | Passing Voltage | Unit |
|--------------|--------------------------------------------------|-----------------|------|
| $V_{ESDHBM}$ | ESD voltage using the HBM (GPIOs) <sup>(1)</sup> | $\pm 2000$      | V    |
|              | ESD using the HBM (HSSI I/Os) <sup>(2)</sup>     | $\pm 1000$      | V    |
| $V_{ESDCDM}$ | ESD using the CDM (GPIOs)                        | $\pm 500$       | V    |
|              | ESD using the CDM (HSSI I/Os) <sup>(2)</sup>     | $\pm 250$       | V    |

**Notes to Table 1-5:**

- (1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is  $\pm 1000$ V.
- (2) This value is applicable only to Cyclone IV GX devices.

## DC Characteristics

This section lists the I/O leakage current, pin capacitance, on-chip termination (OCT) tolerance, and bus hold specifications for Cyclone IV devices.

### Supply Current

The device supply current requirement is the minimum current drawn from the power supply pins that can be used as a reference for power size planning. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary greatly with the resources used. Table 1-6 lists the I/O pin leakage current for Cyclone IV devices.

**Table 1-6. I/O Pin Leakage Current for Cyclone IV Devices <sup>(1), (2)</sup>**

| Symbol   | Parameter                         | Conditions                        | Device | Min | Typ | Max | Unit          |
|----------|-----------------------------------|-----------------------------------|--------|-----|-----|-----|---------------|
| $I_I$    | Input pin leakage current         | $V_I = 0\text{ V to }V_{CCIOMAX}$ | —      | -10 | —   | 10  | $\mu\text{A}$ |
| $I_{OZ}$ | Tristated I/O pin leakage current | $V_O = 0\text{ V to }V_{CCIOMAX}$ | —      | -10 | —   | 10  | $\mu\text{A}$ |

**Notes to Table 1-6:**

- (1) This value is specified for normal device operation. The value varies during device power-up. This applies for all  $V_{CCIO}$  settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).
- (2) The 10  $\mu\text{A}$  I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

### Bus Hold

The bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1-7 lists bus hold specifications for Cyclone IV devices.

**Table 1-7. Bus Hold Parameter for Cyclone IV Devices (Part 1 of 2) <sup>(1)</sup>**

| Parameter                         | Condition                                   | V <sub>CCIO</sub> (V) |      |     |      |     |      |     |      |     |      |     |      | Unit |
|-----------------------------------|---------------------------------------------|-----------------------|------|-----|------|-----|------|-----|------|-----|------|-----|------|------|
|                                   |                                             | 1.2                   |      | 1.5 |      | 1.8 |      | 2.5 |      | 3.0 |      | 3.3 |      |      |
|                                   |                                             | Min                   | Max  | Min | Max  | Min | Max  | Min | Max  | Min | Max  | Min | Max  |      |
| Bus hold low, sustaining current  | V <sub>IN</sub> > V <sub>IL</sub> (maximum) | 8                     | —    | 12  | —    | 30  | —    | 50  | —    | 70  | —    | 70  | —    | μA   |
| Bus hold high, sustaining current | V <sub>IN</sub> < V <sub>IL</sub> (minimum) | −8                    | —    | −12 | —    | −30 | —    | −50 | —    | −70 | —    | −70 | —    | μA   |
| Bus hold low, overdrive current   | 0 V < V <sub>IN</sub> < V <sub>CCIO</sub>   | —                     | 125  | —   | 175  | —   | 200  | —   | 300  | —   | 500  | —   | 500  | μA   |
| Bus hold high, overdrive current  | 0 V < V <sub>IN</sub> < V <sub>CCIO</sub>   | —                     | −125 | —   | −175 | —   | −200 | —   | −300 | —   | −500 | —   | −500 | μA   |

Example 1–1 shows how to calculate the change of 50-Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

#### Example 1–1. Impedance Change

$$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$$

$$\Delta R_T = (85 - 25) \times 0.262 = 15.72$$

Because  $\Delta R_V$  is negative,

$$MF_V = 1 / (3.83/100 + 1) = 0.963$$

Because  $\Delta R_T$  is positive,

$$MF_T = 15.72/100 + 1 = 1.157$$

$$MF = 0.963 \times 1.157 = 1.114$$

$$R_{\text{final}} = 50 \times 1.114 = 55.71 \, \Omega$$

## Pin Capacitance

Table 1–11 lists the pin capacitance for Cyclone IV devices.

**Table 1–11. Pin Capacitance for Cyclone IV Devices <sup>(1)</sup>**

| Symbol                     | Parameter                                                                                                           | Typical –<br>Quad Flat<br>Pack<br>(QFP) | Typical –<br>Quad Flat<br>No Leads<br>(QFN) | Typical –<br>Ball-Grid<br>Array<br>(BGA) | Unit |
|----------------------------|---------------------------------------------------------------------------------------------------------------------|-----------------------------------------|---------------------------------------------|------------------------------------------|------|
| C <sub>IOTB</sub>          | Input capacitance on top and bottom I/O pins                                                                        | 7                                       | 7                                           | 6                                        | pF   |
| C <sub>IOLR</sub>          | Input capacitance on right I/O pins                                                                                 | 7                                       | 7                                           | 5                                        | pF   |
| C <sub>LVDSLR</sub>        | Input capacitance on right I/O pins with dedicated LVDS output                                                      | 8                                       | 8                                           | 7                                        | pF   |
| C <sub>VREFLR</sub><br>(2) | Input capacitance on right dual-purpose V <sub>REF</sub> pin when used as V <sub>REF</sub> or user I/O pin          | 21                                      | 21                                          | 21                                       | pF   |
| C <sub>VREFTB</sub><br>(2) | Input capacitance on top and bottom dual-purpose V <sub>REF</sub> pin when used as V <sub>REF</sub> or user I/O pin | 23 (3)                                  | 23                                          | 23                                       | pF   |
| C <sub>CLKTB</sub>         | Input capacitance on top and bottom dedicated clock input pins                                                      | 7                                       | 7                                           | 6                                        | pF   |
| C <sub>CLKLR</sub>         | Input capacitance on right dedicated clock input pins                                                               | 6                                       | 6                                           | 5                                        | pF   |

#### Notes to Table 1–11:

- (1) The pin capacitance applies to FBGA, UBGA, and MBGA packages.
- (2) When you use the V<sub>REF</sub> pin as a regular input or output, you can expect a reduced performance of toggle rate and t<sub>CO</sub> because of higher pin capacitance.
- (3) C<sub>VREFTB</sub> for the EP4CE22 device is 30 pF.

## Internal Weak Pull-Up and Weak Pull-Down Resistor

Table 1-12 lists the weak pull-up and pull-down resistor values for Cyclone IV devices.

**Table 1-12. Internal Weak Pull-Up and Weak Pull-Down Resistor Values for Cyclone IV Devices <sup>(1)</sup>**

| Symbol          | Parameter                                                                                                                                          | Conditions                                         | Min | Typ | Max | Unit |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|-----|-----|-----|------|
| R <sub>PU</sub> | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option | V <sub>CCIO</sub> = 3.3 V ± 5% <sup>(2), (3)</sup> | 7   | 25  | 41  | kΩ   |
|                 |                                                                                                                                                    | V <sub>CCIO</sub> = 3.0 V ± 5% <sup>(2), (3)</sup> | 7   | 28  | 47  | kΩ   |
|                 |                                                                                                                                                    | V <sub>CCIO</sub> = 2.5 V ± 5% <sup>(2), (3)</sup> | 8   | 35  | 61  | kΩ   |
|                 |                                                                                                                                                    | V <sub>CCIO</sub> = 1.8 V ± 5% <sup>(2), (3)</sup> | 10  | 57  | 108 | kΩ   |
|                 |                                                                                                                                                    | V <sub>CCIO</sub> = 1.5 V ± 5% <sup>(2), (3)</sup> | 13  | 82  | 163 | kΩ   |
|                 |                                                                                                                                                    | V <sub>CCIO</sub> = 1.2 V ± 5% <sup>(2), (3)</sup> | 19  | 143 | 351 | kΩ   |
| R <sub>PD</sub> | Value of the I/O pin pull-down resistor before and during configuration                                                                            | V <sub>CCIO</sub> = 3.3 V ± 5% <sup>(4)</sup>      | 6   | 19  | 30  | kΩ   |
|                 |                                                                                                                                                    | V <sub>CCIO</sub> = 3.0 V ± 5% <sup>(4)</sup>      | 6   | 22  | 36  | kΩ   |
|                 |                                                                                                                                                    | V <sub>CCIO</sub> = 2.5 V ± 5% <sup>(4)</sup>      | 6   | 25  | 43  | kΩ   |
|                 |                                                                                                                                                    | V <sub>CCIO</sub> = 1.8 V ± 5% <sup>(4)</sup>      | 7   | 35  | 71  | kΩ   |
|                 |                                                                                                                                                    | V <sub>CCIO</sub> = 1.5 V ± 5% <sup>(4)</sup>      | 8   | 50  | 112 | kΩ   |

### Notes to Table 1-12:

- (1) All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.
- (2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V<sub>CCIO</sub>.
- (3)  $R_{PU} = (V_{CCIO} - V_I) / I_{R_{PU}}$   
Minimum condition: -40°C; V<sub>CCIO</sub> = V<sub>CC</sub> + 5%, V<sub>I</sub> = V<sub>CC</sub> + 5% - 50 mV;  
Typical condition: 25°C; V<sub>CCIO</sub> = V<sub>CC</sub>, V<sub>I</sub> = 0 V;  
Maximum condition: 100°C; V<sub>CCIO</sub> = V<sub>CC</sub> - 5%, V<sub>I</sub> = 0 V; in which V<sub>I</sub> refers to the input voltage at the I/O pin.
- (4)  $R_{PD} = V_I / I_{R_{PD}}$   
Minimum condition: -40°C; V<sub>CCIO</sub> = V<sub>CC</sub> + 5%, V<sub>I</sub> = 50 mV;  
Typical condition: 25°C; V<sub>CCIO</sub> = V<sub>CC</sub>, V<sub>I</sub> = V<sub>CC</sub> - 5%;  
Maximum condition: 100°C; V<sub>CCIO</sub> = V<sub>CC</sub> - 5%, V<sub>I</sub> = V<sub>CC</sub> - 5%; in which V<sub>I</sub> refers to the input voltage at the I/O pin.

## Hot-Socketing

Table 1-13 lists the hot-socketing specifications for Cyclone IV devices.

**Table 1-13. Hot-Socketing Specifications for Cyclone IV Devices**

| Symbol                  | Parameter                         | Maximum             |
|-------------------------|-----------------------------------|---------------------|
| I <sub>IOPIN(DC)</sub>  | DC current per I/O pin            | 300 μA              |
| I <sub>IOPIN(AC)</sub>  | AC current per I/O pin            | 8 mA <sup>(1)</sup> |
| I <sub>XCVRTX(DC)</sub> | DC current per transceiver TX pin | 100 mA              |
| I <sub>XCVRRX(DC)</sub> | DC current per transceiver RX pin | 50 mA               |

### Note to Table 1-13:

- (1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |I<sub>IOPIN</sub>| = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.



During hot-socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

## Schmitt Trigger Input

Cyclone IV devices support Schmitt trigger input on the TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF\_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rate. Table 1–14 lists the hysteresis specifications across the supported  $V_{CCIO}$  range for Schmitt trigger inputs in Cyclone IV devices.

**Table 1–14. Hysteresis Specifications for Schmitt Trigger Input in Cyclone IV Devices**

| Symbol        | Parameter                            | Conditions (V)   | Minimum | Unit |
|---------------|--------------------------------------|------------------|---------|------|
| $V_{SCHMITT}$ | Hysteresis for Schmitt trigger input | $V_{CCIO} = 3.3$ | 200     | mV   |
|               |                                      | $V_{CCIO} = 2.5$ | 200     | mV   |
|               |                                      | $V_{CCIO} = 1.8$ | 140     | mV   |
|               |                                      | $V_{CCIO} = 1.5$ | 110     | mV   |

## I/O Standard Specifications

The following tables list input voltage sensitivities ( $V_{IH}$  and  $V_{IL}$ ), output voltage ( $V_{OH}$  and  $V_{OL}$ ), and current drive characteristics ( $I_{OH}$  and  $I_{OL}$ ), for various I/O standards supported by Cyclone IV devices. Table 1–15 through Table 1–20 provide the I/O standard specifications for Cyclone IV devices.

**Table 1–15. Single-Ended I/O Standard Specifications for Cyclone IV Devices <sup>(1), (2)</sup>**

| I/O Standard                | $V_{CCIO}$ (V) |     |       | $V_{IL}$ (V) |                        | $V_{IH}$ (V)           |                  | $V_{OL}$ (V)           | $V_{OH}$ (V)           | $I_{OL}$ (mA)<br>(4) | $I_{OH}$ (mA)<br>(4) |
|-----------------------------|----------------|-----|-------|--------------|------------------------|------------------------|------------------|------------------------|------------------------|----------------------|----------------------|
|                             | Min            | Typ | Max   | Min          | Max                    | Min                    | Max              | Max                    | Min                    |                      |                      |
| 3.3-V LVTTTL <sup>(3)</sup> | 3.135          | 3.3 | 3.465 | —            | 0.8                    | 1.7                    | 3.6              | 0.45                   | 2.4                    | 4                    | –4                   |
| 3.3-V LVCMOS <sup>(3)</sup> | 3.135          | 3.3 | 3.465 | —            | 0.8                    | 1.7                    | 3.6              | 0.2                    | $V_{CCIO} - 0.2$       | 2                    | –2                   |
| 3.0-V LVTTTL <sup>(3)</sup> | 2.85           | 3.0 | 3.15  | –0.3         | 0.8                    | 1.7                    | $V_{CCIO} + 0.3$ | 0.45                   | 2.4                    | 4                    | –4                   |
| 3.0-V LVCMOS <sup>(3)</sup> | 2.85           | 3.0 | 3.15  | –0.3         | 0.8                    | 1.7                    | $V_{CCIO} + 0.3$ | 0.2                    | $V_{CCIO} - 0.2$       | 0.1                  | –0.1                 |
| 2.5 V <sup>(3)</sup>        | 2.375          | 2.5 | 2.625 | –0.3         | 0.7                    | 1.7                    | $V_{CCIO} + 0.3$ | 0.4                    | 2.0                    | 1                    | –1                   |
| 1.8 V                       | 1.71           | 1.8 | 1.89  | –0.3         | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | 2.25             | 0.45                   | $V_{CCIO} - 0.45$      | 2                    | –2                   |
| 1.5 V                       | 1.425          | 1.5 | 1.575 | –0.3         | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2                    | –2                   |
| 1.2 V                       | 1.14           | 1.2 | 1.26  | –0.3         | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2                    | –2                   |
| 3.0-V PCI                   | 2.85           | 3.0 | 3.15  | —            | $0.3 \times V_{CCIO}$  | $0.5 \times V_{CCIO}$  | $V_{CCIO} + 0.3$ | $0.1 \times V_{CCIO}$  | $0.9 \times V_{CCIO}$  | 1.5                  | –0.5                 |
| 3.0-V PCI-X                 | 2.85           | 3.0 | 3.15  | —            | $0.35 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$  | $V_{CCIO} + 0.3$ | $0.1 \times V_{CCIO}$  | $0.9 \times V_{CCIO}$  | 1.5                  | –0.5                 |

**Notes to Table 1–15:**

- (1) For voltage-referenced receiver input waveform and explanation of terms used in Table 1–15, refer to “Glossary” on page 1–37.
- (2) AC load  $CL = 10$  pF
- (3) For more information about interfacing Cyclone IV devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O standards, refer to *AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O Systems*.
- (4) To meet the  $I_{OL}$  and  $I_{OH}$  specifications, you must set the current strength settings accordingly. For example, to meet the **3.3-V LVTTTL** specification (4 mA), set the current strength settings to 4 mA or higher. Setting at lower current strength may not meet the  $I_{OL}$  and  $I_{OH}$  specifications in the handbook.



**Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices <sup>(1)</sup> (Part 2 of 2)**

| I/O Standard                                | V <sub>CCIO</sub> (V) |     |       | V <sub>ID</sub> (mV) |     | V <sub>ICM</sub> (V) <sup>(2)</sup> |                                                       |      | V <sub>OD</sub> (mV) <sup>(3)</sup> |     |     | V <sub>OS</sub> (V) <sup>(3)</sup> |      |       |
|---------------------------------------------|-----------------------|-----|-------|----------------------|-----|-------------------------------------|-------------------------------------------------------|------|-------------------------------------|-----|-----|------------------------------------|------|-------|
|                                             | Min                   | Typ | Max   | Min                  | Max | Min                                 | Condition                                             | Max  | Min                                 | Typ | Max | Min                                | Typ  | Max   |
| LVDS<br>(Column I/Os)                       | 2.375                 | 2.5 | 2.625 | 100                  | —   | 0.05                                | $D_{MAX} \leq 500 \text{ Mbps}$                       | 1.80 | 247                                 | —   | 600 | 1.125                              | 1.25 | 1.375 |
|                                             |                       |     |       |                      |     | 0.55                                | $500 \text{ Mbps} \leq D_{MAX} \leq 700 \text{ Mbps}$ | 1.80 |                                     |     |     |                                    |      |       |
|                                             |                       |     |       |                      |     | 1.05                                | $D_{MAX} > 700 \text{ Mbps}$                          | 1.55 |                                     |     |     |                                    |      |       |
| BLVDS (Row I/Os) <sup>(4)</sup>             | 2.375                 | 2.5 | 2.625 | 100                  | —   | —                                   | —                                                     | —    | —                                   | —   | —   | —                                  | —    | —     |
| BLVDS (Column I/Os) <sup>(4)</sup>          | 2.375                 | 2.5 | 2.625 | 100                  | —   | —                                   | —                                                     | —    | —                                   | —   | —   | —                                  | —    | —     |
| mini-LVDS (Row I/Os) <sup>(5)</sup>         | 2.375                 | 2.5 | 2.625 | —                    | —   | —                                   | —                                                     | —    | 300                                 | —   | 600 | 1.0                                | 1.2  | 1.4   |
| mini-LVDS (Column I/Os) <sup>(5)</sup>      | 2.375                 | 2.5 | 2.625 | —                    | —   | —                                   | —                                                     | —    | 300                                 | —   | 600 | 1.0                                | 1.2  | 1.4   |
| RSDS <sup>®</sup> (Row I/Os) <sup>(5)</sup> | 2.375                 | 2.5 | 2.625 | —                    | —   | —                                   | —                                                     | —    | 100                                 | 200 | 600 | 0.5                                | 1.2  | 1.5   |
| RSDS (Column I/Os) <sup>(5)</sup>           | 2.375                 | 2.5 | 2.625 | —                    | —   | —                                   | —                                                     | —    | 100                                 | 200 | 600 | 0.5                                | 1.2  | 1.5   |
| PPDS (Row I/Os) <sup>(5)</sup>              | 2.375                 | 2.5 | 2.625 | —                    | —   | —                                   | —                                                     | —    | 100                                 | 200 | 600 | 0.5                                | 1.2  | 1.4   |
| PPDS (Column I/Os) <sup>(5)</sup>           | 2.375                 | 2.5 | 2.625 | —                    | —   | —                                   | —                                                     | —    | 100                                 | 200 | 600 | 0.5                                | 1.2  | 1.4   |

**Notes to Table 1–20:**

- (1) For an explanation of terms used in Table 1–20, refer to “Glossary” on page 1–37.
- (2) V<sub>IN</sub> range:  $0 \text{ V} \leq V_{IN} \leq 1.85 \text{ V}$ .
- (3) R<sub>L</sub> range:  $90 \leq R_L \leq 110 \Omega$ .
- (4) There are no fixed V<sub>IN</sub>, V<sub>OD</sub>, and V<sub>OS</sub> specifications for BLVDS. They depend on the system topology.
- (5) The Mini-LVDS, RSDS, and PPDS standards are only supported at the output pins.
- (6) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported for output pins.

## Transceiver Performance Specifications

Table 1-21 lists the Cyclone IV GX transceiver specifications.

**Table 1-21. Transceiver Specification for Cyclone IV GX Devices (Part 1 of 4)**

| Symbol/<br>Description                           | Conditions                                                          | C6                      |            |        | C7, I7                  |            |        | C8                      |            |        | Unit   |
|--------------------------------------------------|---------------------------------------------------------------------|-------------------------|------------|--------|-------------------------|------------|--------|-------------------------|------------|--------|--------|
|                                                  |                                                                     | Min                     | Typ        | Max    | Min                     | Typ        | Max    | Min                     | Typ        | Max    |        |
| Reference Clock                                  |                                                                     |                         |            |        |                         |            |        |                         |            |        |        |
| Supported I/O Standards                          | 1.2 V PCML, 1.5 V PCML, 3.3 V PCML, Differential LVPECL, LVDS, HCSL |                         |            |        |                         |            |        |                         |            |        |        |
| Input frequency from REFCLK input pins           | —                                                                   | 50                      | —          | 156.25 | 50                      | —          | 156.25 | 50                      | —          | 156.25 | MHz    |
| Spread-spectrum modulating clock frequency       | Physical interface for PCI Express (PIPE) mode                      | 30                      | —          | 33     | 30                      | —          | 33     | 30                      | —          | 33     | kHz    |
| Spread-spectrum downspread                       | PIPE mode                                                           | —                       | 0 to –0.5% | —      | —                       | 0 to –0.5% | —      | —                       | 0 to –0.5% | —      | —      |
| Peak-to-peak differential input voltage          | —                                                                   | 0.1                     | —          | 1.6    | 0.1                     | —          | 1.6    | 0.1                     | —          | 1.6    | V      |
| V <sub>ICM</sub> (AC coupled)                    | —                                                                   | 1100 ± 5%               |            |        | 1100 ± 5%               |            |        | 1100 ± 5%               |            |        | mV     |
| V <sub>ICM</sub> (DC coupled)                    | HCSL I/O standard for PCIe reference clock                          | 250                     | —          | 550    | 250                     | —          | 550    | 250                     | —          | 550    | mV     |
| Transmitter REFCLK Phase Noise <sup>(1)</sup>    | Frequency offset = 1 MHz – 8 MHz                                    | —                       | —          | –123   | —                       | —          | –123   | —                       | —          | –123   | dBc/Hz |
| Transmitter REFCLK Total Jitter <sup>(1)</sup>   |                                                                     | —                       | —          | 42.3   | —                       | —          | 42.3   | —                       | —          | 42.3   | ps     |
| R <sub>ref</sub>                                 | —                                                                   | —                       | 2000 ± 1%  | —      | —                       | 2000 ± 1%  | —      | —                       | 2000 ± 1%  | —      | Ω      |
| Transceiver Clock                                |                                                                     |                         |            |        |                         |            |        |                         |            |        |        |
| cal_blk_clk clock frequency                      | —                                                                   | 10                      | —          | 125    | 10                      | —          | 125    | 10                      | —          | 125    | MHz    |
| fixedclk clock frequency                         | PCIe Receiver Detect                                                | —                       | 125        | —      | —                       | 125        | —      | —                       | 125        | —      | MHz    |
| reconfig_clk clock frequency                     | Dynamic reconfiguration clock frequency                             | 2.5/37.5 <sup>(2)</sup> | —          | 50     | 2.5/37.5 <sup>(2)</sup> | —          | 50     | 2.5/37.5 <sup>(2)</sup> | —          | 50     | MHz    |
| Delta time between reconfig_clk                  | —                                                                   | —                       | —          | 2      | —                       | —          | 2      | —                       | —          | 2      | ms     |
| Transceiver block minimum power-down pulse width | —                                                                   | —                       | 1          | —      | —                       | 1          | —      | —                       | 1          | —      | μs     |

Table 1-21. Transceiver Specification for Cyclone IV GX Devices (Part 2 of 4)

| Symbol/<br>Description                                                               | Conditions                                                            | C6                              |           |                                                   | C7, I7 |           |                                                   | C8   |           |                                                   | Unit |
|--------------------------------------------------------------------------------------|-----------------------------------------------------------------------|---------------------------------|-----------|---------------------------------------------------|--------|-----------|---------------------------------------------------|------|-----------|---------------------------------------------------|------|
|                                                                                      |                                                                       | Min                             | Typ       | Max                                               | Min    | Typ       | Max                                               | Min  | Typ       | Max                                               |      |
| Receiver                                                                             |                                                                       |                                 |           |                                                   |        |           |                                                   |      |           |                                                   |      |
| Supported I/O Standards                                                              | 1.4 V PCML,<br>1.5 V PCML,<br>2.5 V PCML,<br>LVPECL, LVDS             |                                 |           |                                                   |        |           |                                                   |      |           |                                                   |      |
| Data rate (F324 and smaller package) <sup>(15)</sup>                                 | —                                                                     | 600                             | —         | 2500                                              | 600    | —         | 2500                                              | 600  | —         | 2500                                              | Mbps |
| Data rate (F484 and larger package) <sup>(15)</sup>                                  | —                                                                     | 600                             | —         | 3125                                              | 600    | —         | 3125                                              | 600  | —         | 2500                                              | Mbps |
| Absolute V <sub>MAX</sub> for a receiver pin <sup>(3)</sup>                          | —                                                                     | —                               | —         | 1.6                                               | —      | —         | 1.6                                               | —    | —         | 1.6                                               | V    |
| Operational V <sub>MAX</sub> for a receiver pin                                      | —                                                                     | —                               | —         | 1.5                                               | —      | —         | 1.5                                               | —    | —         | 1.5                                               | V    |
| Absolute V <sub>MIN</sub> for a receiver pin                                         | —                                                                     | −0.4                            | —         | —                                                 | −0.4   | —         | —                                                 | −0.4 | —         | —                                                 | V    |
| Peak-to-peak differential input voltage V <sub>ID</sub> (diff p-p)                   | V <sub>ICM</sub> = 0.82 V setting, Data Rate = 600 Mbps to 3.125 Gbps | 0.1                             | —         | 2.7                                               | 0.1    | —         | 2.7                                               | 0.1  | —         | 2.7                                               | V    |
| V <sub>ICM</sub>                                                                     | V <sub>ICM</sub> = 0.82 V setting                                     | —                               | 820 ± 10% | —                                                 | —      | 820 ± 10% | —                                                 | —    | 820 ± 10% | —                                                 | mV   |
| Differential on-chip termination resistors                                           | 100−Ω setting                                                         | —                               | 100       | —                                                 | —      | 100       | —                                                 | —    | 100       | —                                                 | Ω    |
|                                                                                      | 150−Ω setting                                                         | —                               | 150       | —                                                 | —      | 150       | —                                                 | —    | 150       | —                                                 | Ω    |
| Differential and common mode return loss                                             | PIPE, Serial Rapid I/O SR, SATA, CPRI LV, SDI, XAUI                   | Compliant                       |           |                                                   |        |           |                                                   |      |           |                                                   | —    |
| Programmable ppm detector <sup>(4)</sup>                                             | —                                                                     | ± 62.5, 100, 125, 200, 250, 300 |           |                                                   |        |           |                                                   |      |           |                                                   | ppm  |
| Clock data recovery (CDR) ppm tolerance (without spread-spectrum clocking enabled)   | —                                                                     | —                               | —         | ±300 <sup>(5)</sup> ,<br>±350 <sup>(6), (7)</sup> | —      | —         | ±300 <sup>(5)</sup> ,<br>±350 <sup>(6), (7)</sup> | —    | —         | ±300 <sup>(5)</sup> ,<br>±350 <sup>(6), (7)</sup> | ppm  |
| CDR ppm tolerance (with synchronous spread-spectrum clocking enabled) <sup>(8)</sup> | —                                                                     | —                               | —         | 350 to −5350 <sup>(7), (9)</sup>                  | —      | —         | 350 to −5350 <sup>(7), (9)</sup>                  | —    | —         | 350 to −5350 <sup>(7), (9)</sup>                  | ppm  |
| Run length                                                                           | —                                                                     | —                               | 80        | —                                                 | —      | 80        | —                                                 | —    | 80        | —                                                 | UI   |
| Programmable equalization                                                            | No Equalization                                                       | —                               | —         | 1.5                                               | —      | —         | 1.5                                               | —    | —         | 1.5                                               | dB   |
|                                                                                      | Medium Low                                                            | —                               | —         | 4.5                                               | —      | —         | 4.5                                               | —    | —         | 4.5                                               | dB   |
|                                                                                      | Medium High                                                           | —                               | —         | 5.5                                               | —      | —         | 5.5                                               | —    | —         | 5.5                                               | dB   |
|                                                                                      | High                                                                  | —                               | —         | 7                                                 | —      | —         | 7                                                 | —    | —         | 7                                                 | dB   |

Figure 1-4 shows the differential receiver input waveform.

**Figure 1-4. Receiver Input Waveform**

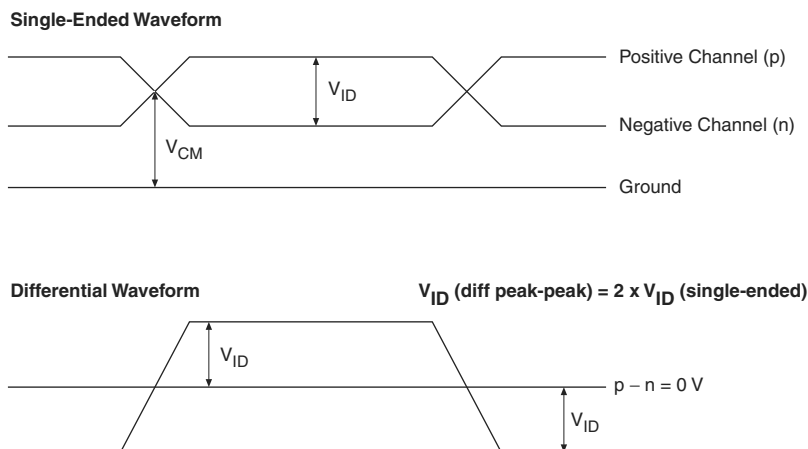


Figure 1-5 shows the transmitter output waveform.

**Figure 1-5. Transmitter Output Waveform**

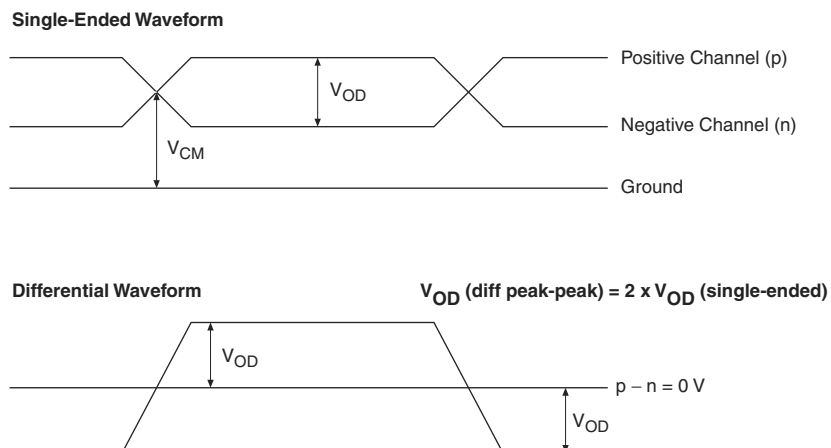


Table 1-22 lists the typical  $V_{OD}$  for Tx term that equals 100  $\Omega$ .

**Table 1-22. Typical  $V_{OD}$  Setting, Tx Term = 100  $\Omega$**

| Symbol                                          | $V_{OD}$ Setting (mV) |     |     |       |      |      |
|-------------------------------------------------|-----------------------|-----|-----|-------|------|------|
|                                                 | 1                     | 2   | 3   | 4 (1) | 5    | 6    |
| $V_{OD}$ differential peak to peak typical (mV) | 400                   | 600 | 800 | 900   | 1000 | 1200 |

**Note to Table 1-22:**

(1) This setting is required for compliance with the PCIe protocol.

Table 1–23 lists the Cyclone IV GX transceiver block AC specifications.

**Table 1–23. Transceiver Block AC Specification for Cyclone IV GX Devices <sup>(1), (2)</sup>**

| Symbol/<br>Description                                            | Conditions         | C6     |     |       | C7, I7 |     |       | C8     |     |       | Unit |
|-------------------------------------------------------------------|--------------------|--------|-----|-------|--------|-----|-------|--------|-----|-------|------|
|                                                                   |                    | Min    | Typ | Max   | Min    | Typ | Max   | Min    | Typ | Max   |      |
| PCIe Transmit Jitter Generation <sup>(3)</sup>                    |                    |        |     |       |        |     |       |        |     |       |      |
| Total jitter at 2.5 Gbps (Gen1)                                   | Compliance pattern | —      | —   | 0.25  | —      | —   | 0.25  | —      | —   | 0.25  | UI   |
| PCIe Receiver Jitter Tolerance <sup>(3)</sup>                     |                    |        |     |       |        |     |       |        |     |       |      |
| Total jitter at 2.5 Gbps (Gen1)                                   | Compliance pattern | > 0.6  |     |       | > 0.6  |     |       | > 0.6  |     |       | UI   |
| GIGE Transmit Jitter Generation <sup>(4)</sup>                    |                    |        |     |       |        |     |       |        |     |       |      |
| Deterministic jitter (peak-to-peak)                               | Pattern = CRPAT    | —      | —   | 0.14  | —      | —   | 0.14  | —      | —   | 0.14  | UI   |
| Total jitter (peak-to-peak)                                       | Pattern = CRPAT    | —      | —   | 0.279 | —      | —   | 0.279 | —      | —   | 0.279 | UI   |
| GIGE Receiver Jitter Tolerance <sup>(4)</sup>                     |                    |        |     |       |        |     |       |        |     |       |      |
| Deterministic jitter tolerance (peak-to-peak)                     | Pattern = CJPAT    | > 0.4  |     |       | > 0.4  |     |       | > 0.4  |     |       | UI   |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Pattern = CJPAT    | > 0.66 |     |       | > 0.66 |     |       | > 0.66 |     |       | UI   |

**Notes to Table 1–23:**

- (1) Dedicated `refclk` pins were used to drive the input reference clocks.
- (2) The jitter numbers specified are valid for the stated conditions only.
- (3) The jitter numbers for PIPE are compliant to the PCIe Base Specification 2.0.
- (4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.

## Core Performance Specifications

The following sections describe the clock tree specifications, PLLs, embedded multiplier, memory block, and configuration specifications for Cyclone IV Devices.

### Clock Tree Specifications

Table 1–24 lists the clock tree specifications for Cyclone IV devices.

**Table 1–24. Clock Tree Performance for Cyclone IV Devices (Part 1 of 2)**

| Device  | Performance |       |     |                    |                    |       |                    |     | Unit |
|---------|-------------|-------|-----|--------------------|--------------------|-------|--------------------|-----|------|
|         | C6          | C7    | C8  | C8L <sup>(1)</sup> | C9L <sup>(1)</sup> | I7    | I8L <sup>(1)</sup> | A7  |      |
| EP4CE6  | 500         | 437.5 | 402 | 362                | 265                | 437.5 | 362                | 402 | MHz  |
| EP4CE10 | 500         | 437.5 | 402 | 362                | 265                | 437.5 | 362                | 402 | MHz  |
| EP4CE15 | 500         | 437.5 | 402 | 362                | 265                | 437.5 | 362                | 402 | MHz  |
| EP4CE22 | 500         | 437.5 | 402 | 362                | 265                | 437.5 | 362                | 402 | MHz  |
| EP4CE30 | 500         | 437.5 | 402 | 362                | 265                | 437.5 | 362                | 402 | MHz  |
| EP4CE40 | 500         | 437.5 | 402 | 362                | 265                | 437.5 | 362                | 402 | MHz  |

 For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interfaces Handbook*.

 Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specifications

Table 1–31 through Table 1–36 list the high-speed I/O timing for Cyclone IV devices. For definitions of high-speed timing specifications, refer to “Glossary” on page 1–37.

**Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices <sup>(1)</sup>, <sup>(2)</sup>, <sup>(4)</sup> (Part 1 of 2)**

| Symbol                                        | Modes                                         | C6  |     |     | C7, I7 |     |       | C8, A7 |     |       | C8L, I8L |     |       | C9L |     |       | Unit |
|-----------------------------------------------|-----------------------------------------------|-----|-----|-----|--------|-----|-------|--------|-----|-------|----------|-----|-------|-----|-----|-------|------|
|                                               |                                               | Min | Typ | Max | Min    | Typ | Max   | Min    | Typ | Max   | Min      | Typ | Max   | Min | Typ | Max   |      |
| $f_{\text{HSCLK}}$<br>(input clock frequency) | ×10                                           | 5   | —   | 180 | 5      | —   | 155.5 | 5      | —   | 155.5 | 5        | —   | 155.5 | 5   | —   | 132.5 | MHz  |
|                                               | ×8                                            | 5   | —   | 180 | 5      | —   | 155.5 | 5      | —   | 155.5 | 5        | —   | 155.5 | 5   | —   | 132.5 | MHz  |
|                                               | ×7                                            | 5   | —   | 180 | 5      | —   | 155.5 | 5      | —   | 155.5 | 5        | —   | 155.5 | 5   | —   | 132.5 | MHz  |
|                                               | ×4                                            | 5   | —   | 180 | 5      | —   | 155.5 | 5      | —   | 155.5 | 5        | —   | 155.5 | 5   | —   | 132.5 | MHz  |
|                                               | ×2                                            | 5   | —   | 180 | 5      | —   | 155.5 | 5      | —   | 155.5 | 5        | —   | 155.5 | 5   | —   | 132.5 | MHz  |
|                                               | ×1                                            | 5   | —   | 360 | 5      | —   | 311   | 5      | —   | 311   | 5        | —   | 311   | 5   | —   | 265   | MHz  |
| Device operation in Mbps                      | ×10                                           | 100 | —   | 360 | 100    | —   | 311   | 100    | —   | 311   | 100      | —   | 311   | 100 | —   | 265   | Mbps |
|                                               | ×8                                            | 80  | —   | 360 | 80     | —   | 311   | 80     | —   | 311   | 80       | —   | 311   | 80  | —   | 265   | Mbps |
|                                               | ×7                                            | 70  | —   | 360 | 70     | —   | 311   | 70     | —   | 311   | 70       | —   | 311   | 70  | —   | 265   | Mbps |
|                                               | ×4                                            | 40  | —   | 360 | 40     | —   | 311   | 40     | —   | 311   | 40       | —   | 311   | 40  | —   | 265   | Mbps |
|                                               | ×2                                            | 20  | —   | 360 | 20     | —   | 311   | 20     | —   | 311   | 20       | —   | 311   | 20  | —   | 265   | Mbps |
|                                               | ×1                                            | 10  | —   | 360 | 10     | —   | 311   | 10     | —   | 311   | 10       | —   | 311   | 10  | —   | 265   | Mbps |
| $t_{\text{DUTY}}$                             | —                                             | 45  | —   | 55  | 45     | —   | 55    | 45     | —   | 55    | 45       | —   | 55    | 45  | —   | 55    | %    |
| Transmitter channel-to-channel skew (TCCS)    | —                                             | —   | —   | 200 | —      | —   | 200   | —      | —   | 200   | —        | —   | 200   | —   | —   | 200   | ps   |
| Output jitter (peak to peak)                  | —                                             | —   | —   | 500 | —      | —   | 500   | —      | —   | 550   | —        | —   | 600   | —   | —   | 700   | ps   |
| $t_{\text{RISE}}$                             | 20 – 80%,<br>$C_{\text{LOAD}} = 5 \text{ pF}$ | —   | 500 | —   | —      | 500 | —     | —      | 500 | —     | —        | 500 | —     | —   | 500 | —     | ps   |
| $t_{\text{FALL}}$                             | 20 – 80%,<br>$C_{\text{LOAD}} = 5 \text{ pF}$ | —   | 500 | —   | —      | 500 | —     | —      | 500 | —     | —        | 500 | —     | —   | 500 | —     | ps   |

**Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices <sup>(1), (3)</sup> (Part 2 of 2)**

| Symbol                           | Modes | C6  |     | C7, I7 |     | C8, A7 |     | C8L, I8L |     | C9L |     | Unit |
|----------------------------------|-------|-----|-----|--------|-----|--------|-----|----------|-----|-----|-----|------|
|                                  |       | Min | Max | Min    | Max | Min    | Max | Min      | Max | Min | Max |      |
| t <sub>DUTY</sub>                | —     | 45  | 55  | 45     | 55  | 45     | 55  | 45       | 55  | 45  | 55  | %    |
| TCCS                             | —     | —   | 200 | —      | 200 | —      | 200 | —        | 200 | —   | 200 | ps   |
| Output jitter (peak to peak)     | —     | —   | 500 | —      | 500 | —      | 550 | —        | 600 | —   | 700 | ps   |
| t <sub>LOCK</sub> <sup>(2)</sup> | —     | —   | 1   | —      | 1   | —      | 1   | —        | 1   | —   | 1   | ms   |

**Notes to Table 1–35:**

- (1) Cyclone IV E—emulated LVDS transmitter is supported at the output pin of all I/O Banks.  
Cyclone IV GX—emulated LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2) t<sub>LOCK</sub> is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

**Table 1–36. LVDS Receiver Timing Specifications for Cyclone IV Devices <sup>(1), (3)</sup>**

| Symbol                                    | Modes | C6  |       | C7, I7 |       | C8, A7 |       | C8L, I8L |     | C9L |     | Unit |
|-------------------------------------------|-------|-----|-------|--------|-------|--------|-------|----------|-----|-----|-----|------|
|                                           |       | Min | Max   | Min    | Max   | Min    | Max   | Min      | Max | Min | Max |      |
| f <sub>HCLK</sub> (input clock frequency) | ×10   | 10  | 437.5 | 10     | 370   | 10     | 320   | 10       | 320 | 10  | 250 | MHz  |
|                                           | ×8    | 10  | 437.5 | 10     | 370   | 10     | 320   | 10       | 320 | 10  | 250 | MHz  |
|                                           | ×7    | 10  | 437.5 | 10     | 370   | 10     | 320   | 10       | 320 | 10  | 250 | MHz  |
|                                           | ×4    | 10  | 437.5 | 10     | 370   | 10     | 320   | 10       | 320 | 10  | 250 | MHz  |
|                                           | ×2    | 10  | 437.5 | 10     | 370   | 10     | 320   | 10       | 320 | 10  | 250 | MHz  |
|                                           | ×1    | 10  | 437.5 | 10     | 402.5 | 10     | 402.5 | 10       | 362 | 10  | 265 | MHz  |
| HSIODR                                    | ×10   | 100 | 875   | 100    | 740   | 100    | 640   | 100      | 640 | 100 | 500 | Mbps |
|                                           | ×8    | 80  | 875   | 80     | 740   | 80     | 640   | 80       | 640 | 80  | 500 | Mbps |
|                                           | ×7    | 70  | 875   | 70     | 740   | 70     | 640   | 70       | 640 | 70  | 500 | Mbps |
|                                           | ×4    | 40  | 875   | 40     | 740   | 40     | 640   | 40       | 640 | 40  | 500 | Mbps |
|                                           | ×2    | 20  | 875   | 20     | 740   | 20     | 640   | 20       | 640 | 20  | 500 | Mbps |
|                                           | ×1    | 10  | 437.5 | 10     | 402.5 | 10     | 402.5 | 10       | 362 | 10  | 265 | Mbps |
| SW                                        | —     | —   | 400   | —      | 400   | —      | 400   | —        | 550 | —   | 640 | ps   |
| Input jitter tolerance                    | —     | —   | 500   | —      | 500   | —      | 550   | —        | 600 | —   | 700 | ps   |
| t <sub>LOCK</sub> <sup>(2)</sup>          | —     | —   | 1     | —      | 1     | —      | 1     | —        | 1   | —   | 1   | ms   |

**Notes to Table 1–36:**

- (1) Cyclone IV E—LVDS receiver is supported at all I/O Banks.  
Cyclone IV GX—LVDS receiver is supported at I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2) t<sub>LOCK</sub> is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

## External Memory Interface Specifications

The external memory interfaces for Cyclone IV devices are auto-calibrating and easy to implement.

For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interface Handbook*.

Table 1–37 lists the memory output clock jitter specifications for Cyclone IV devices.

**Table 1–37. Memory Output Clock Jitter Specifications for Cyclone IV Devices <sup>(1), (2)</sup>**

| Parameter                    | Symbol          | Min  | Max | Unit |
|------------------------------|-----------------|------|-----|------|
| Clock period jitter          | $t_{JIT(per)}$  | –125 | 125 | ps   |
| Cycle-to-cycle period jitter | $t_{JIT(cc)}$   | –200 | 200 | ps   |
| Duty cycle jitter            | $t_{JIT(duty)}$ | –150 | 150 | ps   |

**Notes to Table 1–37:**

- (1) Memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2 standard.
- (2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock (GCLK) network.

## Duty Cycle Distortion Specifications

Table 1–38 lists the worst case duty cycle distortion for Cyclone IV devices.

**Table 1–38. Duty Cycle Distortion on Cyclone IV Devices I/O Pins <sup>(1), (2), (3)</sup>**

| Symbol            | C6  |     | C7, I7 |     | C8, I8L, A7 |     | C9L |     | Unit |
|-------------------|-----|-----|--------|-----|-------------|-----|-----|-----|------|
|                   | Min | Max | Min    | Max | Min         | Max | Min | Max |      |
| Output Duty Cycle | 45  | 55  | 45     | 55  | 45          | 55  | 45  | 55  | %    |

**Notes to Table 1–38:**

- (1) The duty cycle distortion specification applies to clock outputs from the PLLs, global clock tree, and IOE driving the dedicated and general purpose I/O pins.
- (2) Cyclone IV devices meet the specified duty cycle distortion at the maximum output toggle rate for each combination of I/O standard and current strength.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

## OCT Calibration Timing Specification

Table 1–39 lists the duration of calibration for series OCT with calibration at device power-up for Cyclone IV devices.

**Table 1–39. Timing Specification for Series OCT with Calibration at Device Power-Up for Cyclone IV Devices <sup>(1)</sup>**

| Symbol       | Description                                                | Maximum | Units   |
|--------------|------------------------------------------------------------|---------|---------|
| $t_{OCTCAL}$ | Duration of series OCT with calibration at device power-up | 20      | $\mu$ s |

**Note to Table 1–39:**

- (1) OCT calibration takes place after device configuration and before entering user mode.



Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

**Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices <sup>(1), (2)</sup>**

| Parameter                                                       | Paths Affected              | Number of Setting | Min Offset | Max Offset  |       |       |             |       |       |       |       | Unit |
|-----------------------------------------------------------------|-----------------------------|-------------------|------------|-------------|-------|-------|-------------|-------|-------|-------|-------|------|
|                                                                 |                             |                   |            | Fast Corner |       |       | Slow Corner |       |       |       |       |      |
|                                                                 |                             |                   |            | C6          | I7    | A7    | C6          | C7    | C8    | I7    | A7    |      |
| Input delay from pin to internal cells                          | Pad to I/O dataout to core  | 7                 | 0          | 1.314       | 1.211 | 1.211 | 2.177       | 2.340 | 2.433 | 2.388 | 2.508 | ns   |
| Input delay from pin to input register                          | Pad to I/O input register   | 8                 | 0          | 1.307       | 1.203 | 1.203 | 2.19        | 2.387 | 2.540 | 2.430 | 2.545 | ns   |
| Delay from output register to output pin                        | I/O output register to pad  | 2                 | 0          | 0.437       | 0.402 | 0.402 | 0.747       | 0.820 | 0.880 | 0.834 | 0.873 | ns   |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12                | 0          | 0.693       | 0.665 | 0.665 | 1.200       | 1.379 | 1.532 | 1.393 | 1.441 | ns   |

**Notes to Table 1–42:**

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices <sup>(1), (2)</sup>**

| Parameter                                                       | Paths Affected              | Number of Setting | Min Offset | Max Offset  |       |       |             |       |       |       |       | Unit |
|-----------------------------------------------------------------|-----------------------------|-------------------|------------|-------------|-------|-------|-------------|-------|-------|-------|-------|------|
|                                                                 |                             |                   |            | Fast Corner |       |       | Slow Corner |       |       |       |       |      |
|                                                                 |                             |                   |            | C6          | I7    | A7    | C6          | C7    | C8    | I7    | A7    |      |
| Input delay from pin to internal cells                          | Pad to I/O dataout to core  | 7                 | 0          | 1.314       | 1.209 | 1.209 | 2.201       | 2.386 | 2.510 | 2.429 | 2.548 | ns   |
| Input delay from pin to input register                          | Pad to I/O input register   | 8                 | 0          | 1.312       | 1.207 | 1.207 | 2.202       | 2.402 | 2.558 | 2.447 | 2.557 | ns   |
| Delay from output register to output pin                        | I/O output register to pad  | 2                 | 0          | 0.458       | 0.419 | 0.419 | 0.783       | 0.861 | 0.924 | 0.875 | 0.915 | ns   |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12                | 0          | 0.686       | 0.657 | 0.657 | 1.185       | 1.360 | 1.506 | 1.376 | 1.422 | ns   |

**Notes to Table 1–43:**

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

**Table 1–44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices <sup>(1), (2)</sup>**

| Parameter                                                       | Paths Affected              | Number of Settings | Min Offset | Max Offset  |       |             |       |       |       | Unit |
|-----------------------------------------------------------------|-----------------------------|--------------------|------------|-------------|-------|-------------|-------|-------|-------|------|
|                                                                 |                             |                    |            | Fast Corner |       | Slow Corner |       |       |       |      |
|                                                                 |                             |                    |            | C6          | I7    | C6          | C7    | C8    | I7    |      |
| Input delay from pin to internal cells                          | Pad to I/O dataout to core  | 7                  | 0          | 1.313       | 1.209 | 2.184       | 2.336 | 2.451 | 2.387 | ns   |
| Input delay from pin to input register                          | Pad to I/O input register   | 8                  | 0          | 1.312       | 1.208 | 2.200       | 2.399 | 2.554 | 2.446 | ns   |
| Delay from output register to output pin                        | I/O output register to pad  | 2                  | 0          | 0.438       | 0.404 | 0.751       | 0.825 | 0.886 | 0.839 | ns   |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12                 | 0          | 0.713       | 0.682 | 1.228       | 1.41  | 1.566 | 1.424 | ns   |

**Notes to Table 1–44:**

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices <sup>(1), (2)</sup>**

| Parameter                                                       | Paths Affected              | Number of Settings | Min Offset | Max Offset  |       |             |       |       |       | Unit |
|-----------------------------------------------------------------|-----------------------------|--------------------|------------|-------------|-------|-------------|-------|-------|-------|------|
|                                                                 |                             |                    |            | Fast Corner |       | Slow Corner |       |       |       |      |
|                                                                 |                             |                    |            | C6          | I7    | C6          | C7    | C8    | I7    |      |
| Input delay from pin to internal cells                          | Pad to I/O dataout to core  | 7                  | 0          | 1.314       | 1.210 | 2.209       | 2.398 | 2.526 | 2.443 | ns   |
| Input delay from pin to input register                          | Pad to I/O input register   | 8                  | 0          | 1.313       | 1.208 | 2.205       | 2.406 | 2.563 | 2.450 | ns   |
| Delay from output register to output pin                        | I/O output register to pad  | 2                  | 0          | 0.461       | 0.421 | 0.789       | 0.869 | 0.933 | 0.884 | ns   |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12                 | 0          | 0.712       | 0.682 | 1.225       | 1.407 | 1.562 | 1.421 | ns   |

**Notes to Table 1–45:**

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software

## I/O Timing

Use the following methods to determine I/O timing:

- the Excel-based I/O Timing
- the Quartus II timing analyzer

The Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get a timing budget estimation as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.



The Excel-based I/O Timing spreadsheet is downloadable from Cyclone IV Devices Literature website.

## Glossary

Table 1-46 lists the glossary for this chapter.

**Table 1-46. Glossary (Part 1 of 5)**

| Letter | Term                                                   | Definitions                                                                                                                                                                                                                                                            |
|--------|--------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A      | —                                                      | —                                                                                                                                                                                                                                                                      |
| B      | —                                                      | —                                                                                                                                                                                                                                                                      |
| C      | —                                                      | —                                                                                                                                                                                                                                                                      |
| D      | —                                                      | —                                                                                                                                                                                                                                                                      |
| E      | —                                                      | —                                                                                                                                                                                                                                                                      |
| F      | $f_{\text{HSCLK}}$                                     | High-speed I/O block: High-speed receiver/transmitter input and output clock frequency.                                                                                                                                                                                |
| G      | GCLK                                                   | Input pin directly to Global Clock network.                                                                                                                                                                                                                            |
|        | GCLK PLL                                               | Input pin to Global Clock network through the PLL.                                                                                                                                                                                                                     |
| H      | HSIODR                                                 | High-speed I/O block: Maximum/minimum LVDS data transfer rate ( $\text{HSIODR} = 1/\text{TUI}$ ).                                                                                                                                                                      |
| I      | Input Waveforms for the SSTL Differential I/O Standard | <p>The diagram shows a differential signal waveform. The signal transitions between <math>V_{\text{IH}}</math> and <math>V_{\text{IL}}</math>, with a swing of <math>V_{\text{SWING}}</math>. The reference voltage <math>V_{\text{REF}}</math> is also indicated.</p> |

## Document Revision History

Table 1–47 lists the revision history for this chapter.

**Table 1–47. Document Revision History**

| Date          | Version | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| March 2016    | 2.0     | Updated note (5) in Table 1–21 to remove support for the N148 package.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| October 2014  | 1.9     | Updated maximum value for $V_{CCD\_PLL}$ in Table 1–1.<br>Removed extended temperature note in Table 1–3.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| December 2013 | 1.8     | Updated Table 1–21 by adding Note (15).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| May 2013      | 1.7     | Updated Table 1–15 by adding Note (4).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| October 2012  | 1.6     | <ul style="list-style-type: none"> <li>■ Updated the maximum value for <math>V_I</math>, <math>V_{CCD\_PLL}</math>, <math>V_{CCIO}</math>, <math>V_{CC\_CLKIN}</math>, <math>V_{CCH\_GXB}</math>, and <math>V_{CCA\_GXB}</math> in Table 1–1.</li> <li>■ Updated Table 1–11 and Table 1–22.</li> <li>■ Updated Table 1–21 to include peak-to-peak differential input voltage for the Cyclone IV GX transceiver input reference clock.</li> <li>■ Updated Table 1–29 to include the typical <math>DCLK</math> value.</li> <li>■ Updated the minimum <math>f_{HCLK}</math> value in Table 1–31, Table 1–32, Table 1–33, Table 1–34, and Table 1–35.</li> </ul> |
| November 2011 | 1.5     | <ul style="list-style-type: none"> <li>■ Updated “Maximum Allowed Overshoot or Undershoot Voltage”, “Operating Conditions”, and “PLL Specifications” sections.</li> <li>■ Updated Table 1–2, Table 1–3, Table 1–4, Table 1–5, Table 1–8, Table 1–9, Table 1–15, Table 1–18, Table 1–19, and Table 1–21.</li> <li>■ Updated Figure 1–1.</li> </ul>                                                                                                                                                                                                                                                                                                            |
| December 2010 | 1.4     | <ul style="list-style-type: none"> <li>■ Updated for the Quartus II software version 10.1 release.</li> <li>■ Updated Table 1–21 and Table 1–25.</li> <li>■ Minor text edits.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| July 2010     | 1.3     | <p>Updated for the Quartus II software version 10.0 release:</p> <ul style="list-style-type: none"> <li>■ Updated Table 1–3, Table 1–4, Table 1–21, Table 1–25, Table 1–28, Table 1–30, Table 1–40, Table 1–41, Table 1–42, Table 1–43, Table 1–44, and Table 1–45.</li> <li>■ Updated Figure 1–2 and Figure 1–3.</li> <li>■ Removed SW Requirement and TCCS for Cyclone IV Devices tables.</li> <li>■ Minor text edits.</li> </ul>                                                                                                                                                                                                                          |
| March 2010    | 1.2     | <p>Updated to include automotive devices:</p> <ul style="list-style-type: none"> <li>■ Updated the “Operating Conditions” and “PLL Specifications” sections.</li> <li>■ Updated Table 1–1, Table 1–8, Table 1–9, Table 1–21, Table 1–26, Table 1–27, Table 1–31, Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–36, Table 1–37, Table 1–38, Table 1–40, Table 1–42, and Table 1–43.</li> <li>■ Added Table 1–5 to include ESD for Cyclone IV devices GPIOs and HSSI I/Os.</li> <li>■ Added Table 1–44 and Table 1–45 to include IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.</li> <li>■ Minor text edits.</li> </ul>         |

**Table 1–47. Document Revision History**

| Date          | Version | Changes                                                                                                                                                                                                                                       |
|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| February 2010 | 1.1     | <ul style="list-style-type: none"><li>■ Updated Table 1–3 through Table 1–44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release.</li><li>■ Minor text edits.</li></ul> |
| November 2009 | 1.0     | Initial release.                                                                                                                                                                                                                              |