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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	900
Number of Logic Elements/Cells	14400
Total RAM Bits	552960
Number of I/O	72
Number of Gates	-
Voltage - Supply	1.16V ~ 1.24V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	169-LBGA
Supplier Device Package	169-FBGA (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep4cgx15bf14c8">https://www.e-xfl.com/product-detail/intel/ep4cgx15bf14c8</a>



Cyclone IV E industrial devices I7 are offered with extended operating temperature range.

## Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone IV devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Table 1–1 lists the absolute maximum ratings for Cyclone IV devices.



Conditions beyond those listed in Table 1–1 cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time have adverse effects on the device.

**Table 1–1. Absolute Maximum Ratings for Cyclone IV Devices <sup>(1)</sup>**


Symbol	Parameter	Min	Max	Unit
$V_{CCINT}$	Core voltage, PCI Express® (PCIe®) hard IP block, and transceiver physical coding sublayer (PCS) power supply	–0.5	1.8	V
$V_{CCA}$	Phase-locked loop (PLL) analog power supply	–0.5	3.75	V
$V_{CCD\_PLL}$	PLL digital power supply	–0.5	1.8	V
$V_{CCIO}$	I/O banks power supply	–0.5	3.75	V
$V_{CC\_CLKIN}$	Differential clock input pins power supply	–0.5	4.5	V
$V_{CCH\_GXB}$	Transceiver output buffer power supply	–0.5	3.75	V
$V_{CCA\_GXB}$	Transceiver physical medium attachment (PMA) and auxiliary power supply	–0.5	3.75	V
$V_{CCL\_GXB}$	Transceiver PMA and auxiliary power supply	–0.5	1.8	V
$V_I$	DC input voltage	–0.5	4.2	V
$I_{OUT}$	DC output current, per pin	–25	40	mA
$T_{STG}$	Storage temperature	–65	150	°C
$T_J$	Operating junction temperature	–40	125	°C

**Note to Table 1–1:**

(1) Supply voltage specifications apply to voltage readings taken at the device pins with respect to ground, not at the power supply.

## Maximum Allowed Overshoot or Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to –2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns. Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device.

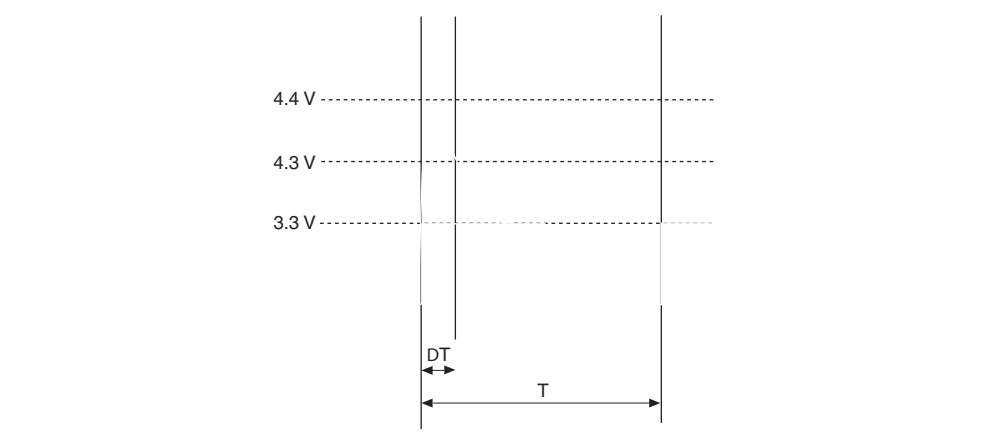
 A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

**Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices**

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit
$V_i$	AC Input Voltage	$V_i = 4.20$	100	%
		$V_i = 4.25$	98	%
		$V_i = 4.30$	65	%
		$V_i = 4.35$	43	%
		$V_i = 4.40$	29	%
		$V_i = 4.45$	20	%
		$V_i = 4.50$	13	%
		$V_i = 4.55$	9	%
		$V_i = 4.60$	6	%

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as  $([\Delta T]/T) \times 100$ . This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

**Figure 1–1. Cyclone IV Devices Overshoot Duration**



**Table 1-4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CCA\_GXB}$	Transceiver PMA and auxiliary power supply	—	2.375	2.5	2.625	V
$V_{CCL\_GXB}$	Transceiver PMA and auxiliary power supply	—	1.16	1.2	1.24	V
$V_I$	DC input voltage	—	-0.5	—	3.6	V
$V_O$	DC output voltage	—	0	—	$V_{CCIO}$	V
$T_J$	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	-40	—	100	°C
$t_{RAMP}$	Power supply ramp time	Standard power-on reset (POR) <sup>(7)</sup>	50 $\mu$ s	—	50 ms	—
		Fast POR <sup>(8)</sup>	50 $\mu$ s	—	3 ms	—
$I_{Diode}$	Magnitude of DC current across PCI-clamp diode when enabled	—	—	—	10	mA

**Notes to Table 1-4:**

- (1) All  $V_{CCA}$  pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- (2) You must connect  $V_{CCD\_PLL}$  to  $V_{CCINT}$  through a decoupling capacitor and ferrite bead.
- (3) Power supplies must rise monotonically.
- (4)  $V_{CCIO}$  for all I/O banks must be powered up during device operation. Configurations pins are powered up by  $V_{CCIO}$  of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support  $V_{CCIO}$  of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the  $V_{CCIO}$  level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.
- (5) You must set  $V_{CC\_CLKIN}$  to 2.5 V if you use  $CLKIN$  as a high-speed serial interface (HSSI)  $refclk$  or as a  $DIFFCLK$  input.
- (6) The  $CLKIN$  pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.
- (7) The POR time for Standard POR ranges between 50 and 200 ms.  $V_{CCINT}$ ,  $V_{CCA}$ , and  $V_{CCIO}$  of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.
- (8) The POR time for Fast POR ranges between 3 and 9 ms.  $V_{CCINT}$ ,  $V_{CCA}$ , and  $V_{CCIO}$  of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

## ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1-5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

**Table 1-5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os**

Symbol	Parameter	Passing Voltage	Unit
$V_{ESDHBM}$	ESD voltage using the HBM (GPIOs) <sup>(1)</sup>	$\pm 2000$	V
	ESD using the HBM (HSSI I/Os) <sup>(2)</sup>	$\pm 1000$	V
$V_{ESDCDM}$	ESD using the CDM (GPIOs)	$\pm 500$	V
	ESD using the CDM (HSSI I/Os) <sup>(2)</sup>	$\pm 250$	V

**Notes to Table 1-5:**

- (1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is  $\pm 1000$ V.
- (2) This value is applicable only to Cyclone IV GX devices.

Example 1–1 shows how to calculate the change of 50-Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

#### Example 1–1. Impedance Change

$$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$$

$$\Delta R_T = (85 - 25) \times 0.262 = 15.72$$

Because  $\Delta R_V$  is negative,

$$MF_V = 1 / (3.83/100 + 1) = 0.963$$

Because  $\Delta R_T$  is positive,

$$MF_T = 15.72/100 + 1 = 1.157$$

$$MF = 0.963 \times 1.157 = 1.114$$

$$R_{\text{final}} = 50 \times 1.114 = 55.71 \, \Omega$$

## Pin Capacitance

Table 1–11 lists the pin capacitance for Cyclone IV devices.

**Table 1–11. Pin Capacitance for Cyclone IV Devices <sup>(1)</sup>**

Symbol	Parameter	Typical – Quad Flat Pack (QFP)	Typical – Quad Flat No Leads (QFN)	Typical – Ball-Grid Array (BGA)	Unit
C <sub>IOTB</sub>	Input capacitance on top and bottom I/O pins	7	7	6	pF
C <sub>IOLR</sub>	Input capacitance on right I/O pins	7	7	5	pF
C <sub>LVDSLR</sub>	Input capacitance on right I/O pins with dedicated LVDS output	8	8	7	pF
C <sub>VREFLR</sub> (2)	Input capacitance on right dual-purpose V <sub>REF</sub> pin when used as V <sub>REF</sub> or user I/O pin	21	21	21	pF
C <sub>VREFTB</sub> (2)	Input capacitance on top and bottom dual-purpose V <sub>REF</sub> pin when used as V <sub>REF</sub> or user I/O pin	23 (3)	23	23	pF
C <sub>CLKTB</sub>	Input capacitance on top and bottom dedicated clock input pins	7	7	6	pF
C <sub>CLKLR</sub>	Input capacitance on right dedicated clock input pins	6	6	5	pF

#### Notes to Table 1–11:

- (1) The pin capacitance applies to FBGA, UBGA, and MBGA packages.
- (2) When you use the V<sub>REF</sub> pin as a regular input or output, you can expect a reduced performance of toggle rate and t<sub>CO</sub> because of higher pin capacitance.
- (3) C<sub>VREFTB</sub> for the EP4CE22 device is 30 pF.

## Schmitt Trigger Input

Cyclone IV devices support Schmitt trigger input on the TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF\_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rate. Table 1–14 lists the hysteresis specifications across the supported  $V_{CCIO}$  range for Schmitt trigger inputs in Cyclone IV devices.

**Table 1–14. Hysteresis Specifications for Schmitt Trigger Input in Cyclone IV Devices**

Symbol	Parameter	Conditions (V)	Minimum	Unit
$V_{SCHMITT}$	Hysteresis for Schmitt trigger input	$V_{CCIO} = 3.3$	200	mV
		$V_{CCIO} = 2.5$	200	mV
		$V_{CCIO} = 1.8$	140	mV
		$V_{CCIO} = 1.5$	110	mV

## I/O Standard Specifications

The following tables list input voltage sensitivities ( $V_{IH}$  and  $V_{IL}$ ), output voltage ( $V_{OH}$  and  $V_{OL}$ ), and current drive characteristics ( $I_{OH}$  and  $I_{OL}$ ), for various I/O standards supported by Cyclone IV devices. Table 1–15 through Table 1–20 provide the I/O standard specifications for Cyclone IV devices.

**Table 1–15. Single-Ended I/O Standard Specifications for Cyclone IV Devices <sup>(1), (2)</sup>**

I/O Standard	$V_{CCIO}$ (V)			$V_{IL}$ (V)		$V_{IH}$ (V)		$V_{OL}$ (V)	$V_{OH}$ (V)	$I_{OL}$ (mA) (4)	$I_{OH}$ (mA) (4)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTTL <sup>(3)</sup>	3.135	3.3	3.465	—	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS <sup>(3)</sup>	3.135	3.3	3.465	—	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	2	–2
3.0-V LVTTTL <sup>(3)</sup>	2.85	3.0	3.15	–0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.45	2.4	4	–4
3.0-V LVCMOS <sup>(3)</sup>	2.85	3.0	3.15	–0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.2	$V_{CCIO} - 0.2$	0.1	–0.1
2.5 V <sup>(3)</sup>	2.375	2.5	2.625	–0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.4	2.0	1	–1
1.8 V	1.71	1.8	1.89	–0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	2.25	0.45	$V_{CCIO} - 0.45$	2	–2
1.5 V	1.425	1.5	1.575	–0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	–2
1.2 V	1.14	1.2	1.26	–0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	–2
3.0-V PCI	2.85	3.0	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	–0.5
3.0-V PCI-X	2.85	3.0	3.15	—	$0.35 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	–0.5

**Notes to Table 1–15:**

- (1) For voltage-referenced receiver input waveform and explanation of terms used in Table 1–15, refer to “Glossary” on page 1–37.
- (2) AC load  $CL = 10$  pF
- (3) For more information about interfacing Cyclone IV devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O standards, refer to *AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O Systems*.
- (4) To meet the  $I_{OL}$  and  $I_{OH}$  specifications, you must set the current strength settings accordingly. For example, to meet the **3.3-V LVTTTL** specification (4 mA), set the current strength settings to 4 mA or higher. Setting at lower current strength may not meet the  $I_{OL}$  and  $I_{OH}$  specifications in the handbook.

**Table 1-16. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Cyclone IV Devices <sup>(1)</sup>**

I/O Standard	V <sub>CCIO</sub> (V)			V <sub>REF</sub> (V)			V <sub>TT</sub> (V) <sup>(2)</sup>		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V <sub>REF</sub> - 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V <sub>REF</sub> - 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 × V <sub>CCIO</sub> <sup>(3)</sup>	0.5 × V <sub>CCIO</sub> <sup>(3)</sup>	0.52 × V <sub>CCIO</sub> <sup>(3)</sup>	—	0.5 × V <sub>CCIO</sub>	—
				0.47 × V <sub>CCIO</sub> <sup>(4)</sup>	0.5 × V <sub>CCIO</sub> <sup>(4)</sup>	0.53 × V <sub>CCIO</sub> <sup>(4)</sup>			

**Notes to Table 1-16:**

- (1) For an explanation of terms used in Table 1-16, refer to “Glossary” on page 1-37.
- (2) V<sub>TT</sub> of the transmitting device must track V<sub>REF</sub> of the receiving device.
- (3) Value shown refers to DC input reference voltage, V<sub>REF(DC)</sub>.
- (4) Value shown refers to AC input reference voltage, V<sub>REF(AC)</sub>.

**Table 1-17. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone IV Devices**

I/O Standard	V <sub>IL(DC)</sub> (V)		V <sub>IH(DC)</sub> (V)		V <sub>IL(AC)</sub> (V)		V <sub>IH(AC)</sub> (V)		V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	I <sub>OL</sub> (mA)	I <sub>OH</sub> (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V <sub>REF</sub> - 0.18	V <sub>REF</sub> + 0.18	—	—	V <sub>REF</sub> - 0.35	V <sub>REF</sub> + 0.35	—	V <sub>TT</sub> - 0.57	V <sub>TT</sub> + 0.57	8.1	-8.1
SSTL-2 Class II	—	V <sub>REF</sub> - 0.18	V <sub>REF</sub> + 0.18	—	—	V <sub>REF</sub> - 0.35	V <sub>REF</sub> + 0.35	—	V <sub>TT</sub> - 0.76	V <sub>TT</sub> + 0.76	16.4	-16.4
SSTL-18 Class I	—	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125	—	—	V <sub>REF</sub> - 0.25	V <sub>REF</sub> + 0.25	—	V <sub>TT</sub> - 0.475	V <sub>TT</sub> + 0.475	6.7	-6.7
SSTL-18 Class II	—	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125	—	—	V <sub>REF</sub> - 0.25	V <sub>REF</sub> + 0.25	—	0.28	V <sub>CCIO</sub> - 0.28	13.4	-13.4
HSTL-18 Class I	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	—	0.4	V <sub>CCIO</sub> - 0.4	8	-8
HSTL-18 Class II	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	—	0.4	V <sub>CCIO</sub> - 0.4	16	-16
HSTL-15 Class I	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	—	0.4	V <sub>CCIO</sub> - 0.4	8	-8
HSTL-15 Class II	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	—	0.4	V <sub>CCIO</sub> - 0.4	16	-16
HSTL-12 Class I	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	-0.24	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	V <sub>CCIO</sub> + 0.24	0.25 × V <sub>CCIO</sub>	0.75 × V <sub>CCIO</sub>	8	-8
HSTL-12 Class II	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	-0.24	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	V <sub>CCIO</sub> + 0.24	0.25 × V <sub>CCIO</sub>	0.75 × V <sub>CCIO</sub>	14	-14

## Transceiver Performance Specifications

Table 1-21 lists the Cyclone IV GX transceiver specifications.

**Table 1-21. Transceiver Specification for Cyclone IV GX Devices (Part 1 of 4)**

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	1.2 V PCML, 1.5 V PCML, 3.3 V PCML, Differential LVPECL, LVDS, HCSL										
Input frequency from REFCLK input pins	—	50	—	156.25	50	—	156.25	50	—	156.25	MHz
Spread-spectrum modulating clock frequency	Physical interface for PCI Express (PIPE) mode	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PIPE mode	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
Peak-to-peak differential input voltage	—	0.1	—	1.6	0.1	—	1.6	0.1	—	1.6	V
V <sub>ICM</sub> (AC coupled)	—	1100 ± 5%			1100 ± 5%			1100 ± 5%			mV
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise <sup>(1)</sup>	Frequency offset = 1 MHz – 8 MHz	—	—	–123	—	—	–123	—	—	–123	dBc/Hz
Transmitter REFCLK Total Jitter <sup>(1)</sup>		—	—	42.3	—	—	42.3	—	—	42.3	ps
R <sub>ref</sub>	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clock											
cal_blk_clk clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5/37.5 <sup>(2)</sup>	—	50	2.5/37.5 <sup>(2)</sup>	—	50	2.5/37.5 <sup>(2)</sup>	—	50	MHz
Delta time between reconfig_clk	—	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum power-down pulse width	—	—	1	—	—	1	—	—	1	—	μs



**Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 4 of 4)**

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PLD-Transceiver Interface											
Interface speed (F324 and smaller package)	—	25	—	125	25	—	125	25	—	125	MHz
Interface speed (F484 and larger package)	—	25	—	156.25	25	—	156.25	25	—	156.25	MHz
Digital reset pulse width	—	Minimum is 2 parallel clock cycles									

**Notes to Table 1–21:**

- (1) This specification is valid for transmitter output jitter specification with a maximum total jitter value of 112 ps, typically for 3.125 Gbps SRIO and XAUI protocols.
- (2) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter Only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver Only** or **Receiver and Transmitter** mode.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The rate matcher supports only up to  $\pm 300$  parts per million (ppm).
- (5) Supported for the F169 and F324 device packages only.
- (6) Supported for the F484, F672, and F896 device packages only. Pending device characterization.
- (7) To support CDR ppm tolerance greater than  $\pm 300$  ppm, implement ppm detector in user logic and configure CDR to Manual Lock Mode.
- (8) Asynchronous spread-spectrum clocking is not supported.
- (9) For the EP4CGX30 (F484 package only), EP4CGX50, and EP4CGX75 devices, the CDR ppl tolerance is  $\pm 200$  ppm.
- (10) Time taken until `p11_locked` goes high after `p11_powerdown` deasserts.
- (11) Time that the CDR must be kept in lock-to-reference mode after `rx_analogreset` deasserts and before `rx_locktodata` is asserted in manual mode.
- (12) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode (Figure 1–2), or after `rx_freqlocked` signal goes high in automatic mode (Figure 1–3).
- (13) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode.
- (14) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode.
- (15) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Figure 1-4 shows the differential receiver input waveform.

**Figure 1-4. Receiver Input Waveform**

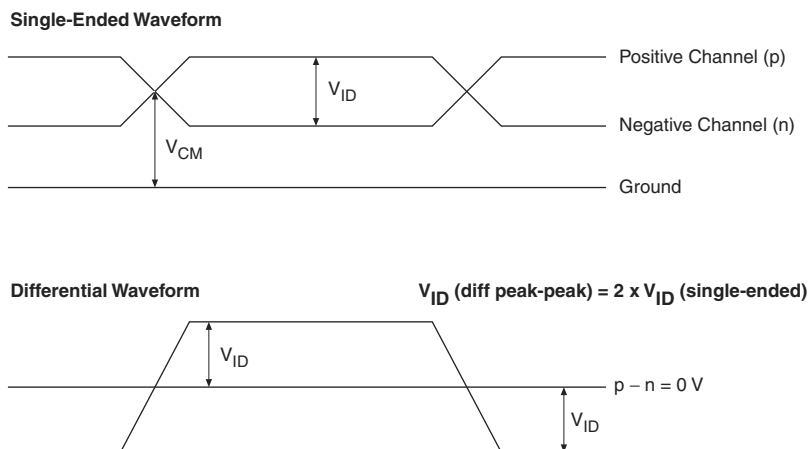


Figure 1-5 shows the transmitter output waveform.

**Figure 1-5. Transmitter Output Waveform**

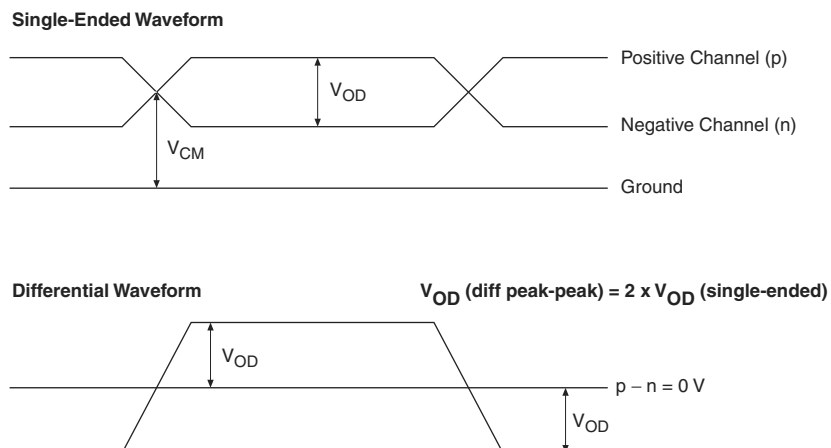


Table 1-22 lists the typical  $V_{OD}$  for Tx term that equals 100  $\Omega$ .

**Table 1-22. Typical  $V_{OD}$  Setting, Tx Term = 100  $\Omega$**

Symbol	$V_{OD}$ Setting (mV)					
	1	2	3	4 (1)	5	6
$V_{OD}$ differential peak to peak typical (mV)	400	600	800	900	1000	1200

**Note to Table 1-22:**

(1) This setting is required for compliance with the PCIe protocol.

**Table 1–24. Clock Tree Performance for Cyclone IV Devices (Part 2 of 2)**

Device	Performance								Unit
	C6	C7	C8	C8L <sup>(1)</sup>	C9L <sup>(1)</sup>	I7	I8L <sup>(1)</sup>	A7	
EP4CE55	500	437.5	402	362	265	437.5	362	—	MHz
EP4CE75	500	437.5	402	362	265	437.5	362	—	MHz
EP4CE115	—	437.5	402	362	265	437.5	362	—	MHz
EP4CGX15	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX22	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX30	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX50	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX75	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX110	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX150	500	437.5	402	—	—	437.5	—	—	MHz

**Note to Table 1–24:**

(1) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades.

## PLL Specifications

Table 1–25 lists the PLL specifications for Cyclone IV devices when operating in the commercial junction temperature range (0°C to 85°C), the industrial junction temperature range (–40°C to 100°C), the extended industrial junction temperature range (–40°C to 125°C), and the automotive junction temperature range (–40°C to 125°C). For more information about the PLL block, refer to “Glossary” on page 1–37.

**Table 1–25. PLL Specifications for Cyclone IV Devices <sup>(1), (2)</sup> (Part 1 of 2)**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{IN}$ <sup>(3)</sup>	Input clock frequency (–6, –7, –8 speed grades)	5	—	472.5	MHz
	Input clock frequency (–8L speed grade)	5	—	362	MHz
	Input clock frequency (–9L speed grade)	5	—	265	MHz
$f_{INPFD}$	PFD input frequency	5	—	325	MHz
$f_{VCO}$ <sup>(4)</sup>	PLL internal VCO operating range	600	—	1300	MHz
$f_{INDUTY}$	Input clock duty cycle	40	—	60	%
$t_{INJITTER\_CCJ}$ <sup>(5)</sup>	Input clock cycle-to-cycle jitter $F_{REF} \geq 100$ MHz	—	—	0.15	UI
	$F_{REF} < 100$ MHz	—	—	±750	ps
$f_{OUT\_EXT}$ (external clock output) <sup>(3)</sup>	PLL output frequency	—	—	472.5	MHz
$f_{OUT}$ (to global clock)	PLL output frequency (–6 speed grade)	—	—	472.5	MHz
	PLL output frequency (–7 speed grade)	—	—	450	MHz
	PLL output frequency (–8 speed grade)	—	—	402.5	MHz
	PLL output frequency (–8L speed grade)	—	—	362	MHz
	PLL output frequency (–9L speed grade)	—	—	265	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
$t_{LOCK}$	Time required to lock from end of device configuration	—	—	1	ms

**Table 1–25. PLL Specifications for Cyclone IV Devices <sup>(1), (2)</sup> (Part 2 of 2)**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{DLOCK}$	Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or $\overline{areset}$ is deasserted)	—	—	1	ms
$t_{OUTJITTER\_PERIOD\_DEDCLK}^{(6)}$	Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER\_CCJ\_DEDCLK}^{(6)}$	Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER\_PERIOD\_IO}^{(6)}$	Regular I/O period jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER\_CCJ\_IO}^{(6)}$	Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{PLL\_PSERR}$	Accuracy of PLL phase shift	—	—	$\pm 50$	ps
$t_{ARESET}$	Minimum pulse width on $\overline{areset}$ signal.	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	3.5 <sup>(7)</sup>	—	SCANCLK cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
$t_{CASC\_OUTJITTER\_PERIOD\_DEDCLK}^{(8), (9)}$	Period jitter for dedicated clock output in cascaded PLLs ( $F_{OUT} \geq 100$ MHz)	—	—	425	ps
	Period jitter for dedicated clock output in cascaded PLLs ( $F_{OUT} < 100$ MHz)	—	—	42.5	mUI

**Notes to Table 1–25:**

- (1) This table is applicable for general purpose PLLs and multipurpose PLLs.
- (2) You must connect  $V_{CCD\_PLL}$  to  $V_{CCINT}$  through the decoupling capacitor and ferrite bead.
- (3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (4) The  $V_{CO}$  frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the  $V_{CO}$  post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the  $f_{VCO}$  specification.
- (5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.
- (6) Peak-to-peak jitter with a probability level of  $10^{-12}$  (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.
- (7) With 100-MHz scanclk frequency.
- (8) The cascaded PLLs specification is applicable only with the following conditions:
  - Upstream PLL— $0.59 \text{ MHz} \leq \text{Upstream PLL bandwidth} < 1 \text{ MHz}$
  - Downstream PLL—Downstream PLL bandwidth  $> 2 \text{ MHz}$
- (9) PLL cascading is not supported for transceiver applications.

## Embedded Multiplier Specifications

Table 1–26 lists the embedded multiplier specifications for Cyclone IV devices.

**Table 1–26. Embedded Multiplier Specifications for Cyclone IV Devices**

Mode	Resources Used	Performance					Unit
	Number of Multipliers	C6	C7, I7, A7	C8	C8L, I8L	C9L	
9 × 9-bit multiplier	1	340	300	260	240	175	MHz
18 × 18-bit multiplier	1	287	250	200	185	135	MHz

## Memory Block Specifications

Table 1–27 lists the M9K memory block specifications for Cyclone IV devices.

**Table 1–27. Memory Block Performance Specifications for Cyclone IV Devices**

Memory	Mode	Resources Used		Performance					Unit
		LEs	M9K Memory	C6	C7, I7, A7	C8	C8L, I8L	C9L	
M9K Block	FIFO 256 × 36	47	1	315	274	238	200	157	MHz
	Single-port 256 × 36	0	1	315	274	238	200	157	MHz
	Simple dual-port 256 × 36 CLK	0	1	315	274	238	200	157	MHz
	True dual port 512 × 18 single CLK	0	1	315	274	238	200	157	MHz

## Configuration and JTAG Specifications

Table 1–28 lists the configuration mode specifications for Cyclone IV devices.

**Table 1–28. Passive Configuration Mode Specifications for Cyclone IV Devices <sup>(1)</sup>**

Programming Mode	V <sub>CCINT</sub> Voltage Level (V)	DCLK f <sub>MAX</sub>	Unit
Passive Serial (PS)	1.0 <sup>(3)</sup>	66	MHz
	1.2	133	MHz
Fast Passive Parallel (FPP) <sup>(2)</sup>	1.0 <sup>(3)</sup>	66	MHz
	1.2 <sup>(4)</sup>	100	MHz

**Notes to Table 1–28:**

- (1) For more information about PS and FPP configuration timing parameters, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter.
- (2) FPP configuration mode supports all Cyclone IV E devices (except for E144 package devices) and EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 only.
- (3) V<sub>CCINT</sub> = 1.0 V is only supported for Cyclone IV E 1.0 V core voltage devices.
- (4) Cyclone IV E devices support 1.2 V V<sub>CCINT</sub>. Cyclone IV E 1.2 V core voltage devices support 133 MHz DCLK f<sub>MAX</sub> for EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, and EP4CE40 only.

Table 1–29 lists the active configuration mode specifications for Cyclone IV devices.

**Table 1–29. Active Configuration Mode Specifications for Cyclone IV Devices**

Programming Mode	DCLK Range	Typical DCLK	Unit
Active Parallel (AP) <sup>(1)</sup>	20 to 40	33	MHz
Active Serial (AS)	20 to 40	33	MHz

**Note to Table 1–29:**

(1) AP configuration mode is only supported for Cyclone IV E devices.

Table 1–30 lists the JTAG timing parameters and values for Cyclone IV devices.

**Table 1–30. JTAG Timing Parameters for Cyclone IV Devices <sup>(1)</sup>**

Symbol	Parameter	Min	Max	Unit
t <sub>JCP</sub>	TCK clock period	40	—	ns
t <sub>JCH</sub>	TCK clock high time	19	—	ns
t <sub>JCL</sub>	TCK clock low time	19	—	ns
t <sub>JPSU_TDI</sub>	JTAG port setup time for TDI	1	—	ns
t <sub>JPSU_TMS</sub>	JTAG port setup time for TMS	3	—	ns
t <sub>JPH</sub>	JTAG port hold time	10	—	ns
t <sub>JPCO</sub>	JTAG port clock to output <sup>(2), (3)</sup>	—	15	ns
t <sub>JPZX</sub>	JTAG port high impedance to valid output <sup>(2), (3)</sup>	—	15	ns
t <sub>JPXZ</sub>	JTAG port valid output to high impedance <sup>(2), (3)</sup>	—	15	ns
t <sub>JSSU</sub>	Capture register setup time	5	—	ns
t <sub>JSH</sub>	Capture register hold time	10	—	ns
t <sub>JSCO</sub>	Update register clock to output	—	25	ns
t <sub>JSZX</sub>	Update register high impedance to valid output	—	25	ns
t <sub>JSXZ</sub>	Update register valid output to high impedance	—	25	ns

**Notes to Table 1–30:**

(1) For more information about JTAG waveforms, refer to “JTAG Waveform” in “Glossary” on page 1–37.

(2) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 16 ns.

(3) For EP4CGX22, EP4CGX30 (F324 and smaller package), EP4CGX110, and EP4CGX150 devices, the output time specification for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins is 16 ns. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 18 ns.

## Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/Os using the SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speeds. I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-V LVTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.

**Table 1–34. True LVDS Transmitter Timing Specifications for Cyclone IV Devices <sup>(1)</sup>, <sup>(3)</sup>**

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f <sub>HCLK</sub> (input clock frequency)	×10	5	420	5	370	5	320	5	320	5	250	MHz
	×8	5	420	5	370	5	320	5	320	5	250	MHz
	×7	5	420	5	370	5	320	5	320	5	250	MHz
	×4	5	420	5	370	5	320	5	320	5	250	MHz
	×2	5	420	5	370	5	320	5	320	5	250	MHz
	×1	5	420	5	402.5	5	402.5	5	362	5	265	MHz
HSIODR	×10	100	840	100	740	100	640	100	640	100	500	Mbps
	×8	80	840	80	740	80	640	80	640	80	500	Mbps
	×7	70	840	70	740	70	640	70	640	70	500	Mbps
	×4	40	840	40	740	40	640	40	640	40	500	Mbps
	×2	20	840	20	740	20	640	20	640	20	500	Mbps
	×1	10	420	10	402.5	10	402.5	10	362	10	265	Mbps
t <sub>DUTY</sub>	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	—	600	—	700	ps
t <sub>LOCK</sub> <sup>(2)</sup>	—	—	1	—	1	—	1	—	1	—	1	ms

**Notes to Table 1–34:**

- (1) Cyclone IV E—true LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Cyclone IV GX—true LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6.
- (2) t<sub>LOCK</sub> is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

**Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices <sup>(1)</sup>, <sup>(3)</sup> (Part 1 of 2)**

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f <sub>HCLK</sub> (input clock frequency)	×10	5	320	5	320	5	275	5	275	5	250	MHz
	×8	5	320	5	320	5	275	5	275	5	250	MHz
	×7	5	320	5	320	5	275	5	275	5	250	MHz
	×4	5	320	5	320	5	275	5	275	5	250	MHz
	×2	5	320	5	320	5	275	5	275	5	250	MHz
	×1	5	402.5	5	402.5	5	402.5	5	362	5	265	MHz
HSIODR	×10	100	640	100	640	100	550	100	550	100	500	Mbps
	×8	80	640	80	640	80	550	80	550	80	500	Mbps
	×7	70	640	70	640	70	550	70	550	70	500	Mbps
	×4	40	640	40	640	40	550	40	550	40	500	Mbps
	×2	20	640	20	640	20	550	20	550	20	500	Mbps
	×1	10	402.5	10	402.5	10	402.5	10	362	10	265	Mbps

## IOE Programmable Delay

Table 1–40 and Table 1–41 list the IOE programmable delay for Cyclone IV E 1.0 V core voltage devices.

**Table 1–40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Devices <sup>(1), (2)</sup>**

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset					Unit
				Fast Corner		Slow Corner			
				C8L	I8L	C8L	C9L	I8L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.054	1.924	3.387	4.017	3.411	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.010	1.875	3.341	4.252	3.367	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.641	0.631	1.111	1.377	1.124	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.971	0.931	1.684	2.298	1.684	ns

**Notes to Table 1–40:**

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–41. IOE Programmable Delay on Row Pins for Cyclone IV E 1.0 V Core Voltage Devices <sup>(1), (2)</sup>**

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset					Unit
				Fast Corner		Slow Corner			
				C8L	I8L	C8L	C9L	I8L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.057	1.921	3.389	4.146	3.412	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.059	1.919	3.420	4.374	3.441	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.670	0.623	1.160	1.420	1.168	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.960	0.919	1.656	2.258	1.656	ns

**Notes to Table 1–41:**

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.



Table 1-46. Glossary (Part 2 of 5)

Letter	Term	Definitions
<b>J</b>	JTAG Waveform	<p>The diagram illustrates the JTAG waveform with the following timing parameters:</p> <ul style="list-style-type: none"> <li><math>t_{JCP}</math>: Time from TCK rising edge to TMS falling edge.</li> <li><math>t_{JCH}</math>: Time from TCK rising edge to TDI falling edge.</li> <li><math>t_{JCL}</math>: Time from TCK rising edge to TDI rising edge.</li> <li><math>t_{JPSU\_TDI}</math>: Time from TCK rising edge to TDI rising edge.</li> <li><math>t_{JPSU\_TMS}</math>: Time from TCK rising edge to TMS rising edge.</li> <li><math>t_{JPH}</math>: Time from TCK rising edge to TMS falling edge.</li> <li><math>t_{JPZX}</math>: Time from TCK rising edge to TDO rising edge.</li> <li><math>t_{JPCO}</math>: Time from TCK rising edge to TDO falling edge.</li> <li><math>t_{JPXZ}</math>: Time from TCK rising edge to TDO rising edge.</li> <li><math>t_{JSSU}</math>: Time from TCK rising edge to TDO rising edge.</li> <li><math>t_{JSH}</math>: Time from TCK rising edge to TDO falling edge.</li> <li><math>t_{JSZX}</math>: Time from TCK rising edge to TDO rising edge.</li> <li><math>t_{JSCO}</math>: Time from TCK rising edge to TDO falling edge.</li> <li><math>t_{JSXZ}</math>: Time from TCK rising edge to TDO rising edge.</li> </ul>
<b>K</b>	—	—
<b>L</b>	—	—
<b>M</b>	—	—
<b>N</b>	—	—
<b>O</b>	—	—
<b>P</b>	PLL Block	<p>The following highlights the PLL specification parameters:</p> <p>The diagram shows the PLL block architecture with the following components and signals:</p> <ul style="list-style-type: none"> <li><b>Inputs:</b> CLK, Core Clock.</li> <li><b>Switchover:</b> A block that selects between the CLK and Core Clock inputs.</li> <li><b>Frequency Divider:</b> A block that divides the input frequency by <math>N</math> to produce <math>f_{INPFD}</math>.</li> <li><b>PFD (Phase-Frequency Divider):</b> A block that compares the input frequency with the feedback frequency.</li> <li><b>CP (Charge Pump):</b> A block that generates the current for the VCO.</li> <li><b>LF (Loop Filter):</b> A block that filters the output of the CP.</li> <li><b>VCO (Voltage-Controlled Oscillator):</b> A block that generates the output frequency <math>f_{VCO}</math>.</li> <li><b>Counters C0..C4:</b> A block that divides the output frequency by a programmable factor to produce <math>f_{OUT}</math>.</li> <li><b>CLKOUT Pins:</b> The output of the PLL, labeled <math>f_{OUT\_EXT}</math>.</li> <li><b>GCLK:</b> The global clock output.</li> <li><b>Phase tap:</b> A block that provides a phase tap for the PLL.</li> </ul> <p><b>Key:</b></p> <ul style="list-style-type: none"> <li>Reconfigurable in User Mode</li> </ul>
<b>Q</b>	—	—

Table 1-46. Glossary (Part 3 of 5)

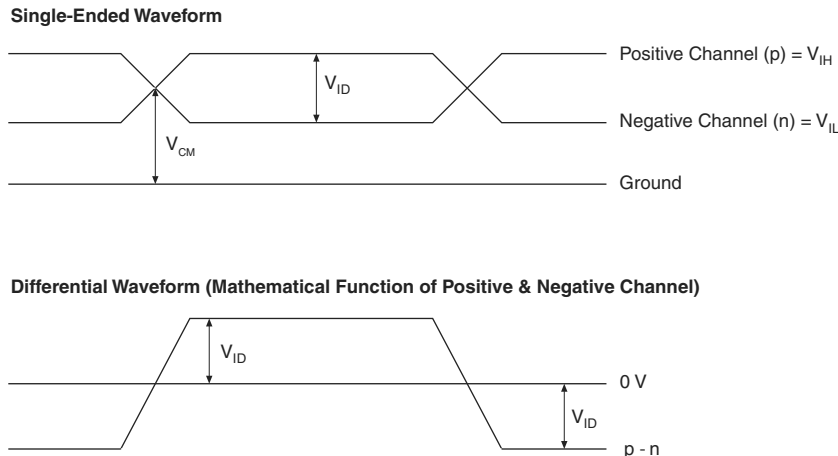
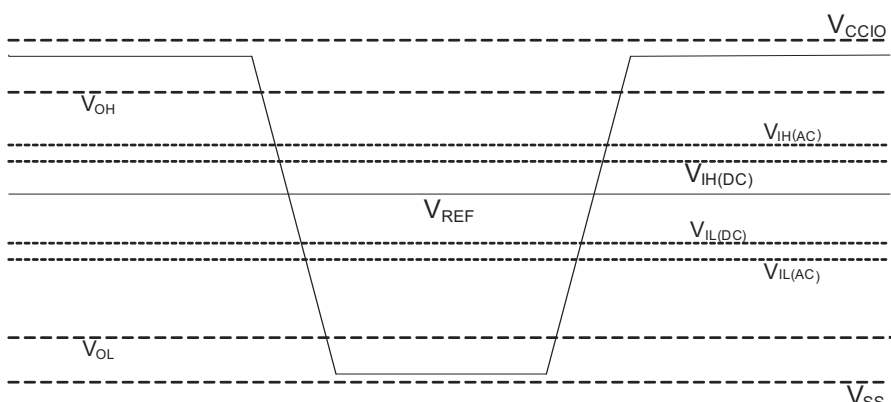
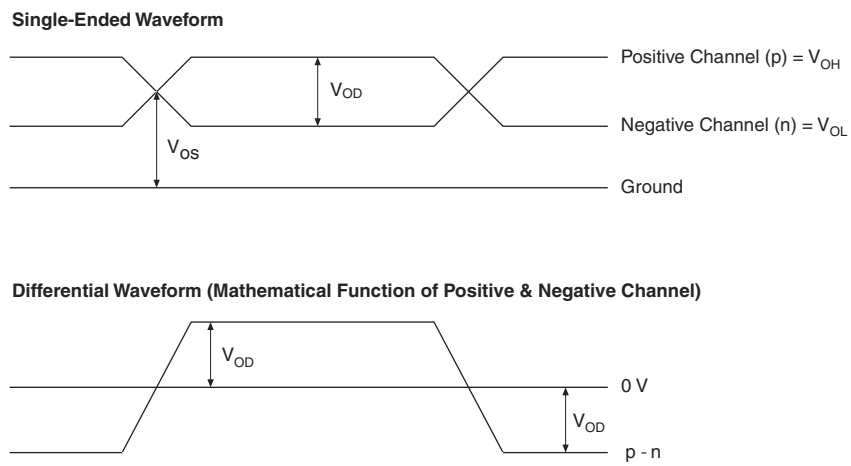
Letter	Term	Definitions
R	$R_L$	Receiver differential input discrete resistor (external to Cyclone IV devices).
	Receiver Input Waveform	<p>Receiver input waveform for LVDS and LVPECL differential standards:</p>  <p>Single-Ended Waveform</p> <p>Positive Channel (p) = <math>V_{IH}</math></p> <p>Negative Channel (n) = <math>V_{IL}</math></p> <p>Ground</p> <p>Differential Waveform (Mathematical Function of Positive &amp; Negative Channel)</p> <p>0 V</p> <p>p - n</p>
	Receiver input skew margin (RSKM)	High-speed I/O block: The total margin left after accounting for the sampling window and TCCS. $RSKM = (TUI - SW - TCCS) / 2$ .
S	Single-ended voltage-referenced I/O Standard	 <p><math>V_{CCIO}</math></p> <p><math>V_{OH}</math></p> <p><math>V_{OL}</math></p> <p><math>V_{REF}</math></p> <p><math>V_{IH(DC)}</math></p> <p><math>V_{IL(DC)}</math></p> <p><math>V_{IH(AC)}</math></p> <p><math>V_{IL(AC)}</math></p> <p><math>V_{SS}</math></p> <p>The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform <i>ringing</i>.</p>
	SW (Sampling Window)	High-speed I/O block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window.

Table 1-46. Glossary (Part 4 of 5)

Letter	Term	Definitions
T	$t_C$	High-speed receiver and transmitter input and output clock period.
	Channel-to-channel-skew (TCCS)	High-speed I/O block: The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew. The clock is included in the TCCS measurement.
	$t_{cin}$	Delay from the clock pad to the I/O input register.
	$t_{CO}$	Delay from the clock pad to the I/O output.
	$t_{cout}$	Delay from the clock pad to the I/O output register.
	$t_{DUTY}$	High-speed I/O block: Duty cycle on high-speed transmitter output clock.
	$t_{FALL}$	Signal high-to-low transition time (80–20%).
	$t_H$	Input register hold time.
	Timing Unit Interval (TUI)	High-speed I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency Multiplication Factor}) = t_C/w$ ).
	$t_{INJITTER}$	Period jitter on the PLL clock input.
	$t_{OUTJITTER\_DEDCLK}$	Period jitter on the dedicated clock output driven by a PLL.
	$t_{OUTJITTER\_IO}$	Period jitter on the general purpose I/O driven by a PLL.
	$t_{pllcin}$	Delay from the PLL inclk pad to the I/O input register.
	$t_{pllcout}$	Delay from the PLL inclk pad to the I/O output register.
	Transmitter Output Waveform	<p>Transmitter output waveforms for the LVDS, mini-LVDS, PPDS and RSDS Differential I/O Standards:</p> 
	$t_{RISE}$	Signal low-to-high transition time (20–80%).
	$t_{SU}$	Input register setup time.
U	—	—

**Table 1–46. Glossary (Part 5 of 5)**

Letter	Term	Definitions
<b>V</b>	$V_{CM(DC)}$	DC common mode input voltage.
	$V_{DIF(AC)}$	AC differential input voltage: The minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage: The minimum DC input differential voltage required for switching.
	$V_{ICM}$	Input common mode voltage: The common mode of the differential signal at the receiver.
	$V_{ID}$	Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{IH}$	Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage.
	$V_{IH(DC)}$	High-level DC input voltage.
	$V_{IL}$	Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage.
	$V_{IL(DC)}$	Low-level DC input voltage.
	$V_{IN}$	DC input voltage.
	$V_{OCM}$	Output common mode voltage: The common mode of the differential signal at the transmitter.
	$V_{OD}$	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} - V_{OL}$ .
	$V_{OH}$	Voltage output high: The maximum positive voltage from an output that the device considers is accepted as the minimum positive high level.
	$V_{OL}$	Voltage output low: The maximum positive voltage from an output that the device considers is accepted as the maximum positive low level.
	$V_{OS}$	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$ .
	$V_{OX(AC)}$	AC differential output cross point voltage: the voltage at which the differential output signals must cross.
	$V_{REF}$	Reference voltage for the SSTL and HSTL I/O standards.
	$V_{REF(AC)}$	AC input reference voltage for the SSTL and HSTL I/O standards. $V_{REF(AC)} = V_{REF(DC)} + \text{noise}$ . The peak-to-peak AC noise on $V_{REF}$ must not exceed 2% of $V_{REF(DC)}$ .
	$V_{REF(DC)}$	DC input reference voltage for the SSTL and HSTL I/O standards.
	$V_{SWING(AC)}$	AC differential input voltage: AC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	$V_{SWING(DC)}$	DC differential input voltage: DC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	$V_{TT}$	Termination voltage for the SSTL and HSTL I/O standards.
	$V_X(AC)$	AC differential input cross point voltage: The voltage at which the differential input signals must cross.
<b>W</b>	—	—
<b>X</b>	—	—
<b>Y</b>	—	—
<b>Z</b>	—	—

**Table 1–47. Document Revision History**

Date	Version	Changes
February 2010	1.1	<ul style="list-style-type: none"><li>■ Updated Table 1–3 through Table 1–44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release.</li><li>■ Minor text edits.</li></ul>
November 2009	1.0	Initial release.