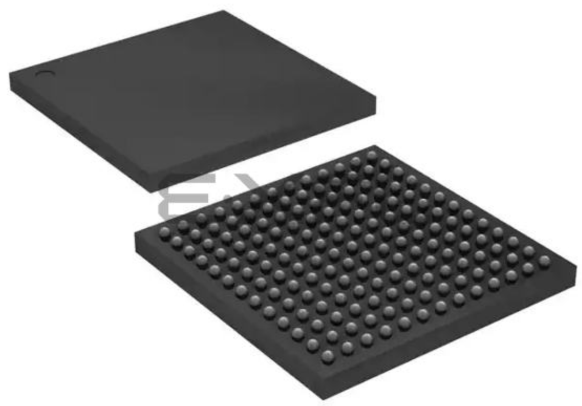
# Intel - EP4CGX22BF14C8 Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 1330 |
| Number of Logic Elements/Cells | 21280 |
| Total RAM Bits | 774144 |
| Number of I/O | 72 |
| Number of Gates | - |
| Voltage - Supply | 1.16V ~ 1.24V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 169-LBGA |
| Supplier Device Package | 169-FBGA (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep4cgx22bf14c8 |

## Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone IV devices. Table 1–3 and Table 1–4 list the steady-state voltage and current values expected from Cyclone IV E and Cyclone IV GX devices. All supplies must be strictly monotonic without plateaus.

**Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices** *(1), (2)* **(Part 1 of 2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CCINT}$ *(3)* | Supply voltage for internal logic, 1.2-V operation | — | 1.15 | 1.2 | 1.25 | V |
| | Supply voltage for internal logic, 1.0-V operation | — | 0.97 | 1.0 | 1.03 | V |
| $V_{CCIO}$ *(3), (4)* | Supply voltage for output buffers, 3.3-V operation | — | 3.135 | 3.3 | 3.465 | V |
| | Supply voltage for output buffers, 3.0-V operation | — | 2.85 | 3 | 3.15 | V |
| | Supply voltage for output buffers, 2.5-V operation | — | 2.375 | 2.5 | 2.625 | V |
| | Supply voltage for output buffers, 1.8-V operation | — | 1.71 | 1.8 | 1.89 | V |
| | Supply voltage for output buffers, 1.5-V operation | — | 1.425 | 1.5 | 1.575 | V |
| | Supply voltage for output buffers, 1.2-V operation | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CCA}$ *(3)* | Supply (analog) voltage for PLL regulator | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCD\_PLL}$ *(3)* | Supply (digital) voltage for PLL, 1.2-V operation | — | 1.15 | 1.2 | 1.25 | V |
| | Supply (digital) voltage for PLL, 1.0-V operation | — | 0.97 | 1.0 | 1.03 | V |
| $V_I$ | Input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | For commercial use | 0 | — | 85 | °C |
| | | For industrial use | –40 | — | 100 | °C |
| | | For extended temperature | –40 | — | 125 | °C |
| | | For automotive use | –40 | — | 125 | °C |
| $t_{RAMP}$ | Power supply ramp time | Standard power-on reset (POR) *(5)* | 50 µs | — | 50 ms | — |
| | | Fast POR *(6)* | 50 µs | — | 3 ms | — |

**Table 1–4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CCA\_GXB}$ | Transceiver PMA and auxiliary power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCL\_GXB}$ | Transceiver PMA and auxiliary power supply | — | 1.16 | 1.2 | 1.24 | V |
| $V_I$ | DC input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | DC output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | For commercial use | 0 | — | 85 | °C |
| | | For industrial use | –40 | — | 100 | °C |
| $t_{RAMP}$ | Power supply ramp time | Standard power-on reset (POR) *(7)* | 50 µs | — | 50 ms | — |
| | | Fast POR *(8)* | 50 µs | — | 3 ms | — |
| $I_{Diode}$ | Magnitude of DC current across PCI-clamp diode when enabled | — | — | — | 10 | mA |

**Notes to Table 1–4:**

(1) All `VCCA` pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.

(2) You must connect $V_{CCD\_PLL}$ to $V_{CCINT}$ through a decoupling capacitor and ferrite bead.

(3) Power supplies must rise monotonically.

(4) $V_{CCIO}$ for all I/O banks must be powered up during device operation. Configurations pins are powered up by $V_{CCIO}$ of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support $V_{CCIO}$ of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the $V_{CCIO}$ level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.

(5) You must set $V_{CC\_CLKIN}$ to 2.5 V if you use `CLKIN` as a high-speed serial interface (HSSI) `refclk` or as a `DIFFCLK` input.

(6) The `CLKIN` pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.

(7) The POR time for Standard POR ranges between 50 and 200 ms. $V_{CCINT}$, $V_{CCA}$, and $V_{CCIO}$ of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.

(8) The POR time for Fast POR ranges between 3 and 9 ms. $V_{CCINT}$, $V_{CCA}$, and $V_{CCIO}$ of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

## ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1–5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

**Table 1–5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os**

| Symbol | Parameter | Passing Voltage | Unit |
|---|---|---|---|
| $V_{ESDHBM}$ | ESD voltage using the HBM (GPIOs) *(1)* | ± 2000 | V |
| | ESD using the HBM (HSSI I/Os) *(2)* | ± 1000 | V |
| $V_{ESDCDM}$ | ESD using the CDM (GPIOs) | ± 500 | V |
| | ESD using the CDM (HSSI I/Os) *(2)* | ± 250 | V |

**Notes to Table 1–5:**

(1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is ±1000V.

(2) This value is applicable only to Cyclone IV GX devices.

# DC Characteristics

This section lists the I/O leakage current, pin capacitance, on-chip termination (OCT) tolerance, and bus hold specifications for Cyclone IV devices.

## Supply Current

The device supply current requirement is the minimum current drawn from the power supply pins that can be used as a reference for power size planning. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary greatly with the resources used. Table 1–6 lists the I/O pin leakage current for Cyclone IV devices.

**Table 1–6. I/O Pin Leakage Current for Cyclone IV Devices** (1), (2)

| Symbol | Parameter | Conditions | Device | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current | $V_I$ = 0 V to $V_{CCIOMAX}$ | — | –10 | — | 10 | µA |
| $I_{OZ}$ | Tristated I/O pin leakage current | $V_O$ = 0 V to $V_{CCIOMAX}$ | — | –10 | — | 10 | µA |

**Notes to Table 1–6:**

(1) This value is specified for normal device operation. The value varies during device power-up. This applies for all $V_{CCIO}$ settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) The 10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

## Bus Hold

The bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1–7 lists bus hold specifications for Cyclone IV devices.

**Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 1 of 2)** (1)

| Parameter | Condition | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus hold low, sustaining current | $V_{IN} > V_{IL}$ (maximum) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | µA |
| Bus hold high, sustaining current | $V_{IN} < V_{IL}$ (minimum) | –8 | — | –12 | — | –30 | — | –50 | — | –70 | — | –70 | — | µA |
| Bus hold low, overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | µA |
| Bus hold high, overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | –125 | — | –175 | — | –200 | — | –300 | — | –500 | — | –500 | µA |

**Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 2 of 2)** (1)

| Parameter | Condition | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus hold trip point | — | 0.3 | 0.9 | 0.375 | 1.125 | 0.68 | 1.07 | 0.7 | 1.7 | 0.8 | 2 | 0.8 | 2 | V |

**Note to Table 1–7:**

(1) Bus hold trip points are based on the calculated input voltages from the JEDEC standard.

## OCT Specifications

Table 1–8 lists the variation of OCT without calibration across process, temperature, and voltage (PVT).

**Table 1–8. Series OCT Without Calibration Specifications for Cyclone IV Devices**

| Description | $V_{CCIO}$ (V) | Resistance Tolerance | | Unit |
|---|---|---|---|---|
| | | Commercial Maximum | Industrial, Extended industrial, and Automotive Maximum | |
| Series OCT without calibration | 3.0 | ±30 | ±40 | % |
| | 2.5 | ±30 | ±40 | % |
| | 1.8 | ±40 | ±50 | % |
| | 1.5 | ±50 | ±50 | % |
| | 1.2 | ±50 | ±50 | % |

OCT calibration is automatically performed at device power-up for OCT-enabled I/Os.

Table 1–9 lists the OCT calibration accuracy at device power-up.

**Table 1–9. Series OCT with Calibration at Device Power-Up Specifications for Cyclone IV Devices**

| Description | $V_{CCIO}$ (V) | Calibration Accuracy | | Unit |
|---|---|---|---|---|
| | | Commercial Maximum | Industrial, Extended industrial, and Automotive Maximum | |
| Series OCT with calibration at device power-up | 3.0 | ±10 | ±10 | % |
| | 2.5 | ±10 | ±10 | % |
| | 1.8 | ±10 | ±10 | % |
| | 1.5 | ±10 | ±10 | % |
| | 1.2 | ±10 | ±10 | % |

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up. Use Table 1–10 and Equation 1–1 to determine the final OCT resistance considering the variations after calibration at device power-up. Table 1–10 lists the change percentage of the OCT resistance with voltage and temperature.

**Table 1–10. OCT Variation After Calibration at Device Power-Up for Cyclone IV Devices**

| Nominal Voltage | dR/dT (%/°C) | dR/dV (%/mV) |
|---|---|---|
| 3.0 | 0.262 | –0.026 |
| 2.5 | 0.234 | –0.039 |
| 1.8 | 0.219 | –0.086 |
| 1.5 | 0.199 | –0.136 |
| 1.2 | 0.161 | –0.288 |

**Equation 1–1. Final OCT Resistance** *(1), (2), (3), (4), (5), (6)*

$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV$ ——— *(7)*

$\Delta R_T = (T_2 - T_1) \times dR/dT$ ——— *(8)*

For $\Delta R_x < 0$; $MF_x = 1/ (|\Delta R_x|/100 + 1)$ ——— *(9)*

For $\Delta R_x > 0$; $MF_x = \Delta R_x/100 + 1$ ——— *(10)*

$MF = MF_V \times MF_T$ ——— *(11)*

$R_{final} = R_{initial} \times MF$ ——— *(12)*

**Notes to Equation 1–1:**

(1) $T_2$ is the final temperature.
(2) $T_1$ is the initial temperature.
(3) MF is multiplication factor.
(4) $R_{final}$ is final resistance.
(5) $R_{initial}$ is initial resistance.
(6) Subscript $_x$ refers to both $_V$ and $_T$.
(7) $\Delta R_V$ is a variation of resistance with voltage.
(8) $\Delta R_T$ is a variation of resistance with temperature.
(9) dR/dT is the change percentage of resistance with temperature after calibration at device power-up.
(10) dR/dV is the change percentage of resistance with voltage after calibration at device power-up.
(11) $V_2$ is final voltage.
(12) $V_1$ is the initial voltage.

**Table 1–16. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Cyclone IV Devices** *(1)*

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) *(2)* | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 1.19 | 1.25 | 1.31 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.7 | 1.8 | 1.9 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | 0.85 | 0.9 | 0.95 |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.71 | 0.75 | 0.79 | 0.71 | 0.75 | 0.79 |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.48 x $V_{CCIO}$ *(3)*<br>0.47 x $V_{CCIO}$ *(4)* | 0.5 x $V_{CCIO}$ *(3)*<br>0.5 x $V_{CCIO}$ *(4)* | 0.52 x $V_{CCIO}$ *(3)*<br>0.53 x $V_{CCIO}$ *(4)* | — | 0.5 x $V_{CCIO}$ | — |

**Notes to Table 1–16:**

(1) For an explanation of terms used in Table 1–16, refer to "Glossary" on page 1–37.

(2) $V_{TT}$ of the transmitting device must track $V_{REF}$ of the receiving device.

(3) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.

(4) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

**Table 1–17. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone IV Devices**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | | $V_{IH(AC)}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Max | Min | | |
| SSTL-2 Class I | — | $V_{REF}$ – 0.18 | $V_{REF}$ + 0.18 | — | — | $V_{REF}$ – 0.35 | $V_{REF}$ + 0.35 | — | $V_{TT}$ – 0.57 | $V_{TT}$ + 0.57 | 8.1 | –8.1 |
| SSTL-2 Class II | — | $V_{REF}$ – 0.18 | $V_{REF}$ + 0.18 | — | — | $V_{REF}$ – 0.35 | $V_{REF}$ + 0.35 | — | $V_{TT}$ – 0.76 | $V_{TT}$ + 0.76 | 16.4 | –16.4 |
| SSTL-18 Class I | — | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | — | — | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | — | $V_{TT}$ – 0.475 | $V_{TT}$ + 0.475 | 6.7 | –6.7 |
| SSTL-18 Class II | — | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | — | — | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | — | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |
| HSTL-18 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-18 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-12 Class I | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | –0.24 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.24 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 8 | –8 |
| HSTL-12 Class II | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | –0.24 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.24 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 14 | –14 |

For more information about receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *I/O Features in Cyclone IV Devices* chapter.

**Table 1–18. Differential SSTL I/O Standard Specifications for Cyclone IV Devices** *(1)*

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{Swing(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{Swing(AC)}$ (V) | | $V_{OX(AC)}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.36 | $V_{CCIO}$ | $V_{CCIO}/2 - 0.2$ | — | $V_{CCIO}/2 + 0.2$ | 0.7 | $V_{CCIO}$ | $V_{CCIO}/2 - 0.125$ | — | $V_{CCIO}/2 + 0.125$ |
| SSTL-18 Class I, II | 1.7 | 1.8 | 1.90 | 0.25 | $V_{CCIO}$ | $V_{CCIO}/2 - 0.175$ | — | $V_{CCIO}/2 + 0.175$ | 0.5 | $V_{CCIO}$ | $V_{CCIO}/2 - 0.125$ | — | $V_{CCIO}/2 + 0.125$ |

**Note to Table 1–18:**

(1) Differential SSTL requires a $V_{REF}$ input.

**Table 1–19. Differential HSTL I/O Standard Specifications for Cyclone IV Devices** *(1)*

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.85 | — | 0.95 | 0.85 | — | 0.95 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.71 | — | 0.79 | 0.71 | — | 0.79 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ | 0.48 x $V_{CCIO}$ | — | 0.52 x $V_{CCIO}$ | 0.48 x $V_{CCIO}$ | — | 0.52 x $V_{CCIO}$ | 0.3 | 0.48 x $V_{CCIO}$ |

**Note to Table 1–19:**

(1) Differential HSTL requires a $V_{REF}$ input.

**Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices** *(1)* **(Part 1 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV) | | $V_{IcM}$ (V) *(2)* | | | $V_{OD}$ (mV) *(3)* | | | $V_{OS}$ (V) *(3)* | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| LVPECL (Row I/Os) *(6)* | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX} \leq$ 500 Mbps | 1.80 | — | — | — | — | — | — |
| | | | | | | 0.55 | 500 Mbps $\leq D_{MAX} \leq$ 700 Mbps | 1.80 | | | | | | |
| | | | | | | 1.05 | $D_{MAX} >$ 700 Mbps | 1.55 | | | | | | |
| LVPECL (Column I/Os) *(6)* | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX} \leq$ 500 Mbps | 1.80 | — | — | — | — | — | — |
| | | | | | | 0.55 | 500 Mbps $\leq D_{MAX} \leq$ 700 Mbps | 1.80 | | | | | | |
| | | | | | | 1.05 | $D_{MAX} >$ 700 Mbps | 1.55 | | | | | | |
| LVDS (Row I/Os) | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX} \leq$ 500 Mbps | 1.80 | 247 | — | 600 | 1.125 | 1.25 | 1.375 |
| | | | | | | 0.55 | 500 Mbps $\leq D_{MAX} \leq$ 700 Mbps | 1.80 | | | | | | |
| | | | | | | 1.05 | $D_{MAX} >$ 700 Mbps | 1.55 | | | | | | |

**Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices** *(1)* **(Part 2 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV) | | $V_{IcM}$ (V) *(2)* | | | $V_{OD}$ (mV) *(3)* | | | $V_{OS}$ (V) *(3)* | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| LVDS (Column I/Os) | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX} \leq$ 500 Mbps | 1.80 | 247 | — | 600 | 1.125 | 1.25 | 1.375 |
| | | | | | | 0.55 | 500 Mbps $\leq D_{MAX} \leq$ 700 Mbps | 1.80 | | | | | | |
| | | | | | | 1.05 | $D_{MAX}$ > 700 Mbps | 1.55 | | | | | | |
| BLVDS (Row I/Os) *(4)* | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — |
| BLVDS (Column I/Os) *(4)* | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — |
| mini-LVDS (Row I/Os) *(5)* | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 300 | — | 600 | 1.0 | 1.2 | 1.4 |
| mini-LVDS (Column I/Os) *(5)* | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 300 | — | 600 | 1.0 | 1.2 | 1.4 |
| RSDS® (Row I/Os) *(5)* | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.5 |
| RSDS (Column I/Os) *(5)* | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.5 |
| PPDS (Row I/Os) *(5)* | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.4 |
| PPDS (Column I/Os) *(5)* | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.4 |

**Notes to Table 1–20:**

(1) For an explanation of terms used in Table 1–20, refer to “Glossary” on page 1–37.

(2) $V_{IN}$ range: 0 V ≤ $V_{IN}$ ≤ 1.85 V.

(3) $R_L$ range: 90 ≤ $R_L$ ≤ 110 Ω.

(4) There are no fixed $V_{IN}$, $V_{OD}$, and $V_{OS}$ specifications for BLVDS. They depend on the system topology.

(5) The Mini-LVDS, RSDS, and PPDS standards are only supported at the output pins.

(6) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported for output pins.

# Power Consumption

Use the following methods to estimate power for a design:

- the Excel-based EPE
- the Quartus® II PowerPlay power analyzer feature

The interactive Excel-based EPE is used prior to designing the device to get a magnitude estimate of the device power. The Quartus II PowerPlay power analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay power analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, combined with detailed circuit models, can yield very accurate power estimates.

For more information about power estimation tools, refer to the *Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handboo*k.

# Switching Characteristics

This section provides performance characteristics of Cyclone IV core and periphery blocks for commercial grade devices.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The upper-right hand corner of these tables show the designation as “Preliminary”.
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

## Transceiver Performance Specifications

Table 1–21 lists the Cyclone IV GX transceiver specifications.

**Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 1 of 4)**

| Symbol/ Description | Conditions | C6 | | | C7, I7 | | | C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Reference Clock** | | | | | | | | | | | |
| Supported I/O Standards | 1.2 V PCML, 1.5 V PCML, 3.3 V PCML, Differential LVPECL, LVDS, HCSL | | | | | | | | | | |
| Input frequency from `REFCLK` input pins | — | 50 | — | 156.25 | 50 | — | 156.25 | 50 | — | 156.25 | MHz |
| Spread-spectrum modulating clock frequency | Physical interface for PCI Express (PIPE) mode | 30 | — | 33 | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PIPE mode | — | 0 to –0.5% | — | — | 0 to –0.5% | — | — | 0 to –0.5% | — | — |
| Peak-to-peak differential input voltage | — | 0.1 | — | 1.6 | 0.1 | — | 1.6 | 0.1 | — | 1.6 | V |
| $V_{ICM}$ (AC coupled) | — | 1100 ± 5% | | | 1100 ± 5% | | | 1100 ± 5% | | | mV |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise *(1)* | Frequency offset = 1 MHz – 8 MHZ | — | — | –123 | — | — | –123 | — | — | –123 | dBc/Hz |
| Transmitter REFCLK Total Jitter *(1)* | | — | — | 42.3 | — | — | 42.3 | — | — | 42.3 | ps |
| $R_{ref}$ | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | Ω |
| **Transceiver Clock** | | | | | | | | | | | |
| `cal_blk_clk` clock frequency | — | 10 | — | 125 | 10 | — | 125 | 10 | — | 125 | MHz |
| `fixedclk` clock frequency | PCIe Receiver Detect | — | 125 | — | — | 125 | — | — | 125 | — | MHz |
| `reconfig_clk` clock frequency | Dynamic reconfiguration clock frequency | 2.5/ 37.5 *(2)* | — | 50 | 2.5/ 37.5 *(2)* | — | 50 | 2.5/ 37.5 *(2)* | — | 50 | MHz |
| Delta time between `reconfig_clk` | — | — | — | 2 | — | — | 2 | — | — | 2 | ms |
| Transceiver block minimum power-down pulse width | — | — | 1 | — | — | 1 | — | — | 1 | — | µs |

**Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 4 of 4)**

| Symbol/ Description | Conditions | C6 | | | C7, I7 | | | C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **PLD-Transceiver Interface** | | | | | | | | | | | |
| Interface speed (F324 and smaller package) | — | 25 | — | 125 | 25 | — | 125 | 25 | — | 125 | MHz |
| Interface speed (F484 and larger package) | — | 25 | — | 156.25 | 25 | — | 156.25 | 25 | — | 156.25 | MHz |
| Digital reset pulse width | — | Minimum is 2 parallel clock cycles | | | | | | | | | |

**Notes to Table 1–21:**

(1) This specification is valid for transmitter output jitter specification with a maximum total jitter value of 112 ps, typically for 3.125 Gbps SRIO and XAUI protocols.

(2) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter Only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver Only** or **Receiver and Transmitter** mode.

(3) The device cannot tolerate prolonged operation at this absolute maximum.

(4) The rate matcher supports only up to ±300 parts per million (ppm).

(5) Supported for the F169 and F324 device packages only.

(6) Supported for the F484, F672, and F896 device packages only. Pending device characterization.

(7) To support CDR ppm tolerance greater than ±300 ppm, implement ppm detector in user logic and configure CDR to Manual Lock Mode.

(8) Asynchronous spread-spectrum clocking is not supported.

(9) For the EP4CGX30 (F484 package only), EP4CGX50, and EP4CGX75 devices, the CDR ppl tolerance is ±200 ppm.

(10) Time taken until `pll_locked` goes high after `pll_powerdown` deasserts.

(11) Time that the CDR must be kept in lock-to-reference mode after `rx_analogreset` deasserts and before `rx_locktodata` is asserted in manual mode.

(12) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode (Figure 1–2), or after `rx_freqlocked` signal goes high in automatic mode (Figure 1–3).

(13) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode.

(14) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode.

(15) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Figure 1–2 shows the lock time parameters in manual mode.

☞ LTD = lock-to-data. LTR = lock-to-reference.

**Figure 1–2. Lock Time Parameters for Manual Mode**

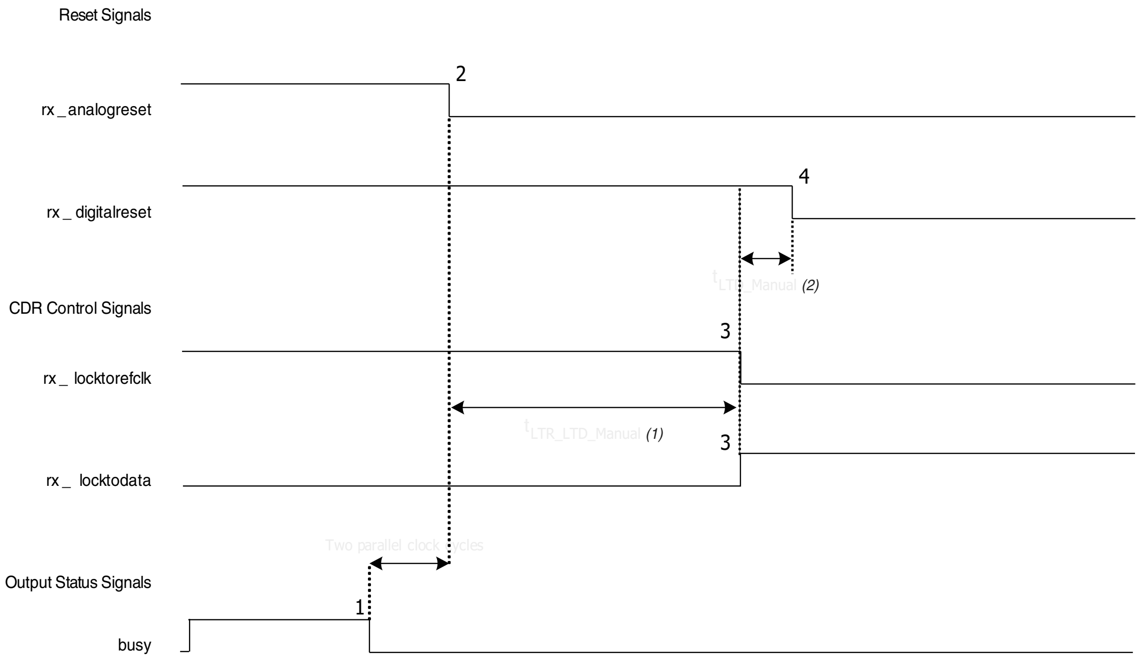

Figure 1–3 shows the lock time parameters in automatic mode.

**Figure 1–3. Lock Time Parameters for Automatic Mode**

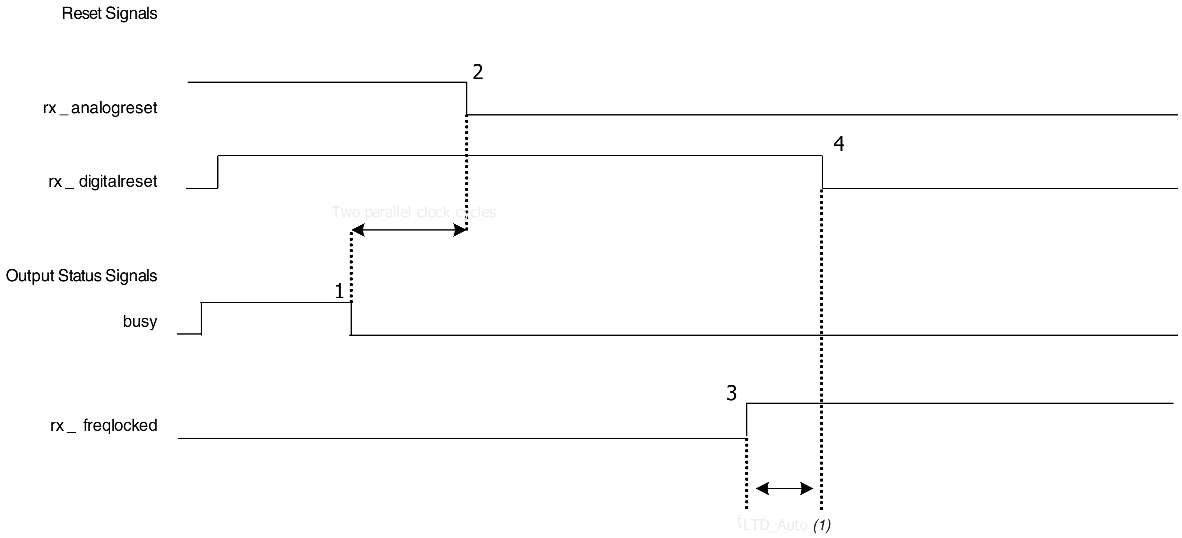

Figure 1–4 shows the differential receiver input waveform.

**Figure 1–4. Receiver Input Waveform**

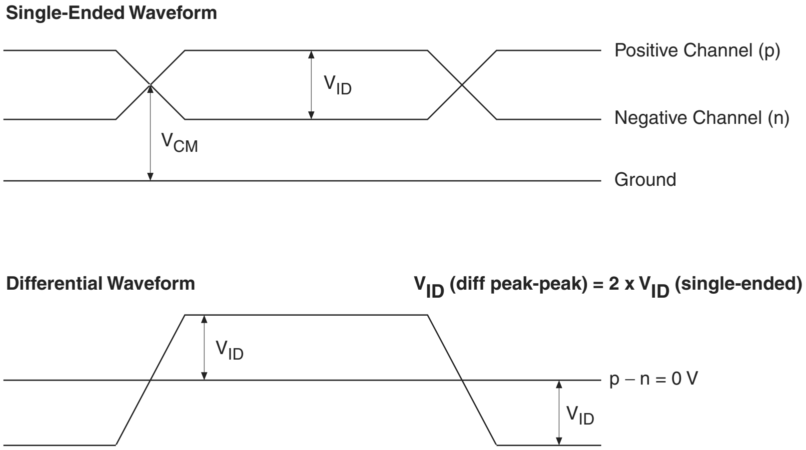

Figure 1–5 shows the transmitter output waveform.

**Figure 1–5. Transmitter Output Waveform**

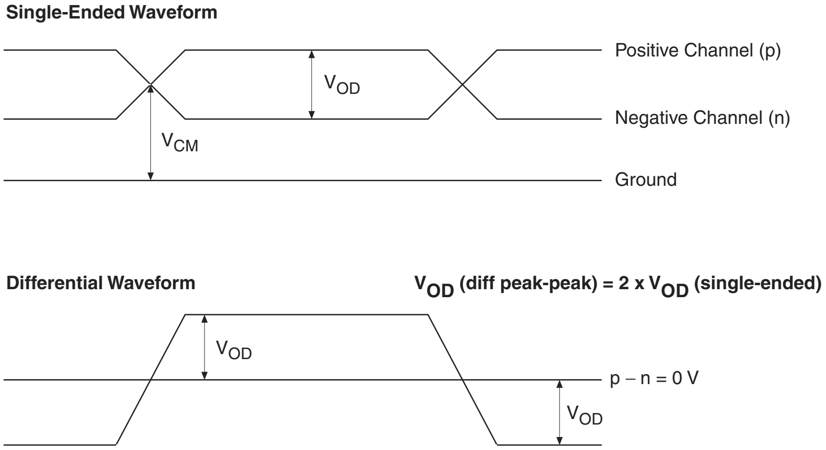

Table 1–22 lists the typical $V_{OD}$ for Tx term that equals 100 Ω.

**Table 1–22. Typical $V_{OD}$ Setting, Tx Term = 100 Ω**

| Symbol | $V_{OD}$ Setting (mV) | | | | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 (1) | 5 | 6 |
| $V_{OD}$ differential peak to peak typical (mV) | 400 | 600 | 800 | 900 | 1000 | 1200 |

**Note to Table 1–22:**

(1) This setting is required for compliance with the PCIe protocol.

**Table 1–25. PLL Specifications for Cyclone IV Devices** *(1), (2)* **(Part 2 of 2)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or `areset` is deasserted) | — | — | 1 | ms |
| $t_{OUTJITTER\_PERIOD\_DEDCLK}$ *(6)* | Dedicated clock output period jitter<br>$F_{OUT} \geq 100$ MHz | — | — | 300 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 30 | mUI |
| $t_{OUTJITTER\_CCJ\_DEDCLK}$ *(6)* | Dedicated clock output cycle-to-cycle jitter<br>$F_{OUT} \geq 100$ MHz | — | — | 300 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 30 | mUI |
| $t_{OUTJITTER\_PERIOD\_IO}$ *(6)* | Regular I/O period jitter<br>$F_{OUT} \geq 100$ MHz | — | — | 650 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 75 | mUI |
| $t_{OUTJITTER\_CCJ\_IO}$ *(6)* | Regular I/O cycle-to-cycle jitter<br>$F_{OUT} \geq 100$ MHz | — | — | 650 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 75 | mUI |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on `areset` signal. | 10 | — | — | ns |
| $t_{CONFIGPLL}$ | Time required to reconfigure scan chains for PLLs | — | 3.5 *(7)* | — | `SCANCLK` cycles |
| $f_{SCANCLK}$ | `scanclk` frequency | — | — | 100 | MHz |
| $t_{CASC\_OUTJITTER\_PERIOD\_DEDCLK}$ *(8), (9)* | Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz) | — | — | 425 | ps |
| | Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz) | — | — | 42.5 | mUI |

**Notes to Table 1–25:**

(1) This table is applicable for general purpose PLLs and multipurpose PLLs.

(2) You must connect $V_{CCD\_PLL}$ to $V_{CCINT}$ through the decoupling capacitor and ferrite bead.

(3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(4) The $V_{CO}$ frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the $V_{CO}$ post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.

(6) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.

(7) With 100-MHz `scanclk` frequency.

(8) The cascaded PLLs specification is applicable only with the following conditions:
- Upstream PLL—0.59 MHz ≤ Upstream PLL bandwidth < 1 MHz
- Downstream PLL—Downstream PLL bandwidth > 2 MHz

(9) PLL cascading is not supported for transceiver applications.

For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interfaces Handbook*.

Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specifications

Table 1–31 through Table 1–36 list the high-speed I/O timing for Cyclone IV devices. For definitions of high-speed timing specifications, refer to "Glossary" on page 1–37.

**Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4) (Part 1 of 2)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×8 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×7 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×4 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×2 | 5 | — | 180 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 155.5 | 5 | — | 132.5 | MHz |
| | ×1 | 5 | — | 360 | 5 | — | 311 | 5 | — | 311 | 5 | — | 311 | 5 | — | 265 | MHz |
| Device operation in Mbps | ×10 | 100 | — | 360 | 100 | — | 311 | 100 | — | 311 | 100 | — | 311 | 100 | — | 265 | Mbps |
| | ×8 | 80 | — | 360 | 80 | — | 311 | 80 | — | 311 | 80 | — | 311 | 80 | — | 265 | Mbps |
| | ×7 | 70 | — | 360 | 70 | — | 311 | 70 | — | 311 | 70 | — | 311 | 70 | — | 265 | Mbps |
| | ×4 | 40 | — | 360 | 40 | — | 311 | 40 | — | 311 | 40 | — | 311 | 40 | — | 265 | Mbps |
| | ×2 | 20 | — | 360 | 20 | — | 311 | 20 | — | 311 | 20 | — | 311 | 20 | — | 265 | Mbps |
| | ×1 | 10 | — | 360 | 10 | — | 311 | 10 | — | 311 | 10 | — | 311 | 10 | — | 265 | Mbps |
| $t_{DUTY}$ | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| Transmitter channel-to-channel skew (TCCS) | — | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 550 | — | — | 600 | — | — | 700 | ps |
| $t_{RISE}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |

**Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4) (Part 2 of 2)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | |
| $t_{LOCK}$ (3) | — | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | ms |

**Notes to Table 1–31:**

(1) Applicable for true RSDS and emulated RSDS_E_3R transmitter.

(2) Cyclone IV E devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated RSDS transmitter is supported at the output pin of all I/O Banks.
Cyclone IV GX devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(3) $t_{LOCK}$ is the time required for the PLL to lock from the end-of-device configuration.

(4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

**Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 1 of 2)**

| Symbol | Modes | C6 | | | C7, I7 | | | C8, A7 | | | C8L, I8L | | | C9L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | |
| $f_{HSCLK}$ (input clock frequency) | ×10 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 72.5 | MHz |
| | ×8 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 72.5 | MHz |
| | ×7 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 72.5 | MHz |
| | ×4 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 72.5 | MHz |
| | ×2 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | 5 | — | 72.5 | MHz |
| | ×1 | 5 | — | 170 | 5 | — | 170 | 5 | — | 170 | 5 | — | 170 | 5 | — | 145 | MHz |
| Device operation in Mbps | ×10 | 100 | — | 170 | 100 | — | 170 | 100 | — | 170 | 100 | — | 170 | 100 | — | 145 | Mbps |
| | ×8 | 80 | — | 170 | 80 | — | 170 | 80 | — | 170 | 80 | — | 170 | 80 | — | 145 | Mbps |
| | ×7 | 70 | — | 170 | 70 | — | 170 | 70 | — | 170 | 70 | — | 170 | 70 | — | 145 | Mbps |
| | ×4 | 40 | — | 170 | 40 | — | 170 | 40 | — | 170 | 40 | — | 170 | 40 | — | 145 | Mbps |
| | ×2 | 20 | — | 170 | 20 | — | 170 | 20 | — | 170 | 20 | — | 170 | 20 | — | 145 | Mbps |
| | ×1 | 10 | — | 170 | 10 | — | 170 | 10 | — | 170 | 10 | — | 170 | 10 | — | 145 | Mbps |
| $t_{DUTY}$ | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS | — | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 550 | — | — | 600 | — | — | 700 | ps |
| $t_{RISE}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |

## IOE Programmable Delay

Table 1–40 and Table 1–41 list the IOE programmable delay for Cyclone IV E 1.0 V core voltage devices.

**Table 1–40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Devices** (1), (2)

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | |
| | | | | C8L | I8L | C8L | C9L | I8L | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 2.054 | 1.924 | 3.387 | 4.017 | 3.411 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 2.010 | 1.875 | 3.341 | 4.252 | 3.367 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.641 | 0.631 | 1.111 | 1.377 | 1.124 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.971 | 0.931 | 1.684 | 2.298 | 1.684 | ns |

**Notes to Table 1–40:**

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–41. IOE Programmable Delay on Row Pins for Cyclone IV E 1.0 V Core Voltage Devices** (1), (2)

| Parameter | Paths Affected | Number of Setting | Min Offset | Max Offset | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | |
| | | | | C8L | I8L | C8L | C9L | I8L | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 2.057 | 1.921 | 3.389 | 4.146 | 3.412 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 2.059 | 1.919 | 3.420 | 4.374 | 3.441 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.670 | 0.623 | 1.160 | 1.420 | 1.168 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.960 | 0.919 | 1.656 | 2.258 | 1.656 | ns |

**Notes to Table 1–41:**

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–46. Glossary (Part 5 of 5)**

| Letter | Term | Definitions |
|---|---|---|
| **V** | $V_{CM(DC)}$ | DC common mode input voltage. |
| | $V_{DIF(AC)}$ | AC differential input voltage: The minimum AC input differential voltage required for switching. |
| | $V_{DIF(DC)}$ | DC differential input voltage: The minimum DC input differential voltage required for switching. |
| | $V_{ICM}$ | Input common mode voltage: The common mode of the differential signal at the receiver. |
| | $V_{ID}$ | Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | $V_{IH}$ | Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high. |
| | $V_{IH(AC)}$ | High-level AC input voltage. |
| | $V_{IH(DC)}$ | High-level DC input voltage. |
| | $V_{IL}$ | Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low. |
| | $V_{IL\ (AC)}$ | Low-level AC input voltage. |
| | $V_{IL\ (DC)}$ | Low-level DC input voltage. |
| | $V_{IN}$ | DC input voltage. |
| | $V_{OCM}$ | Output common mode voltage: The common mode of the differential signal at the transmitter. |
| | $V_{OD}$ | Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} – V_{OL}$. |
| | $V_{OH}$ | Voltage output high: The maximum positive voltage from an output that the device considers is accepted as the minimum positive high level. |
| | $V_{OL}$ | Voltage output low: The maximum positive voltage from an output that the device considers is accepted as the maximum positive low level. |
| | $V_{OS}$ | Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$. |
| | $V_{OX\ (AC)}$ | AC differential output cross point voltage: the voltage at which the differential output signals must cross. |
| | $V_{REF}$ | Reference voltage for the SSTL and HSTL I/O standards. |
| | $V_{REF\ (AC)}$ | AC input reference voltage for the SSTL and HSTL I/O standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise. The peak-to-peak AC noise on $V_{REF}$ must not exceed 2% of $V_{REF(DC)}$. |
| | $V_{REF\ (DC)}$ | DC input reference voltage for the SSTL and HSTL I/O standards. |
| | $V_{SWING\ (AC)}$ | AC differential input voltage: AC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms. |
| | $V_{SWING\ (DC)}$ | DC differential input voltage: DC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms. |
| | $V_{TT}$ | Termination voltage for the SSTL and HSTL I/O standards. |
| | $V_{X\ (AC)}$ | AC differential input cross point voltage: The voltage at which the differential input signals must cross. |
| **W** | — | — |
| **X** | — | — |
| **Y** | — | — |
| **Z** | — | — |

# Document Revision History

Table 1–47 lists the revision history for this chapter.

**Table 1–47. Document Revision History**

| Date | Version | Changes |
|---|---|---|
| March 2016 | 2.0 | Updated note (5) in Table 1–21 to remove support for the N148 package. |
| October 2014 | 1.9 | Updated maximum value for $V_{CCD\_PLL}$ in Table 1–1.<br>Removed extended temperature note in Table 1–3. |
| December 2013 | 1.8 | Updated Table 1–21 by adding Note (15). |
| May 2013 | 1.7 | Updated Table 1–15 by adding Note (4). |
| October 2012 | 1.6 | ■ Updated the maximum value for $V_I$, $V_{CCD\_PLL}$, $V_{CCIO}$, $V_{CC\_CLKIN}$, $V_{CCH\_GXB}$, and $V_{CCA\_GXB}$ Table 1–1.<br>■ Updated Table 1–11 and Table 1–22.<br>■ Updated Table 1–21 to include peak-to-peak differential input voltage for the Cyclone IV GX transceiver input reference clock.<br>■ Updated Table 1–29 to include the typical `DCLK` value.<br>■ Updated the minimum $f_{HSCLK}$ value in Table 1–31, Table 1–32, Table 1–33, Table 1–34, and Table 1–35. |
| November 2011 | 1.5 | ■ Updated “Maximum Allowed Overshoot or Undershoot Voltage”, “Operating Conditions”, and “PLL Specifications” sections.<br>■ Updated Table 1–2, Table 1–3, Table 1–4, Table 1–5, Table 1–8, Table 1–9, Table 1–15, Table 1–18, Table 1–19, and Table 1–21.<br>■ Updated Figure 1–1. |
| December 2010 | 1.4 | ■ Updated for the Quartus II software version 10.1 release.<br>■ Updated Table 1–21 and Table 1–25.<br>■ Minor text edits. |
| July 2010 | 1.3 | Updated for the Quartus II software version 10.0 release:<br>■ Updated Table 1–3, Table 1–4, Table 1–21, Table 1–25, Table 1–28, Table 1–30, Table 1–40, Table 1–41, Table 1–42, Table 1–43, Table 1–44, and Table 1–45.<br>■ Updated Figure 1–2 and Figure 1–3.<br>■ Removed SW Requirement and TCCS for Cyclone IV Devices tables.<br>■ Minor text edits. |
| March 2010 | 1.2 | Updated to include automotive devices:<br>■ Updated the “Operating Conditions” and “PLL Specifications” sections.<br>■ Updated Table 1–1, Table 1–8, Table 1–9, Table 1–21, Table 1–26, Table 1–27, Table 1–31, Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–36, Table 1–37, Table 1–38, Table 1–40, Table 1–42, and Table 1–43.<br>■ Added Table 1–5 to include ESD for Cyclone IV devices GPIOs and HSSI I/Os.<br>■ Added Table 1–44 and Table 1–45 to include IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.<br>■ Minor text edits. |