Intel - EP4CGX22CF19I7 Datasheet





Welcome to <u>E-XFL.COM</u>

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1330
Number of Logic Elements/Cells	21280
Total RAM Bits	774144
Number of I/O	150
Number of Gates	-
Voltage - Supply	1.16V ~ 1.24V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	324-LBGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4cgx22cf19i7

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Cyclone IV E industrial devices I7 are offered with extended operating temperature range.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone IV devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Table 1–1 lists the absolute maximum ratings for Cyclone IV devices.



Conditions beyond those listed in Table 1–1 cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time have adverse effects on the device.

Symbol	Parameter	Min	Max	Unit
V _{CCINT}	Core voltage, PCI Express [®] (PCIe [®]) hard IP block, and transceiver physical coding sublayer (PCS) power supply	-0.5	1.8	V
V _{CCA}	Phase-locked loop (PLL) analog power supply	-0.5	3.75	V
V _{CCD_PLL}	PLL digital power supply	-0.5	1.8	V
V _{CCIO}	I/O banks power supply	-0.5	3.75	V
V_{CC_CLKIN}	Differential clock input pins power supply	-0.5	4.5	V
V_{CCH_GXB}	Transceiver output buffer power supply	-0.5	3.75	V
V _{CCA_GXB}	Transceiver physical medium attachment (PMA) and auxiliary power supply	-0.5	3.75	V
V _{CCL_GXB}	Transceiver PMA and auxiliary power supply	-0.5	1.8	V
VI	DC input voltage	-0.5	4.2	V
I _{OUT}	DC output current, per pin	-25	40	mA
T _{STG}	Storage temperature	-65	150	0°
TJ	Operating junction temperature	-40	125	O°

Table 1–1. Absolute Maximum Ratings for Cyclone IV Devices (1)

Note to Table 1–1:

(1) Supply voltage specifications apply to voltage readings taken at the device pins with respect to ground, not at the power supply.

Maximum Allowed Overshoot or Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to –2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns. Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device.

DC Characteristics

This section lists the I/O leakage current, pin capacitance, on-chip termination (OCT) tolerance, and bus hold specifications for Cyclone IV devices.

Supply Current

The device supply current requirement is the minimum current drawn from the power supply pins that can be used as a reference for power size planning. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary greatly with the resources used. Table 1–6 lists the I/O pin leakage current for Cyclone IV devices.

Table 1–6. I/O Pin Leakage Current for Cyclone IV Devices (1), (2)

Symbol	Parameter	Conditions	Device	Min	Тур	Max	Unit
I _I	Input pin leakage current	$V_I = 0 V \text{ to } V_{\text{CCIOMAX}}$	—	-10	_	10	μA
I _{OZ}	Tristated I/O pin leakage current	$V_0 = 0 V \text{ to } V_{\text{CCIOMAX}}$		-10		10	μA

Notes to Table 1-6:

(1) This value is specified for normal device operation. The value varies during device power-up. This applies for all V_{CCI0} settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) The 10 μ A I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

Bus Hold

The bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1–7 lists bus hold specifications for Cyclone IV devices.

 Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 1 of 2)⁽¹⁾

		V _{CCI0} (V)												
Parameter	Condition	1	.2	1	.5	1.8		2.5		3.0		3.3		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus hold low, sustaining current	V _{IN} > V _{IL} (maximum)	8	_	12	_	30	_	50	_	70	_	70	_	μΑ
Bus hold high, sustaining current	V _{IN} < V _{IL} (minimum)	-8	_	-12	_	-30	_	-50	_	-70	_	-70	_	μΑ
Bus hold low, overdrive current	$0 V < V_{IN} < V_{CCIO}$	_	125	_	175	_	200	_	300	_	500		500	μA
Bus hold high, overdrive current	$0 V < V_{IN} < V_{CCIO}$		-125		-175		-200		-300		-500		-500	μΑ

Example 1–1 shows how to calculate the change of 50- Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

Example 1–1. Impedance Change

$$\begin{split} \Delta R_V &= (3.15-3) \times 1000 \times -0.026 = -3.83 \\ \Delta R_T &= (85-25) \times 0.262 = 15.72 \\ \text{Because } \Delta R_V \text{ is negative,} \\ MF_V &= 1 \ / \ (3.83/100 + 1) = 0.963 \\ \text{Because } \Delta R_T \text{ is positive,} \\ MF_T &= 15.72/100 + 1 = 1.157 \\ MF &= 0.963 \times 1.157 = 1.114 \\ R_{\text{final}} &= 50 \times 1.114 = 55.71 \ \Omega \end{split}$$

Pin Capacitance

Table 1–11 lists the pin capacitance for Cyclone IV devices.

Table 1–11.	Pin Ca	pacitance 1	for C	vclone IV	Devices	(1)
-------------	--------	-------------	-------	-----------	---------	-----

Symbol	Parameter	Typical – Quad Flat Pack (QFP)	Typical – Quad Flat No Leads (QFN)	Typical – Ball-Grid Array (BGA)	Unit
C _{IOTB}	Input capacitance on top and bottom I/O pins	7	7	6	pF
C _{IOLR}	Input capacitance on right I/O pins	7	7	5	pF
C _{LVDSLR}	Input capacitance on right I/O pins with dedicated LVDS output	8	8	7	pF
C _{VREFLR}	Input capacitance on right dual-purpose ${\tt VREF}$ pin when used as $V_{\sf REF}$ or user I/O pin	21	21	21	pF
C _{VREFTB}	Input capacitance on top and bottom dual-purpose \mathtt{VREF} pin when used as $V_{\textrm{REF}}$ or user I/O pin	23 <i>(3)</i>	23	23	pF
C _{CLKTB}	Input capacitance on top and bottom dedicated clock input pins	7	7	6	pF
C _{CLKLR}	Input capacitance on right dedicated clock input pins	6	6	5	pF

Notes to Table 1-11:

(1) The pin capacitance applies to FBGA, UBGA, and MBGA packages.

(2) When you use the vref pin as a regular input or output, you can expect a reduced performance of toggle rate and t_{CO} because of higher pin capacitance.

(3) C_{VREFTB} for the EP4CE22 device is 30 pF.

Schmitt Trigger Input

Cyclone IV devices support Schmitt trigger input on the TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rate. Table 1–14 lists the hysteresis specifications across the supported V_{CCIO} range for Schmitt trigger inputs in Cyclone IV devices.

 Table 1–14.
 Hysteresis Specifications for Schmitt Trigger Input in Cyclone IV Devices

Symbol	Parameter	Conditions (V)	Minimum	Unit
		V _{CCI0} = 3.3	200	mV
V _{SCHMITT}	Hysteresis for Schmitt trigger	V _{CCI0} = 2.5	200	mV
	input	V _{CCI0} = 1.8	140	mV
		V _{CCI0} = 1.5	110	mV

I/O Standard Specifications

The following tables list input voltage sensitivities (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}), for various I/O standards supported by Cyclone IV devices. Table 1–15 through Table 1–20 provide the I/O standard specifications for Cyclone IV devices.

1/0 Standard		V _{ccio} (V)	V,	_{IL} (V)	V	/ _{IH} (V)	V _{OL} (V)	V _{OH} (V)	l _{oL}	I _{OH}
i/u Stanuaru	Min	Тур	Max	Min	Max	Min	Max	Max	Min	(IIIA) (4)	(IIIA) (4)
3.3-V LVTTL <i>(3)</i>	3.135	3.3	3.465	—	0.8	1.7	3.6	0.45	2.4	4	-4
3.3-V LVCMOS (3)	3.135	3.3	3.465	—	0.8	1.7	3.6	0.2	$V_{CCI0} - 0.2$	2	-2
3.0-V LVTTL (3)	2.85	3.0	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.45	2.4	4	-4
3.0-V LVCMOS (3)	2.85	3.0	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.2	$V_{CCI0} - 0.2$	0.1	-0.1
2.5 V ⁽³⁾	2.375	2.5	2.625	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.4	2.0	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 x V _{CCI0}	0.65 x V _{CCI0}	2.25	0.45	V _{CCI0} – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 x V _{CCIO}	0.65 x V _{CCI0}	V _{CCI0} + 0.3	0.25 x V _{CCIO}	0.75 x V _{CCIO}	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 x V _{CCI0}	0.65 x V _{CCI0}	V _{CCI0} + 0.3	0.25 x V _{CCIO}	0.75 x V _{CCIO}	2	-2
3.0-V PCI	2.85	3.0	3.15		0.3 x V _{CCIO}	0.5 x V _{CCIO}	V _{CCI0} + 0.3	0.1 x V _{CCIO}	0.9 x V _{CCIO}	1.5	-0.5
3.0-V PCI-X	2.85	3.0	3.15	_	0.35 x V _{CCI0}	0.5 x V _{CCI0}	V _{CCI0} + 0.3	$0.1 ext{ x V}_{\text{CCIO}}$	0.9 x V _{ccio}	1.5	-0.5

Table 1–15. Single-Ended I/O Standard Specifications for Cyclone IV Devices (1), (2)

Notes to Table 1–15:

(1) For voltage-referenced receiver input waveform and explanation of terms used in Table 1–15, refer to "Glossary" on page 1–37.

(2) AC load CL = 10 pF

(3) For more information about interfacing Cyclone IV devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards, refer to AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems.

(4) To meet the loL and IoH specifications, you must set the current strength settings accordingly. For example, to meet the **3.3-V LVTTL** specification (4 mA), set the current strength settings to 4 mA or higher. Setting at lower current strength may not meet the loL and IoH specifications in the handbook.

1/0 Standard		V _{ccio} (V)		V _{ID} ((mV)		V _{IcM} (V) ⁽²⁾	V _{OD} (mV) ⁽³⁾			V _{0S} (V) ⁽³⁾			
i/U Stanuaru	Min	Тур	Max	Min	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max
						0.05	$D_{MAX} \leq \ 500 \ Mbps$	1.80						
Column (Column	2.375	2.5	2.625	100	_	0.55	$\begin{array}{l} 500 \text{ Mbps} \leq \text{D}_{\text{MAX}} \\ \leq \ 700 \text{ Mbps} \end{array}$	1.80	247	_	600	1.125	1.25	1.375
1,00)						1.05	D _{MAX} > 700 Mbps	1.55						
BLVDS (Row I/Os) ⁽⁴⁾	2.375	2.5	2.625	100	_	_	_	_	_	_	_	_	_	_
BLVDS (Column I/Os) ⁽⁴⁾	2.375	2.5	2.625	100			_			_		_		
mini-LVDS (Row I/Os) <i>(5)</i>	2.375	2.5	2.625		_	_	_		300	_	600	1.0	1.2	1.4
mini-LVDS (Column I/Os) ⁽⁵⁾	2.375	2.5	2.625				_		300		600	1.0	1.2	1.4
RSDS®(Row I/Os) ⁽⁵⁾	2.375	2.5	2.625	_	_			_	100	200	600	0.5	1.2	1.5
RSDS (Column I/Os) ⁽⁵⁾	2.375	2.5	2.625				_		100	200	600	0.5	1.2	1.5
PPDS (Row I/Os) <i>(5</i>)	2.375	2.5	2.625	_	_			_	100	200	600	0.5	1.2	1.4
PPDS (Column I/Os) ⁽⁵⁾	2.375	2.5	2.625			_	_		100	200	600	0.5	1.2	1.4

Table 1-20.	Differential I/O Standard S	pecifications for C	yclone IV Devices ⁽¹⁾	(Part 2 of 2)
-------------	-----------------------------	---------------------	----------------------------------	---------------

Notes to Table 1-20:

(1) For an explanation of terms used in Table 1–20, refer to "Glossary" on page 1–37.

(2) $~V_{IN}$ range: 0 V $\leq V_{IN} \leq$ 1.85 V.

 $(3) \quad R_L \text{ range: } 90 \leq \ R_L \leq \ 110 \ \Omega \, .$

(4) There are no fixed $V_{\rm IN},\,V_{\rm OD},\,\text{and}\,\,V_{\rm OS}$ specifications for BLVDS. They depend on the system topology.

(5) The Mini-LVDS, RSDS, and PPDS standards are only supported at the output pins.

(6) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported for output pins.

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 4 of 4)

Symbol/	Conditiono		C6			C7, 17			C8	Unit	
Description	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
PLD-Transceiver Inte	-Transceiver Interface										
Interface speed (F324 and smaller package)		25	_	125	25	_	125	25	_	125	MHz
Interface speed (F484 and larger package)	_	25	_	156.25	25	_	156.25	25	_	156.25	MHz
Digital reset pulse width	_		Minimum is 2 parallel clock cycles								

Notes to Table 1–21:

(1) This specification is valid for transmitter output jitter specification with a maximum total jitter value of 112 ps, typically for 3.125 Gbps SRIO and XAUI protocols.

(2) The minimum reconfig_clk frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter Only** mode. The minimum reconfig_clk frequency is 37.5 MHz if the transceiver channel is configured in **Receiver Only** or **Receiver and Transmitter** mode.

- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The rate matcher supports only up to ±300 parts per million (ppm).
- (5) Supported for the F169 and F324 device packages only.
- (6) Supported for the F484, F672, and F896 device packages only. Pending device characterization.
- (7) To support CDR ppm tolerance greater than ±300 ppm, implement ppm detector in user logic and configure CDR to Manual Lock Mode.
- (8) Asynchronous spread-spectrum clocking is not supported.
- (9) For the EP4CGX30 (F484 package only), EP4CGX50, and EP4CGX75 devices, the CDR ppl tolerance is ±200 ppm.
- (10) Time taken until pll_locked goes high after pll_powerdown deasserts.
- (11) Time that the CDR must be kept in lock-to-reference mode after rx_analogreset deasserts and before rx_locktodata is asserted in manual mode.

(12) Time taken to recover valid data after the rx_locktodata signal is asserted in manual mode (Figure 1–2), or after rx_freqlocked signal goes high in automatic mode (Figure 1–3).

(13) Time taken to recover valid data after the rx_locktodata signal is asserted in manual mode.

- (14) Time taken to recover valid data after the $rx_freqlocked$ signal goes high in automatic mode.
- (15) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Figure 1–2 shows the lock time parameters in manual mode.

LTD = lock-to-data. LTR = lock-to-reference.



Figure 1–2. Lock Time Parameters for Manual Mode

Figure 1–3 shows the lock time parameters in automatic mode.

Figure 1–3. Lock Time Parameters for Automatic Mode



Table 1–23 lists the Cyclone IV GX transceiver block AC specifications.

Symbol/	Conditions		C6			C 7, I7	7			llnit	
Description	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UNIT
PCIe Transmit Jitter Gene	ration ⁽³⁾										
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	_	_	0.25	_	_	0.25	_	_	0.25	UI
PCIe Receiver Jitter Toler	ance ⁽³⁾										
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern		> 0.6	;		> 0.6			> 0.6	j	UI
GIGE Transmit Jitter Gene	ration ⁽⁴⁾										
Deterministic jitter	Pattern - CRPAT			0.1/			0.1/			0.1/	111
(peak-to-peak)				0.14			0.14			0.14	01
Total jitter (peak-to-peak)	Pattern = CRPAT	_	—	0.279		—	0.279	_	_	0.279	UI
GIGE Receiver Jitter Toler	ance ⁽⁴⁾										
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4		UI	
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT		> 0.66			> 0.6	6		> 0.6	6	UI

Table 1–23. Transceiver Block AC Specification for Cyclone IV GX Devices (1), (2)

Notes to Table 1-23:

(1) Dedicated refclk pins were used to drive the input reference clocks.

(2) The jitter numbers specified are valid for the stated conditions only.

(3) The jitter numbers for PIPE are compliant to the PCIe Base Specification 2.0.

(4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.

Core Performance Specifications

The following sections describe the clock tree specifications, PLLs, embedded multiplier, memory block, and configuration specifications for Cyclone IV Devices.

Clock Tree Specifications

Table 1–24 lists the clock tree specifications for Cyclone IV devices.

 Table 1–24.
 Clock Tree Performance for Cyclone IV Devices (Part 1 of 2)

Device	Performance													
Device	C6	C7	C8	C8L ⁽¹⁾	C9L ⁽¹⁾	17	18L ⁽¹⁾	A7	Unit					
EP4CE6	500	437.5	402	362	265	437.5	362	402	MHz					
EP4CE10	500	437.5	402	362	265	437.5	362	402	MHz					
EP4CE15	500	437.5	402	362	265	437.5	362	402	MHz					
EP4CE22	500	437.5	402	362	265	437.5	362	402	MHz					
EP4CE30	500	437.5	402	362	265	437.5	362	402	MHz					
EP4CE40	500	437.5	402	362	265	437.5	362	402	MHz					

Dovice	Performance												
Device	C6	C7	C8	C8L ⁽¹⁾	C9L ⁽¹⁾	17	18L ⁽¹⁾	A7	Unit				
EP4CE55	500	437.5	402	362	265	437.5	362	—	MHz				
EP4CE75	500	437.5	402	362	265	437.5	362	—	MHz				
EP4CE115	—	437.5	402	362	265	437.5	362	—	MHz				
EP4CGX15	500	437.5	402		—	437.5	_	—	MHz				
EP4CGX22	500	437.5	402	—	—	437.5	—	—	MHz				
EP4CGX30	500	437.5	402	—	—	437.5	—	—	MHz				
EP4CGX50	500	437.5	402		—	437.5	_	—	MHz				
EP4CGX75	500	437.5	402	—	—	437.5	—	—	MHz				
EP4CGX110	500	437.5	402	—	—	437.5	—	—	MHz				
EP4CGX150	500	437.5	402		—	437.5		_	MHz				

Table 1–24. Clock Tree Performance for Cyclone IV Devices (Part 2 of 2)

Note to Table 1-24:

(1) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades.

PLL Specifications

Table 1–25 lists the PLL specifications for Cyclone IV devices when operating in the commercial junction temperature range (0°C to 85°C), the industrial junction temperature range (–40°C to 100°C), the extended industrial junction temperature range (–40°C to 125°C), and the automotive junction temperature range (–40°C to 125°C). For more information about the PLL block, refer to "Glossary" on page 1–37.

 Table 1–25.
 PLL Specifications for Cyclone IV Devices ^{(1), (2)} (Part 1 of 2)

Symbol	Parameter	Min	Тур	Max	Unit
	Input clock frequency (-6, -7, -8 speed grades)	5	—	472.5	MHz
f _{IN} (3)	Input clock frequency (-8L speed grade)	5	_	362	MHz
	Input clock frequency (–9L speed grade)	5	—	265	MHz
f _{INPFD}	PFD input frequency	5	_	325	MHz
f _{VCO} (4)	PLL internal VCO operating range	600	—	1300	MHz
f _{INDUTY}	Input clock duty cycle	40	—	60	%
t _{injitter_CCJ} <i>(5)</i>	Input clock cycle-to-cycle jitter $F_{REF} \geq 100 \mbox{ MHz}$	_	_	0.15	UI
	F _{REF} < 100 MHz		_	±750	ps
f _{OUT_EXT} (external clock output) ⁽³⁾	PLL output frequency		_	472.5	MHz
	PLL output frequency (-6 speed grade)	_	_	472.5	MHz
	PLL output frequency (-7 speed grade)	_	—	450	MHz
f _{OUT} (to global clock)	PLL output frequency (-8 speed grade)		_	402.5	MHz
	PLL output frequency (-8L speed grade)		—	362	MHz
	PLL output frequency (-9L speed grade)		—	265	MHz
toutduty	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t _{LOCK}	Time required to lock from end of device configuration	_	_	1	ms

Symbol	Modes		C6			C7, I	7		C8, A	7		C8L, I	8L		C9L		Ilnit
Symbol	WOUCS	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
t _{LOCK} (3)	_			1			1	_		1			1	_		1	ms

Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (2), (4)} (Part 2 of 2)

Notes to Table 1-31:

(1) Applicable for true RSDS and emulated RSDS_E_3R transmitter.

(2) Cyclone IV E devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated RSDS transmitter is supported at the output pin of all I/O Banks. Cyclone IV GX devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the

pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
(3) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Ormshall	Madaa		C6			C7, 17	1		C8, A	7		C8L, I8	BL		C9L		11
Symbol	wodes	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
	×10	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×8	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
f _{HSCLK} (input	×7	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
frequency)	×4	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×2	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×1	5	—	170	5	—	170	5	—	170	5	—	170	5	—	145	MHz
	×10	100	—	170	100	—	170	100	—	170	100	—	170	100	—	145	Mbps
	×8	80	—	170	80	—	170	80	—	170	80	—	170	80	—	145	Mbps
Device	×7	70	—	170	70	—	170	70	—	170	70	—	170	70	—	145	Mbps
Mbps	×4	40	—	170	40	—	170	40	—	170	40	—	170	40	—	145	Mbps
	×2	20	—	170	20	—	170	20	—	170	20	—	170	20	—	145	Mbps
	×1	10	—	170	10	—	170	10	—	170	10	—	170	10	—	145	Mbps
t _{DUTY}	_	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS	_	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	_	_	_	500	_	_	500	_	_	550	_	_	600	_	_	700	ps
t _{RISE}	20 - 80%, C _{LOAD} = 5 pF	_	500	_	_	500	_	_	500	_	_	500	_	_	500	_	ps
t _{FALL}	20 - 80%, C _{LOAD} = 5 pF	_	500	_	_	500	_	_	500	_	_	500	_	_	500	_	ps

Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 1 of 2)

Symbol	Modes		C6			C7, 17	,		C8, A7	7		C8L, 18	8L		C9L		llnit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UIII
t _{LOCK} (2)	—	—	—	1			1		_	1	—		1	—	—	1	ms

Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 2 of 2)

Notes to Table 1-32:

(1) Emulated RSDS_E_1R transmitter is supported at the output pin of all I/O Banks of Cyclone IV E devices and I/O Banks 3, 4, 5, 6, 7, 8, and 9 of Cyclone IV GX devices.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Symbol	Madaa		C6			C7, I	7		C8, A	7		C8L, I	8L		C9L		11
Symbol	wodes	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UNIT
	×10	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5		132.5	MHz
	×8	5		200	5		155.5	5		155.5	5		155.5	5		132.5	MHz
f _{HSCLK} (input	×7	5		200	5		155.5	5		155.5	5		155.5	5		132.5	MHz
frequency)	×4	5	—	200	5	—	155.5	5	—	155.5	5		155.5	5	_	132.5	MHz
	×2	5	—	200	5		155.5	5		155.5	5	—	155.5	5		132.5	MHz
	×1	5	—	400	5	—	311	5	—	311	5	—	311	5		265	MHz
	×10	100	—	400	100	—	311	100	—	311	100	—	311	100	_	265	Mbps
	×8	80	—	400	80		311	80		311	80		311	80	_	265	Mbps
Device	×7	70	—	400	70	—	311	70		311	70	—	311	70		265	Mbps
Mbps	×4	40	—	400	40	—	311	40	—	311	40	—	311	40	_	265	Mbps
	×2	20	—	400	20	_	311	20	_	311	20	_	311	20	_	265	Mbps
	×1	10	—	400	10	—	311	10		311	10	—	311	10		265	Mbps
t _{DUTY}	_	45	—	55	45	—	55	45	—	55	45	—	55	45	_	55	%
TCCS		—	—	200	—		200	_		200	—		200	—	_	200	ps
Output jitter (peak to peak)	_	_	_	500	_	_	500		_	550	_	_	600	_		700	ps
t _{RISE}	20 - 80%, C _{LOAD} = 5 pF	_	500	_	_	500			500	_	_	500	_	_	500	_	ps
t _{FALL}	20 - 80%, C _{LOAD} = 5 pF	_	500	_	_	500	_	_	500	_	_	500	_	_	500		ps
t _{LOCK} (3)	—	—	—	1	—		1	—		1	—		1	—	—	1	ms

Table 1–33. Mini-LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4)

Notes to Table 1-33:

(1) Applicable for true and emulated mini-LVDS transmitter.

(2) Cyclone IV E—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated mini-LVDS transmitter is supported at the output pin of all I/O banks.
Cyclone IV CY—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of Row I/O Banks 5.

Cyclone IV GX—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(3) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Symbol	Madaa	C	6	C7,	, 17	C8,	A7	C8L	, 18L	C	9L	Unit
Symbol	MUUUUUS	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	UIII
t _{DUTY}	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	_	—	200	_	200	_	200		200	_	200	ps
Output jitter (peak to peak)	_	_	500	_	500	_	550	_	600	_	700	ps
t _{LOCK} (2)		—	1	_	1	_	1	_	1	—	1	ms

Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 2 of 2)

Notes to Table 1-35:

(1) Cyclone IV E—emulated LVDS transmitter is supported at the output pin of all I/O Banks.

Cyclone IV GX—emulated LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Gumbal	Madaa	C	6	C7,	, 17	C8,	A7	C8L	, 18L	C	9L	11
Symbol	modes	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
	×10	10	437.5	10	370	10	320	10	320	10	250	MHz
	×8	10	437.5	10	370	10	320	10	320	10	250	MHz
f _{HSCLK} (input	×7	10	437.5	10	370	10	320	10	320	10	250	MHz
frequency)	×4	10	437.5	10	370	10	320	10	320	10	250	MHz
1 57	×2	10	437.5	10	370	10	320	10	320	10	250	MHz
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	MHz
	×10	100	875	100	740	100	640	100	640	100	500	Mbps
	×8	80	875	80	740	80	640	80	640	80	500	Mbps
	×7	70	875	70	740	70	640	70	640	70	500	Mbps
HOIDDA	×4	40	875	40	740	40	640	40	640	40	500	Mbps
	×2	20	875	20	740	20	640	20	640	20	500	Mbps
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	Mbps
SW	—	_	400	_	400	_	400	_	550	_	640	ps
Input jitter tolerance	_	_	500	_	500	_	550	_	600	_	700	ps
t _{LOCK} (2)	—	—	1	—	1	—	1	—	1	—	1	ms

Table 1–36. LVDS Receiver Timing Specifications for Cyclone IV Devices (1), (3)

Notes to Table 1-36:

(1) Cyclone IV E—LVDS receiver is supported at all I/O Banks.

Cyclone IV GX—LVDS receiver is supported at I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

External Memory Interface Specifications

The external memory interfaces for Cyclone IV devices are auto-calibrating and easy to implement.

• For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interface Handbook*.

Table 1–37 lists the memory output clock jitter specifications for Cyclone IV devices.

Table 1–37. Memory Output Clock Jitter Specifications for Cyclone IV Devices (1), (2)

Parameter	Symbol	Min	Max	Unit
Clock period jitter	t _{JIT(per)}	-125	125	ps
Cycle-to-cycle period jitter	t _{JIT(cc)}	-200	200	ps
Duty cycle jitter	t _{JIT(duty)}	-150	150	ps

Notes to Table 1-37:

(1) Memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2 standard.

(2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock (GCLK) network.

Duty Cycle Distortion Specifications

Table 1–38 lists the worst case duty cycle distortion for Cyclone IV devices.

Table 1–38. Duty Cycle Distortion on Cyclone IV Devices I/O Pins (1), (2), (3)

Symbol	C	6	C 7	, 17	C8, I8	BL, A7	C	9L	Unit
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Notes to Table 1-38:

(1) The duty cycle distortion specification applies to clock outputs from the PLLs, global clock tree, and IOE driving the dedicated and general purpose I/O pins.

(2) Cyclone IV devices meet the specified duty cycle distortion at the maximum output toggle rate for each combination of I/O standard and current strength.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

OCT Calibration Timing Specification

Table 1–39 lists the duration of calibration for series OCT with calibration at device power-up for Cyclone IV devices.

Table 1–39. Timing Specification for Series OCT with Calibration at Device Power-Up for Cyclone IV Devices $^{(1)}$

Symbol	Description	Maximum	Units
t _{octcal}	Duration of series OCT with calibration at device power-up	20	μs

Note to Table 1-39:

(1) OCT calibration takes place after device configuration and before entering user mode.

IOE Programmable Delay

Table 1–40 and Table 1–41 list the IOE programmable delay for Cyclone IV E 1.0 V core voltage devices.

Table 1–40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Device
--

	Paths Affected	Number of	Min Offset	Max Offset					
Parameter				Fast Corner		Slow Corner			Unit
		Setting		C8L	18L	C8L	C9L	18L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.054	1.924	3.387	4.017	3.411	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.010	1.875	3.341	4.252	3.367	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.641	0.631	1.111	1.377	1.124	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.971	0.931	1.684	2.298	1.684	ns

Notes to Table 1-40:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

		Number of Setting	Min Offset	Max Offset						
Parameter	Paths Affected			Fast Corner		Slow Corner			Unit	
				C8L	18L	C8L	C9L	18L		
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.057	1.921	3.389	4.146	3.412	ns	
Input delay from pin to input register	Pad to I/O input register	8	0	2.059	1.919	3.420	4.374	3.441	ns	
Delay from output register to output pin	I/O output register to pad	2	0	0.670	0.623	1.160	1.420	1.168	ns	
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.960	0.919	1.656	2.258	1.656	ns	

Notes to Table 1-41:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

		Numbor	Min Offset	Max Offset								
Parameter	Paths Affected	of		Fast Corner			Slow Corner					Unit
		Setting		C6	17	A7	C6	C7	C8	17	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.211	1.211	2.177	2.340	2.433	2.388	2.508	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.307	1.203	1.203	2.19	2.387	2.540	2.430	2.545	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.437	0.402	0.402	0.747	0.820	0.880	0.834	0.873	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.693	0.665	0.665	1.200	1.379	1.532	1.393	1.441	ns

Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices	(1),	(2)
---	------	-----

Notes to Table 1-42:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

		Numbor	Min Offset	Max Offset								
Parameter	Paths Affected	of Setting		Fast Corner			Slow Corner					Unit
				C6	17	A7	C6	C7	C8	17	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.209	1.209	2.201	2.386	2.510	2.429	2.548	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.207	1.207	2.202	2.402	2.558	2.447	2.557	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.458	0.419	0.419	0.783	0.861	0.924	0.875	0.915	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.686	0.657	0.657	1.185	1.360	1.506	1.376	1.422	ns

Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices (1), (2)

Notes to Table 1-43:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

Table 1-44.	IOE Programmable	Delay on Column	Pins for Cyclone	IV GX Devices ^{(1), (2)}
-------------	------------------	-----------------	-------------------------	-----------------------------------

		Numbor		Max Offset						
Parameter	Paths Affected	of Settings	Min Offset	Fast Corner		Slow Corner				Unit
				C6	17	C6	C7	C8	17	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.313	1.209	2.184	2.336	2.451	2.387	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.208	2.200	2.399	2.554	2.446	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.438	0.404	0.751	0.825	0.886	0.839	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.713	0.682	1.228	1.41	1.566	1.424	ns

Notes to Table 1-44:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

		Numbor		Max Offset						
Parameter	Paths Affected	of Settings	Min Offset	Fast Corner		Slow Corner				Unit
				C6	17	C6	C7	C8	17	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.210	2.209	2.398	2.526	2.443	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.313	1.208	2.205	2.406	2.563	2.450	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.461	0.421	0.789	0.869	0.933	0.884	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.712	0.682	1.225	1.407	1.562	1.421	ns

Table 1–45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices (1), (2)

Notes to Table 1-45:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software

I/O Timing

Use the following methods to determine I/O timing:

- the Excel-based I/O Timing
- the Quartus II timing analyzer

The Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get a timing budget estimation as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.

The Excel-based I/O Timing spreadsheet is downloadable from Cyclone IV Devices Literature website.

Glossary

Table 1–46 lists the glossary for this chapter.

Letter	Term	Definitions
Α	—	—
В		_
C	—	_
D	—	_
E	—	_
F	f _{HSCLK}	High-speed I/O block: High-speed receiver/transmitter input and output clock frequency.
C	GCLK	Input pin directly to Global Clock network.
u	GCLK PLL	Input pin to Global Clock network through the PLL.
Н	HSIODR	High-speed I/O block: Maximum/minimum LVDS data transfer rate (HSIODR = 1/TUI).
I	Input Waveforms for the SSTL Differential I/O Standard	Vswing Vswing V _{REF} V _{IL}

Table	1-46.	Glossarv	(Part 1	of 5)
10010		aloouij	(1 0 1 0 1	

Table 1-46. Glossary (Part 3 of 5)

Letter	Term	Definitions			
	RL	Receiver differential input discrete resistor (external to Cyclone IV devices).			
R		Receiver input waveform for LVDS and LVPECL differential standards:			
		Single-Ended Waveform			
		Positive Channel (p) = V _{IH}			
		V_{nL} Negative Channel (n) = V _{IL}			
		Ground			
	Waveform				
	Waveronni				
		Differential Waveform (Mathematical Function of Positive & Negative Channel)			
		p-n			
	Receiver input	High-speed I/O block: The total margin left after accounting for the sampling window and TCCS.			
	(RSKM)	RSKM = (TUI - SW - TCCS) / 2.			
S	Single-ended voltage- referenced I/O Standard SW (Sampling Window)				

Document Revision History

Table 1–47 lists the revision history for this chapter.

Date	Version	Changes
March 2016	2.0	Updated note (5) in Table 1–21 to remove support for the N148 package.
October 2014	10	Updated maximum value for V _{CCD_PLL} in Table 1–1.
Uclober 2014	1.9	Removed extended temperature note in Table 1–3.
December 2013	1.8	Updated Table 1–21 by adding Note (15).
May 2013	1.7	Updated Table 1–15 by adding Note (4).
	1.6	■ Updated the maximum value for V _I , V _{CCD_PLL} , V _{CCIO} , V _{CC_CLKIN} , V _{CCH_GXB} , and V _{CCA_GXB} Table 1–1.
		■ Updated Table 1–11 and Table 1–22.
October 2012		 Updated Table 1–21 to include peak-to-peak differential input voltage for the Cyclone IV GX transceiver input reference clock.
		■ Updated Table 1–29 to include the typical DCLK value.
		■ Updated the minimum f _{HSCLK} value in Table 1–31, Table 1–32, Table 1–33, Table 1–34, and Table 1–35.
	1.5	 Updated "Maximum Allowed Overshoot or Undershoot Voltage", "Operating Conditions", and "PLL Specifications" sections.
November 2011		■ Updated Table 1–2, Table 1–3, Table 1–4, Table 1–5, Table 1–8, Table 1–9, Table 1–15, Table 1–18, Table 1–19, and Table 1–21.
		■ Updated Figure 1–1.
	1.4	 Updated for the Quartus II software version 10.1 release.
December 2010		■ Updated Table 1–21 and Table 1–25.
		Minor text edits.
		Updated for the Quartus II software version 10.0 release:
		■ Updated Table 1–3, Table 1–4, Table 1–21, Table 1–25, Table 1–28, Table 1–30, Table 1–40, Table 1–41, Table 1–42, Table 1–43, Table 1–44, and Table 1–45.
July 2010	1.3	■ Updated Figure 1–2 and Figure 1–3.
		Removed SW Requirement and TCCS for Cyclone IV Devices tables.
		 Minor text edits.
		Updated to include automotive devices:
	1.2	 Updated the "Operating Conditions" and "PLL Specifications" sections.
March 2010		■ Updated Table 1–1, Table 1–8, Table 1–9, Table 1–21, Table 1–26, Table 1–27, Table 1–31, Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–36, Table 1–37, Table 1–38, Table 1–40, Table 1–42, and Table 1–43.
		Added Table 1–5 to include ESD for Cyclone IV devices GPIOs and HSSI I/Os.
		 Added Table 1–44 and Table 1–45 to include IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.
		 Minor text edits.

Table 1–47. Document Revision History

Date	Version	Changes
February 2010	1.1	 Updated Table 1–3 through Table 1–44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release. Minor text edits.
November 2009	1.0	Initial release.