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Details	
Product Status	Active
Number of LABs/CLBs	1840
Number of Logic Elements/Cells	29440
Total RAM Bits	1105920
Number of I/O	290
Number of Gates	-
Voltage - Supply	1.16V ~ 1.24V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4cgx30cf23c8

☞ A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit
V_i	AC Input Voltage	V_I = 4.20	100	%
		V_I = 4.25	98	%
		V_I = 4.30	65	%
		V_I = 4.35	43	%
		V_I = 4.40	29	%
		V_I = 4.45	20	%
		V_I = 4.50	13	%
		V_I = 4.55	9	%
		V_I = 4.60	6	%

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

Figure 1–1. Cyclone IV Devices Overshoot Duration

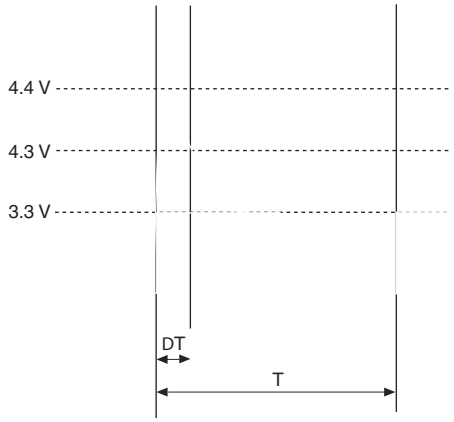


Table 1–4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA_GXB}	Transceiver PMA and auxiliary power supply	—	2.375	2.5	2.625	V
V_{CCL_GXB}	Transceiver PMA and auxiliary power supply	—	1.16	1.2	1.24	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	DC output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR) *(7)*	50 µs	—	50 ms	—
		Fast POR *(8)*	50 µs	—	3 ms	—
I_{Diode}	Magnitude of DC current across PCI-clamp diode when enabled	—	—	—	10	mA

Notes to Table 1–4:

(1) All VCCA pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.

(2) You must connect V_{CCD_PLL} to V_{CCINT} through a decoupling capacitor and ferrite bead.

(3) Power supplies must rise monotonically.

(4) V_{CCIO} for all I/O banks must be powered up during device operation. Configurations pins are powered up by V_{CCIO} of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support V_{CCIO} of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the V_{CCIO} level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.

(5) You must set V_{CC_CLKIN} to 2.5 V if you use CLKIN as a high-speed serial interface (HSSI) refclk or as a DIFFCLK input.

(6) The CLKIN pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.

(7) The POR time for Standard POR ranges between 50 and 200 ms. V_{CCINT}, V_{CCA}, and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.

(8) The POR time for Fast POR ranges between 3 and 9 ms. V_{CCINT}, V_{CCA}, and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1–5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

Table 1–5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os

Symbol	Parameter	Passing Voltage	Unit
V_{ESDHBM}	ESD voltage using the HBM (GPIOs) *(1)*	± 2000	V
	ESD using the HBM (HSSI I/Os) *(2)*	± 1000	V
V_{ESDCDM}	ESD using the CDM (GPIOs)	± 500	V
	ESD using the CDM (HSSI I/Os) *(2)*	± 250	V

Notes to Table 1–5:

(1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is ±1000V.

(2) This value is applicable only to Cyclone IV GX devices.

Internal Weak Pull-Up and Weak Pull-Down Resistor

Table 1–12 lists the weak pull-up and pull-down resistor values for Cyclone IV devices.

Table 1–12. Internal Weak Pull-Up and Weak Pull-Down Resistor Values for Cyclone IV Devices *(1)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{\_PU}$	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option	V_{CCIO} = 3.3 V ± 5% *(2), (3)*	7	25	41	kΩ
		V_{CCIO} = 3.0 V ± 5% *(2), (3)*	7	28	47	kΩ
		V_{CCIO} = 2.5 V ± 5% *(2), (3)*	8	35	61	kΩ
		V_{CCIO} = 1.8 V ± 5% *(2), (3)*	10	57	108	kΩ
		V_{CCIO} = 1.5 V ± 5% *(2), (3)*	13	82	163	kΩ
		V_{CCIO} = 1.2 V ± 5% *(2), (3)*	19	143	351	kΩ
$R_{\_PD}$	Value of the I/O pin pull-down resistor before and during configuration	V_{CCIO} = 3.3 V ± 5% *(4)*	6	19	30	kΩ
		V_{CCIO} = 3.0 V ± 5% *(4)*	6	22	36	kΩ
		V_{CCIO} = 2.5 V ± 5% *(4)*	6	25	43	kΩ
		V_{CCIO} = 1.8 V ± 5% *(4)*	7	35	71	kΩ
		V_{CCIO} = 1.5 V ± 5% *(4)*	8	50	112	kΩ

Notes to Table 1–12:

(1) All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(3) $R_{\_PU} = (V_{CCIO} – V_I)/I_{R\_PU}$
Minimum condition: –40°C; $V_{CCIO} = V_{CC}$ + 5%, $V_I = V_{CC}$ + 5% – 50 mV;
Typical condition: 25°C; $V_{CCIO} = V_{CC}$, V_I = 0 V;
Maximum condition: 100°C; $V_{CCIO} = V_{CC}$ – 5%, V_I = 0 V; in which V_I refers to the input voltage at the I/O pin.

(4) $R_{\_PD} = V_I/I_{R\_PD}$
Minimum condition: –40°C; $V_{CCIO} = V_{CC}$ + 5%, V_I = 50 mV;
Typical condition: 25°C; $V_{CCIO} = V_{CC}$, $V_I = V_{CC}$ – 5%;
Maximum condition: 100°C; $V_{CCIO} = V_{CC}$ – 5%, $V_I = V_{CC}$ – 5%; in which V_I refers to the input voltage at the I/O pin.

Hot-Socketing

Table 1–13 lists the hot-socketing specifications for Cyclone IV devices.

Table 1–13. Hot-Socketing Specifications for Cyclone IV Devices

Symbol	Parameter	Maximum
$I_{IOPIN(DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA *(1)*
$I_{XCVRTX(DC)}$	DC current per transceiver TX pin	100 mA
$I_{XCVRRX(DC)}$	DC current per transceiver RX pin	50 mA

Note to Table 1–13:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |IIOPIN| = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.

☞ During hot-socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

Table 1–16. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Cyclone IV Devices *(1)*

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V) *(2)*		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 x V_{CCIO} *(3)*	0.5 x V_{CCIO} *(3)*	0.52 x V_{CCIO} *(3)*	—	0.5 x V_{CCIO}	—
				0.47 x V_{CCIO} *(4)*	0.5 x V_{CCIO} *(4)*	0.53 x V_{CCIO} *(4)*			

Notes to Table 1–16:

(1) For an explanation of terms used in Table 1–16, refer to "Glossary" on page 1–37.
(2) V_{TT} of the transmitting device must track V_{REF} of the receiving device.
(3) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.
(4) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

Table 1–17. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone IV Devices

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.57	V_{TT} + 0.57	8.1	–8.1
SSTL-2 Class II	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.76	V_{TT} + 0.76	16.4	–16.4
SSTL-18 Class I	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	V_{TT} – 0.475	V_{TT} + 0.475	6.7	–6.7
SSTL-18 Class II	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	0.28	V_{CCIO} – 0.28	13.4	–13.4
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	14	–14

For more information about receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *I/O Features in Cyclone IV Devices* chapter.

Table 1–18. Differential SSTL I/O Standard Specifications for Cyclone IV Devices *(1)*

I/O Standard	V_{CCIO} (V)			$V_{Swing(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{Swing(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.7	V_{CCIO}	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$
SSTL-18 Class I, II	1.7	1.8	1.90	0.25	V_{CCIO}	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	V_{CCIO}	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$

Note to Table 1–18:

(1) Differential SSTL requires a V_{REF} input.

Table 1–19. Differential HSTL I/O Standard Specifications for Cyclone IV Devices *(1)*

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	$0.48 \times V_{CCIO}$	—	$0.52 \times V_{CCIO}$	$0.48 \times V_{CCIO}$	—	$0.52 \times V_{CCIO}$	0.3	$0.48 \times V_{CCIO}$

Note to Table 1–19:

(1) Differential HSTL requires a V_{REF} input.

Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices *(1)* **(Part 1 of 2)**

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) *(2)*			V_{OD} (mV) *(3)*			V_{OS} (V) *(3)*		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (Row I/Os) *(6)*	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq 500$ Mbps	1.80	—	—	—	—	—	—
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	$D_{MAX} >$ 700 Mbps	1.55						
LVPECL (Column I/Os) *(6)*	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.80	—	—	—	—	—	—
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	$D_{MAX} >$ 700 Mbps	1.55						
LVDS (Row I/Os)	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.80	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	$D_{MAX} >$ 700 Mbps	1.55						

Transceiver Performance Specifications

Table 1–21 lists the Cyclone IV GX transceiver specifications.

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 1 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	1.2 V PCML, 1.5 V PCML, 3.3 V PCML, Differential LVPECL, LVDS, HCSL										
Input frequency from REFCLK input pins	—	50	—	156.25	50	—	156.25	50	—	156.25	MHz
Spread-spectrum modulating clock frequency	Physical interface for PCI Express (PIPE) mode	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PIPE mode	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
Peak-to-peak differential input voltage	—	0.1	—	1.6	0.1	—	1.6	0.1	—	1.6	V
V_{ICM} (AC coupled)	—	1100 ± 5%			1100 ± 5%			1100 ± 5%			mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise *(1)*	Frequency offset = 1 MHz – 8 MHZ	—	—	–123	—	—	–123	—	—	–123	dBc/Hz
Transmitter REFCLK Total Jitter *(1)*		—	—	42.3	—	—	42.3	—	—	42.3	ps
R_{ref}	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clock											
cal_blk_clk clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 *(2)*	—	50	2.5/ 37.5 *(2)*	—	50	2.5/ 37.5 *(2)*	—	50	MHz
Delta time between reconfig_clk	—	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum power-down pulse width	—	—	1	—	—	1	—	—	1	—	µs

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 3 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Signal detect/loss threshold	PIPE mode	65	—	175	65	—	175	65	—	175	mV
t_{LTR} *(10)*	—	—	—	75	—	—	75	—	—	75	µs
$t_{LTR-LTD\_Manual}$ *(11)*	—	15	—	—	15	—	—	15	—	—	µs
t_{LTD} *(12)*	—	0	100	4000	0	100	4000	0	100	4000	ns
t_{LTD_Manual} *(13)*	—	—	—	4000	—	—	4000	—	—	4000	ns
t_{LTD_Auto} *(14)*	—	—	—	4000	—	—	4000	—	—	4000	ns
Receiver buffer and CDR offset cancellation time (per channel)	—	—	—	17000	—	—	17000	—	—	17000	reconfig_clk cycles
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	—	6	—	dB
Transmitter											
Supported I/O Standards	1.5 V PCML										
Data rate (F324 and smaller package)	—	600	—	2500	600	—	2500	600	—	2500	Mbps
Data rate (F484 and larger package)	—	600	—	3125	600	—	3125	600	—	2500	Mbps
V_{OCM}	0.65 V setting	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	Ω
	150–Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PIPE, CPRI LV, Serial Rapid I/O SR, SDI, XAUI, SATA	Compliant									—
Rise time	—	50	—	200	50	—	200	50	—	200	ps
Fall time	—	50	—	200	50	—	200	50	—	200	ps
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block skew	—	—	—	120	—	—	120	—	—	120	ps

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 4 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PLD-Transceiver Interface											
Interface speed (F324 and smaller package)	—	25	—	125	25	—	125	25	—	125	MHz
Interface speed (F484 and larger package)	—	25	—	156.25	25	—	156.25	25	—	156.25	MHz
Digital reset pulse width	—	Minimum is 2 parallel clock cycles									

Notes to Table 1–21:

(1) This specification is valid for transmitter output jitter specification with a maximum total jitter value of 112 ps, typically for 3.125 Gbps SRIO and XAUI protocols.

(2) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter Only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver Only** or **Receiver and Transmitter** mode.

(3) The device cannot tolerate prolonged operation at this absolute maximum.

(4) The rate matcher supports only up to ±300 parts per million (ppm).

(5) Supported for the F169 and F324 device packages only.

(6) Supported for the F484, F672, and F896 device packages only. Pending device characterization.

(7) To support CDR ppm tolerance greater than ±300 ppm, implement ppm detector in user logic and configure CDR to Manual Lock Mode.

(8) Asynchronous spread-spectrum clocking is not supported.

(9) For the EP4CGX30 (F484 package only), EP4CGX50, and EP4CGX75 devices, the CDR ppl tolerance is ±200 ppm.

(10) Time taken until `pll_locked` goes high after `pll_powerdown` deasserts.

(11) Time that the CDR must be kept in lock-to-reference mode after `rx_analogreset` deasserts and before `rx_locktodata` is asserted in manual mode.

(12) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode (Figure 1–2), or after `rx_freqlocked` signal goes high in automatic mode (Figure 1–3).

(13) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode.

(14) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode.

(15) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Figure 1–2 shows the lock time parameters in manual mode.

LTD = lock-to-data. LTR = lock-to-reference.

Figure 1–2. Lock Time Parameters for Manual Mode

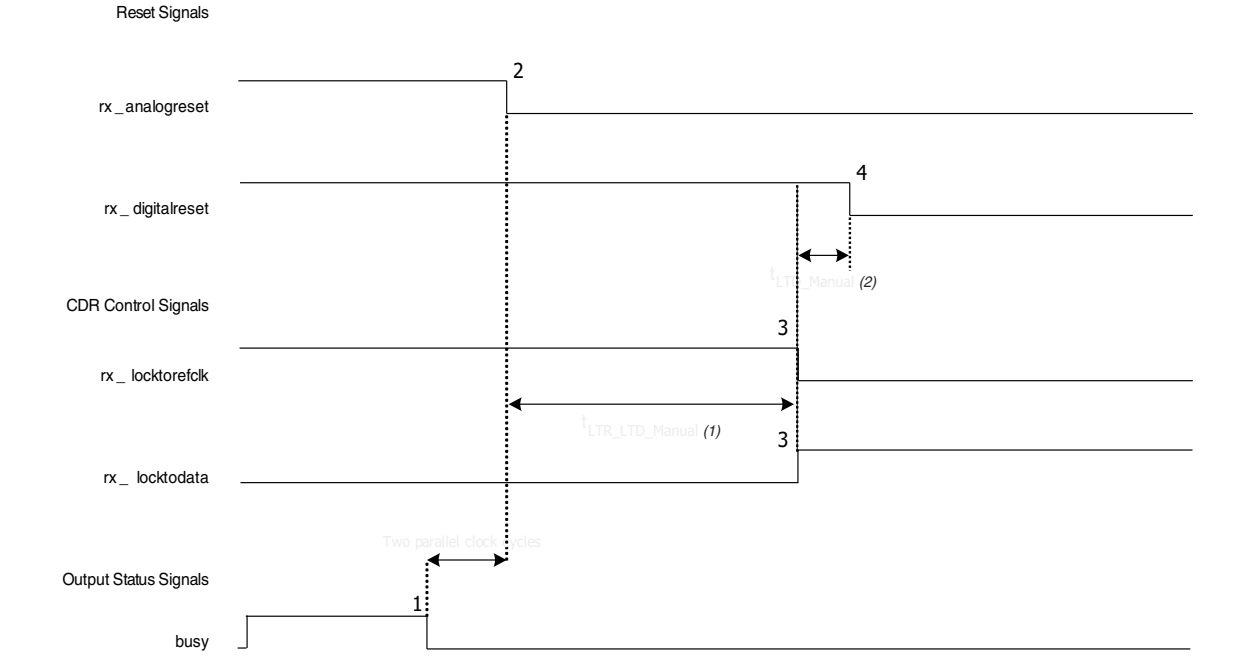


Figure 1–3 shows the lock time parameters in automatic mode.

Figure 1–3. Lock Time Parameters for Automatic Mode

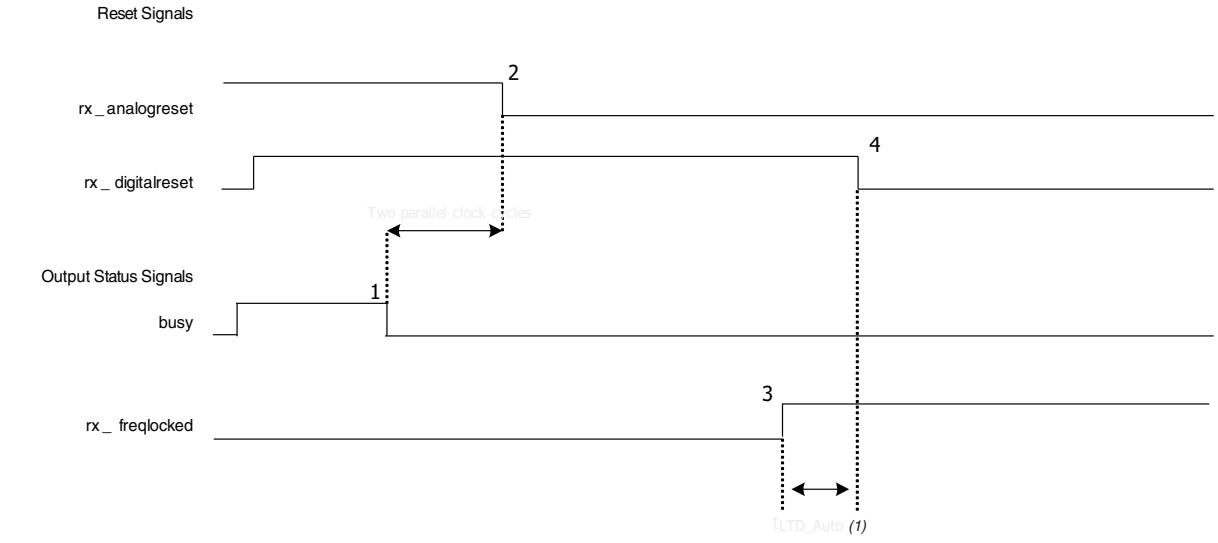


Table 1–25. PLL Specifications for Cyclone IV Devices (1), (2) (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or areset is deasserted)	—	—	1	ms
$t_{OUTJITTER\_PERIOD\_DEDCLK}$ (6)	Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER\_CCJ\_DEDCLK}$ (6)	Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER\_PERIOD\_IO}$ (6)	Regular I/O period jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER\_CCJ\_IO}$ (6)	Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal.	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	3.5 (7)	—	SCANCLK cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
$t_{CASC\_OUTJITTER\_PERIOD\_DEDCLK}$ (8), (9)	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	425	ps
	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz)	—	—	42.5	mUI

Notes to Table 1–25:

(1) This table is applicable for general purpose PLLs and multipurpose PLLs.

(2) You must connect V_{CCD_PLL} to V_{CCINT} through the decoupling capacitor and ferrite bead.

(3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(4) The V_{CO} frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the V_{CO} post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.

(6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.

(7) With 100-MHz scanclk frequency.

(8) The cascaded PLLs specification is applicable only with the following conditions:

- Upstream PLL—0.59 MHz ≤ Upstream PLL bandwidth < 1 MHz
- Downstream PLL—Downstream PLL bandwidth > 2 MHz

(9) PLL cascading is not supported for transceiver applications.

For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interfaces Handbook*.

Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 1–31 through Table 1–36 list the high-speed I/O timing for Cyclone IV devices. For definitions of high-speed timing specifications, refer to "Glossary" on page 1–37.

Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4) (Part 1 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×8	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×7	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×4	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×2	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×1	5	—	360	5	—	311	5	—	311	5	—	311	5	—	265	MHz
Device operation in Mbps	×10	100	—	360	100	—	311	100	—	311	100	—	311	100	—	265	Mbps
	×8	80	—	360	80	—	311	80	—	311	80	—	311	80	—	265	Mbps
	×7	70	—	360	70	—	311	70	—	311	70	—	311	70	—	265	Mbps
	×4	40	—	360	40	—	311	40	—	311	40	—	311	40	—	265	Mbps
	×2	20	—	360	20	—	311	20	—	311	20	—	311	20	—	265	Mbps
	×1	10	—	360	10	—	311	10	—	311	10	—	311	10	—	265	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
Transmitter channel-to-channel skew (TCCS)	—	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	—	—	700	ps
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps

Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 2 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{LOCK} (2)	—	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–32:

(1) Emulated RSDS_E_1R transmitter is supported at the output pin of all I/O Banks of Cyclone IV E devices and I/O Banks 3, 4, 5, 6, 7, 8, and 9 of Cyclone IV GX devices.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–33. Mini-LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×8	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×7	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×4	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×2	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×1	5	—	400	5	—	311	5	—	311	5	—	311	5	—	265	MHz
Device operation in Mbps	×10	100	—	400	100	—	311	100	—	311	100	—	311	100	—	265	Mbps
	×8	80	—	400	80	—	311	80	—	311	80	—	311	80	—	265	Mbps
	×7	70	—	400	70	—	311	70	—	311	70	—	311	70	—	265	Mbps
	×4	40	—	400	40	—	311	40	—	311	40	—	311	40	—	265	Mbps
	×2	20	—	400	20	—	311	20	—	311	20	—	311	20	—	265	Mbps
	×1	10	—	400	10	—	311	10	—	311	10	—	311	10	—	265	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	—	—	700	ps
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{LOCK} (3)	—	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–33:

(1) Applicable for true and emulated mini-LVDS transmitter.

(2) Cyclone IV E—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated mini-LVDS transmitter is supported at the output pin of all I/O banks.
Cyclone IV GX—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(3) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 2 of 2)

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{DUTY}	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	—	600	—	700	ps
t_{LOCK} (2)	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1–35:

(1) Cyclone IV E—emulated LVDS transmitter is supported at the output pin of all I/O Banks.
Cyclone IV GX—emulated LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–36. LVDS Receiver Timing Specifications for Cyclone IV Devices (1), (3)

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{HSCLK} (input clock frequency)	×10	10	437.5	10	370	10	320	10	320	10	250	MHz
	×8	10	437.5	10	370	10	320	10	320	10	250	MHz
	×7	10	437.5	10	370	10	320	10	320	10	250	MHz
	×4	10	437.5	10	370	10	320	10	320	10	250	MHz
	×2	10	437.5	10	370	10	320	10	320	10	250	MHz
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	MHz
HSIODR	×10	100	875	100	740	100	640	100	640	100	500	Mbps
	×8	80	875	80	740	80	640	80	640	80	500	Mbps
	×7	70	875	70	740	70	640	70	640	70	500	Mbps
	×4	40	875	40	740	40	640	40	640	40	500	Mbps
	×2	20	875	20	740	20	640	20	640	20	500	Mbps
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	Mbps
SW	—	—	400	—	400	—	400	—	550	—	640	ps
Input jitter tolerance	—	—	500	—	500	—	550	—	600	—	700	ps
t_{LOCK} (2)	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1–36:

(1) Cyclone IV E—LVDS receiver is supported at all I/O Banks.
Cyclone IV GX—LVDS receiver is supported at I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

External Memory Interface Specifications

The external memory interfaces for Cyclone IV devices are auto-calibrating and easy to implement.

For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interface Handbook*.

Table 1–37 lists the memory output clock jitter specifications for Cyclone IV devices.

Table 1–37. Memory Output Clock Jitter Specifications for Cyclone IV Devices *(1), (2)*

Parameter	Symbol	Min	Max	Unit
Clock period jitter	$t_{JIT(per)}$	–125	125	ps
Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–200	200	ps
Duty cycle jitter	$t_{JIT(duty)}$	–150	150	ps

Notes to Table 1–37:

(1) Memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2 standard.

(2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock (GCLK) network.

Duty Cycle Distortion Specifications

Table 1–38 lists the worst case duty cycle distortion for Cyclone IV devices.

Table 1–38. Duty Cycle Distortion on Cyclone IV Devices I/O Pins *(1), (2), (3)*

Symbol	C6		C7, I7		C8, I8L, A7		C9L		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Notes to Table 1–38:

(1) The duty cycle distortion specification applies to clock outputs from the PLLs, global clock tree, and IOE driving the dedicated and general purpose I/O pins.

(2) Cyclone IV devices meet the specified duty cycle distortion at the maximum output toggle rate for each combination of I/O standard and current strength.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

OCT Calibration Timing Specification

Table 1–39 lists the duration of calibration for series OCT with calibration at device power-up for Cyclone IV devices.

Table 1–39. Timing Specification for Series OCT with Calibration at Device Power-Up for Cyclone IV Devices *(1)*

Symbol	Description	Maximum	Units
t_{OCTCAL}	Duration of series OCT with calibration at device power-up	20	µs

Note to Table 1–39:

(1) OCT calibration takes place after device configuration and before entering user mode.

Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices *(1), (2)*

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset								Unit
				Fast Corner			Slow Corner					
				C6	I7	A7	C6	C7	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.211	1.211	2.177	2.340	2.433	2.388	2.508	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.307	1.203	1.203	2.19	2.387	2.540	2.430	2.545	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.437	0.402	0.402	0.747	0.820	0.880	0.834	0.873	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.693	0.665	0.665	1.200	1.379	1.532	1.393	1.441	ns

Notes to Table 1–42:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices *(1), (2)*

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset								Unit
				Fast Corner			Slow Corner					
				C6	I7	A7	C6	C7	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.209	1.209	2.201	2.386	2.510	2.429	2.548	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.207	1.207	2.202	2.402	2.558	2.447	2.557	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.458	0.419	0.419	0.783	0.861	0.924	0.875	0.915	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.686	0.657	0.657	1.185	1.360	1.506	1.376	1.422	ns

Notes to Table 1–43:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

Table 1–44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices *(1), (2)*

Parameter	Paths Affected	Number of Settings	Min Offset	Max Offset						Unit
				Fast Corner		Slow Corner				
				C6	I7	C6	C7	C8	I7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.313	1.209	2.184	2.336	2.451	2.387	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.208	2.200	2.399	2.554	2.446	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.438	0.404	0.751	0.825	0.886	0.839	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.713	0.682	1.228	1.41	1.566	1.424	ns

Notes to Table 1–44:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices *(1), (2)*

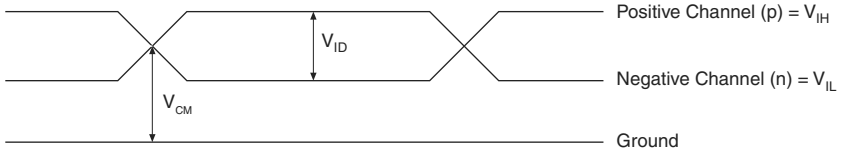
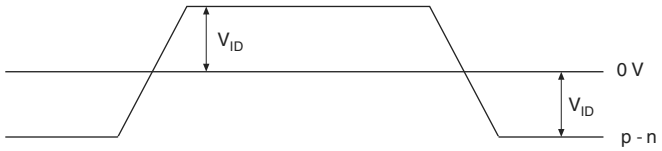
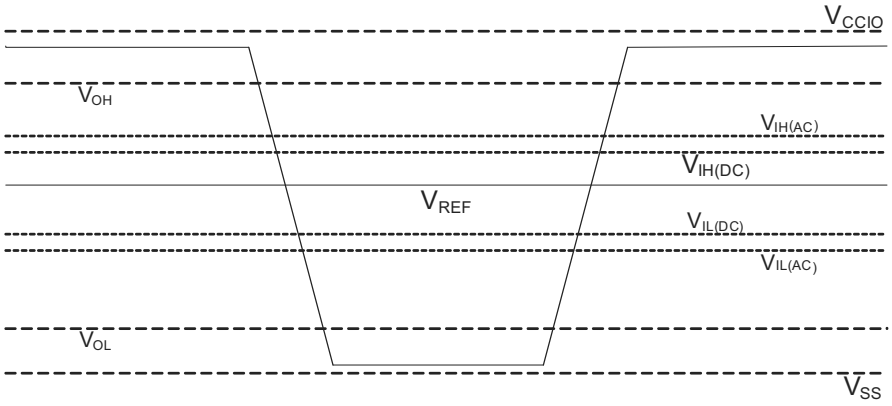
Parameter	Paths Affected	Number of Settings	Min Offset	Max Offset						Unit
				Fast Corner		Slow Corner				
				C6	I7	C6	C7	C8	I7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.210	2.209	2.398	2.526	2.443	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.313	1.208	2.205	2.406	2.563	2.450	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.461	0.421	0.789	0.869	0.933	0.884	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.712	0.682	1.225	1.407	1.562	1.421	ns

Notes to Table 1–45:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software

Table 1–46. Glossary (Part 3 of 5)

Letter	Term	Definitions
R	R_L	Receiver differential input discrete resistor (external to Cyclone IV devices).
	Receiver Input Waveform	Receiver input waveform for LVDS and LVPECL differential standards: **Single-Ended Waveform**  **Differential Waveform (Mathematical Function of Positive & Negative Channel)** 
	Receiver input skew margin (RSKM)	High-speed I/O block: The total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2.
S	Single-ended voltage-referenced I/O Standard	 The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform *ringing*.
	SW (Sampling Window)	High-speed I/O block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window.

Document Revision History

Table 1–47 lists the revision history for this chapter.

Table 1–47. Document Revision History

Date	Version	Changes
March 2016	2.0	Updated note (5) in Table 1–21 to remove support for the N148 package.
October 2014	1.9	Updated maximum value for V_{CCD_PLL} in Table 1–1. Removed extended temperature note in Table 1–3.
December 2013	1.8	Updated Table 1–21 by adding Note (15).
May 2013	1.7	Updated Table 1–15 by adding Note (4).
October 2012	1.6	■ Updated the maximum value for V_I, V_{CCD_PLL}, V_{CCIO}, V_{CC_CLKIN}, V_{CCH_GXB}, and V_{CCA_GXB} Table 1–1. ■ Updated Table 1–11 and Table 1–22. ■ Updated Table 1–21 to include peak-to-peak differential input voltage for the Cyclone IV GX transceiver input reference clock. ■ Updated Table 1–29 to include the typical DCLK value. ■ Updated the minimum f_{HSCLK} value in Table 1–31, Table 1–32, Table 1–33, Table 1–34, and Table 1–35.
November 2011	1.5	■ Updated "Maximum Allowed Overshoot or Undershoot Voltage", "Operating Conditions", and "PLL Specifications" sections. ■ Updated Table 1–2, Table 1–3, Table 1–4, Table 1–5, Table 1–8, Table 1–9, Table 1–15, Table 1–18, Table 1–19, and Table 1–21. ■ Updated Figure 1–1.
December 2010	1.4	■ Updated for the Quartus II software version 10.1 release. ■ Updated Table 1–21 and Table 1–25. ■ Minor text edits.
July 2010	1.3	Updated for the Quartus II software version 10.0 release: ■ Updated Table 1–3, Table 1–4, Table 1–21, Table 1–25, Table 1–28, Table 1–30, Table 1–40, Table 1–41, Table 1–42, Table 1–43, Table 1–44, and Table 1–45. ■ Updated Figure 1–2 and Figure 1–3. ■ Removed SW Requirement and TCCS for Cyclone IV Devices tables. ■ Minor text edits.
March 2010	1.2	Updated to include automotive devices: ■ Updated the "Operating Conditions" and "PLL Specifications" sections. ■ Updated Table 1–1, Table 1–8, Table 1–9, Table 1–21, Table 1–26, Table 1–27, Table 1–31, Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–36, Table 1–37, Table 1–38, Table 1–40, Table 1–42, and Table 1–43. ■ Added Table 1–5 to include ESD for Cyclone IV devices GPIOs and HSSI I/Os. ■ Added Table 1–44 and Table 1–45 to include IOE programmable delay for Cyclone IV E 1.2 V core voltage devices. ■ Minor text edits.

Table 1–47. Document Revision History

Date	Version	Changes
February 2010	1.1	■ Updated Table 1–3 through Table 1–44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release. ■ Minor text edits.
November 2009	1.0	Initial release.