

Intel - EP4CGX50CF23C8N Datasheet



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Details	
Product Status	Active
Number of LABs/CLBs	3118
Number of Logic Elements/Cells	49888
Total RAM Bits	2562048
Number of I/O	290
Number of Gates	-
Voltage - Supply	1.16V ~ 1.24V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4cgx50cf23c8n

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Cyclone IV E industrial devices I7 are offered with extended operating temperature range.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone IV devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Table 1–1 lists the absolute maximum ratings for Cyclone IV devices.



Conditions beyond those listed in Table 1–1 cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time have adverse effects on the device.

Symbol	Parameter	Min	Max	Unit
V _{CCINT}	Core voltage, PCI Express [®] (PCIe [®]) hard IP block, and transceiver physical coding sublayer (PCS) power supply	-0.5	1.8	V
V _{CCA}	Phase-locked loop (PLL) analog power supply	-0.5	3.75	V
V _{CCD_PLL}	PLL digital power supply	-0.5	1.8	V
V _{CCIO}	I/O banks power supply	-0.5	3.75	V
V_{CC_CLKIN}	Differential clock input pins power supply	-0.5	4.5	V
V_{CCH_GXB}	Transceiver output buffer power supply	-0.5	3.75	V
V _{CCA_GXB}	Transceiver physical medium attachment (PMA) and auxiliary power supply	-0.5	3.75	V
V _{CCL_GXB}	Transceiver PMA and auxiliary power supply	-0.5	1.8	V
VI	DC input voltage	-0.5	4.2	V
I _{OUT}	DC output current, per pin	-25	40	mA
T _{STG}	Storage temperature	-65	150	0°
TJ	Operating junction temperature	-40	125	O°

Table 1–1. Absolute Maximum Ratings for Cyclone IV Devices (1)

Note to Table 1–1:

(1) Supply voltage specifications apply to voltage readings taken at the device pins with respect to ground, not at the power supply.

Maximum Allowed Overshoot or Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to –2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns. Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device.

A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit			
		V ₁ = 4.20	100	%			
	V _i AC Input	V ₁ = 4.25	98	%			
		V ₁ = 4.30	65	%			
		V ₁ = 4.35	43	%			
Vi		AC Input Voltage	AC Input Voltage	AC Input Voltage	AC Input Voltage	$V_1 = 4.40$	29
	Voltage	V ₁ = 4.45	20	%			
		$V_1 = 4.50$	13	%			
		V ₁ = 4.55	9	%			
		$V_1 = 4.60$	6	%			

Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.





Table 1-3.	Recommended Operating Conditions for Cyclone IV E Devices (1), (2	²⁾ (Part 2 of 2)
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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _{Diode}	Magnitude of DC current across PCI-clamp diode when enable	_	_	_	10	mA

Notes to Table 1-3:

 Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades.

(2) V_{CCI0} for all I/O banks must be powered up during device operation. All VCCA pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.

(3) V_{CC} must rise monotonically.

(4) V_{CCI0} powers all input buffers.

(5) The POR time for Standard POR ranges between 50 and 200 ms. Each individual power supply must reach the recommended operating range within 50 ms.

(6) The POR time for Fast POR ranges between 3 and 9 ms. Each individual power supply must reach the recommended operating range within 3 ms.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{ccint} (3)	Core voltage, PCIe hard IP block, and transceiver PCS power supply	—	1.16	1.2	1.24	V
V _{CCA} (1), (3)	PLL analog power supply	—	2.375	2.5	2.625	V
V _{CCD_PLL} (2)	PLL digital power supply	—	1.16	1.2	1.24	V
	I/O banks power supply for 3.3-V operation	_	3.135	3.3	3.465	V
	I/O banks power supply for 3.0-V operation	_	2.85	3	3.15	V
\/ (3). (4)	I/O banks power supply for 2.5-V operation	_	2.375	2.5	2.625	V
VCCIO	I/O banks power supply for 1.8-V operation	_	1.71	1.8	1.89	V
	I/O banks power supply for 1.5-V operation	_	1.425	1.5	1.575	V
	I/O banks power supply for 1.2-V operation	_	1.14	1.2	1.26	V
	Differential clock input pins power supply for 3.3-V operation	_	3.135	3.3	3.465	V
	Differential clock input pins power supply for 3.0-V operation	_	2.85	3	3.15	V
V _{CC_CLKIN}	Differential clock input pins power supply for 2.5-V operation	_	2.375	2.5	2.625	V
(3), (5), (6)	Differential clock input pins power supply for 1.8-V operation	_	1.71	1.8	1.89	V
	Differential clock input pins power supply for 1.5-V operation	_	1.425	1.5	1.575	V
	Differential clock input pins power supply for 1.2-V operation	—	1.14	1.2	1.26	V
V _{CCH_GXB}	Transceiver output buffer power supply	—	2.375	2.5	2.625	V

Table 1–4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 1 of 2)

DC Characteristics

This section lists the I/O leakage current, pin capacitance, on-chip termination (OCT) tolerance, and bus hold specifications for Cyclone IV devices.

Supply Current

The device supply current requirement is the minimum current drawn from the power supply pins that can be used as a reference for power size planning. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary greatly with the resources used. Table 1–6 lists the I/O pin leakage current for Cyclone IV devices.

Table 1–6. I/O Pin Leakage Current for Cyclone IV Devices (1), (2)

Symbol	Parameter	Conditions	Device	Min	Тур	Max	Unit
I _I	Input pin leakage current	$V_I = 0 V \text{ to } V_{\text{CCIOMAX}}$	—	-10	_	10	μA
I _{OZ}	Tristated I/O pin leakage current	$V_0 = 0 V \text{ to } V_{\text{CCIOMAX}}$		-10		10	μA

Notes to Table 1-6:

(1) This value is specified for normal device operation. The value varies during device power-up. This applies for all V_{CCI0} settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) The 10 μ A I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

Bus Hold

The bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1–7 lists bus hold specifications for Cyclone IV devices.

 Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 1 of 2)⁽¹⁾

		V _{CCI0} (V)												
Parameter	Condition	1	.2	1	.5	1	.8	2	.5	3	.0	3	.3	Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus hold low, sustaining current	V _{IN} > V _{IL} (maximum)	8	_	12	_	30	_	50	_	70	_	70	_	μΑ
Bus hold high, sustaining current	V _{IN} < V _{IL} (minimum)	-8	_	-12	_	-30	_	-50	_	-70	_	-70	_	μΑ
Bus hold low, overdrive current	$0 V < V_{IN} < V_{CCIO}$	_	125	_	175	_	200	_	300	_	500		500	μA
Bus hold high, overdrive current	$0 V < V_{IN} < V_{CCIO}$		-125		-175		-200		-300		-500		-500	μA

Example 1–1 shows how to calculate the change of 50- Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

Example 1–1. Impedance Change

$$\begin{split} \Delta R_V &= (3.15-3) \times 1000 \times -0.026 = -3.83 \\ \Delta R_T &= (85-25) \times 0.262 = 15.72 \\ \text{Because } \Delta R_V \text{ is negative,} \\ MF_V &= 1 \ / \ (3.83/100 + 1) = 0.963 \\ \text{Because } \Delta R_T \text{ is positive,} \\ MF_T &= 15.72/100 + 1 = 1.157 \\ MF &= 0.963 \times 1.157 = 1.114 \\ R_{\text{final}} &= 50 \times 1.114 = 55.71 \ \Omega \end{split}$$

Pin Capacitance

Table 1–11 lists the pin capacitance for Cyclone IV devices.

Table 1–11.	Pin Ca	pacitance 1	for C	vclone IV	Devices	(1)
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Symbol	Parameter	Typical – Quad Flat Pack (QFP)	Typical – Quad Flat No Leads (QFN)	Typical – Ball-Grid Array (BGA)	Unit
C _{IOTB}	Input capacitance on top and bottom I/O pins	7	7	6	pF
C _{IOLR}	Input capacitance on right I/O pins	7	7	5	pF
C _{LVDSLR}	Input capacitance on right I/O pins with dedicated LVDS output	8	8	7	pF
C _{VREFLR} (2)	Input capacitance on right dual-purpose ${\tt VREF}$ pin when used as $V_{\sf REF}$ or user I/O pin	21	21	21	pF
C _{VREFTB}	Input capacitance on top and bottom dual-purpose \mathtt{VREF} pin when used as $V_{\textrm{REF}}$ or user I/O pin	23 <i>(3)</i>	23	23	pF
C _{CLKTB}	Input capacitance on top and bottom dedicated clock input pins	7	7	6	pF
C _{CLKLR}	Input capacitance on right dedicated clock input pins	6	6	5	pF

Notes to Table 1-11:

(1) The pin capacitance applies to FBGA, UBGA, and MBGA packages.

(2) When you use the vref pin as a regular input or output, you can expect a reduced performance of toggle rate and t_{CO} because of higher pin capacitance.

(3) C_{VREFTB} for the EP4CE22 device is 30 pF.

Internal Weak Pull-Up and Weak Pull-Down Resistor

Table 1–12 lists the weak pull-up and pull-down resistor values for Cyclone IV devices.

Table 1–12. Internal Weak Pull-Up and Weak Pull-Down Resistor Values for Cyclone IV Devices ⁽¹⁾

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		$V_{CC10} = 3.3 \text{ V} \pm 5\%$ (2), (3)	7	25	41	kΩ
	Value of the I/O nin pull-up resistor	$V_{CC10} = 3.0 \text{ V} \pm 5\%$ (2), (3)	7	28	47	kΩ
P	before and during configuration, as	$V_{CCIO} = 2.5 \text{ V} \pm 5\%$ (2), (3)	8	35	61	kΩ
n_pu	well as user mode if you enable the programmable pull-up resistor option	$V_{CCIO} = 1.8 \text{ V} \pm 5\%$ (2), (3)	10	57	108	kΩ
		$V_{CCIO} = 1.5 \text{ V} \pm 5\%$ (2), (3)	13	82	163	kΩ
		$V_{CCIO} = 1.2 \text{ V} \pm 5\%$ (2), (3)	19	143	351	kΩ
		$V_{CCIO} = 3.3 \text{ V} \pm 5\%$ (4)	6	19	30	kΩ
		$V_{CCIO} = 3.0 \text{ V} \pm 5\%$ (4)	6	22	36	kΩ
R_pd	before and during configuration	$V_{CCIO} = 2.5 \text{ V} \pm 5\%$ (4)	6	25	43	kΩ
	soloro and daming borngulation	$V_{CCIO} = 1.8 \text{ V} \pm 5\%$ (4)	7	35	71	kΩ
		$V_{CCIO} = 1.5 \text{ V} \pm 5\%$ (4)	8	50	112	kΩ

Notes to Table 1–12:

- (1) All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.
- (2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO} .
- $\begin{array}{ll} \text{(3)} & \text{R}_{_{PU}} = (\text{V}_{\text{CCI0}} \text{V}_{\text{I}})/\text{I}_{\text{R}_{_{PU}}} \\ & \text{Minimum condition: } -40^{\circ}\text{C}; \ \text{V}_{\text{CCI0}} = \text{V}_{\text{CC}} + 5\%, \ \text{V}_{\text{I}} = \text{V}_{\text{CC}} + 5\% 50 \ \text{mV}; \\ & \text{Typical condition: } 25^{\circ}\text{C}; \ \text{V}_{\text{CCI0}} = \text{V}_{\text{CC}}, \ \text{V}_{\text{I}} = 0 \ \text{V}; \\ & \text{Maximum condition: } 100^{\circ}\text{C}; \ \text{V}_{\text{CCI0}} = \text{V}_{\text{CC}} 5\%, \ \text{V}_{\text{I}} = 0 \ \text{V}; \\ & \text{Maximum condition: } 100^{\circ}\text{C}; \ \text{V}_{\text{CCI0}} = \text{V}_{\text{CC}} 5\%, \ \text{V}_{\text{I}} = 0 \ \text{V}; \\ & \text{maximum condition: } 100^{\circ}\text{C}; \ \text{V}_{\text{CO}} = \text{V}_{\text{CC}} 5\%, \ \text{V}_{\text{I}} = 0 \ \text{V}; \\ & \text{Maximum condition: } 100^{\circ}\text{C}; \ \text{V}_{\text{CO}} = \text{V}_{\text{CC}} 5\%, \ \text{V}_{\text{I}} = 0 \ \text{V}; \\ & \text{Maximum condition: } 100^{\circ}\text{C}; \ \text{V}_{\text{CO}} = \text{V}_{\text{CO}} 5\%, \ \text{V}_{\text{I}} = 0 \ \text{V}; \\ & \text{Maximum condition: } 100^{\circ}\text{C}; \ \text{V}_{\text{CO}} = \text{V}_{\text{CO}} 5\%, \ \text{V}_{\text{I}} = 0 \ \text{V}; \\ & \text{Maximum condition: } 100^{\circ}\text{C}; \ \text{V}_{\text{CO}} = \text{V}_{\text{CO}} 5\%, \ \text{V}_{\text{I}} = 0 \ \text{V}; \\ & \text{Maximum condition: } 100^{\circ}\text{C}; \ \text{V}_{\text{CO}} = \text{V}_{\text{CO}} 5\%, \ \text{V}_{\text{I}} = 0 \ \text{V}; \\ & \text{Maximum condition: } 100^{\circ}\text{C}; \ \text{V}_{\text{CO}} = \text{V}_{\text{CO}} 5\%, \ \text{V}_{\text{I}} = 0 \ \text{V}; \\ & \text{Maximum condition: } 100^{\circ}\text{C}; \ \text{V}_{\text{CO}} = 10^{\circ}\text{C}; \ \text{V}_{\text{CO}} = 10^{\circ$
- $\begin{array}{ll} (4) & R_{_PD} = V_I/I_{R_PD} \\ & \text{Minimum condition:} -40^{\circ}\text{C}; \ V_{CCIO} = V_{CC} + 5\%, \ V_I = 50 \ \text{mV}; \\ & \text{Typical condition:} \ 25^{\circ}\text{C}; \ V_{CCIO} = V_{CC}, \ V_I = V_{CC} 5\%; \\ & \text{Maximum condition:} \ 100^{\circ}\text{C}; \ V_{CCIO} = V_{CC} 5\%, \ V_I = V_{CC} 5\%; \ \text{in which } V_I \ \text{refers to the input voltage at the I/O pin.} \end{array}$

Hot-Socketing

Table 1–13 lists the hot-socketing specifications for Cyclone IV devices.

Table 1–13. Hot-Socketing Specifications for Cyclone IV Devices

Symbol	Maximum	
I _{IOPIN(DC)}	DC current per I/O pin	300 μA
I _{IOPIN(AC)}	AC current per I/O pin	8 mA <i>(1)</i>
I _{XCVRTX(DC)}	DC current per transceiver TX pin	100 mA
I _{XCVRRX(DC)}	DC current per transceiver RX pin	50 mA

Note to Table 1-13:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |IIOPIN| = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.

During hot-socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

Transceiver Performance Specifications

Table 1–21 lists the Cyclone IV GX transceiver specifications.

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 1 of 4)

Symbol/	Conditions		C6			C7, I7			C8		11 14
Description	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Reference Clock											
Supported I/O Standards		1.2 V F	PCML, 1.5	V PCML, 3.	3 V PCN	IL, Differe	ntial LVPE	ECL, LVD	S, HCSL		
Input frequency from REFCLK input pins	_	50	_	156.25	50	_	156.25	50	_	156.25	MHz
Spread-spectrum modulating clock frequency	Physical interface for PCI Express (PIPE) mode	30	_	33	30	_	33	30	_	33	kHz
Spread-spectrum downspread	PIPE mode	_	0 to -0.5%	_	_	0 to -0.5%	_	_	0 to -0.5%	_	_
Peak-to-peak differential input voltage	_	0.1	_	1.6	0.1	_	1.6	0.1	_	1.6	V
V _{ICM} (AC coupled)	—		1100 ± 5	5%		1100 ± 59	%		1100 ± 5	%	mV
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250	_	550	250	_	550	mV
Transmitter REFCLK Phase Noise ⁽¹⁾	Frequency offset	_	_	-123	_	_	-123	_	_	-123	dBc/Hz
Transmitter REFCLK Total Jitter ⁽¹⁾	= 1 MHz – 8 MHZ	_	_	42.3	_	_	42.3	_	_	42.3	ps
R _{ref}	_	_	2000 ± 1%	_	_	2000 ± 1%	_	_	2000 ± 1%	_	Ω
Transceiver Clock											
cal_blk_clk clock frequency	_	10	_	125	10	_	125	10	_	125	MHz
fixedclk clock frequency	PCIe Receiver Detect	_	125	_	_	125	_	_	125	_	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 <i>(2)</i>	_	50	2.5/ 37.5 <i>(2)</i>	_	50	2.5/ 37.5 <i>(2)</i>	_	50	MHz
Delta time between reconfig_clk	_	_	_	2	_		2			2	ms
Transceiver block minimum power-down pulse width	_	_	1	_	_	1	_	_	1	_	μs

Figure 1–2 shows the lock time parameters in manual mode.

LTD = lock-to-data. LTR = lock-to-reference.



Figure 1–2. Lock Time Parameters for Manual Mode

Figure 1–3 shows the lock time parameters in automatic mode.

Figure 1–3. Lock Time Parameters for Automatic Mode



Symbol	Parameter	Min	Тур	Max	Unit
t _{DLOCK}	Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or areset is deasserted)	_	_	1	ms
t _{outjitter_period_dedclk} (6)	Dedicated clock output period jitter $F_{OUT} \ge 100 \text{ MHz}$			300	ps
	F _{OUT} < 100 MHz	_	_	30	mUI
toutjitter_ccj_dedclk <i>(6)</i>	Dedicated clock output cycle-to-cycle jitter $F_{\text{OUT}} \geq 100 \text{ MHz}$	_	_	300	ps
	F _{OUT} < 100 MHz	_	—	30	mUI
toutjitter period 10 <i>(6)</i>	Regular I/O period jitter $F_{OUT} \ge 100 \text{ MHz}$	_	_	650	ps
	F _{OUT} < 100 MHz	_	—	75	mUI
toutjitter ccj 10 (6)	Regular I/O cycle-to-cycle jitter $F_{OUT} \ge 100 \text{ MHz}$	_	_	650	ps
	F _{OUT} < 100 MHz	_	—	75	mUI
t _{PLL_PSERR}	Accuracy of PLL phase shift	_	_	±50	ps
t _{ARESET}	Minimum pulse width on areset signal.	10	—	_	ns
t _{configpll}	Time required to reconfigure scan chains for PLLs	_	3.5 (7)	_	SCANCLK cycles
f _{scanclk}	scanclk frequency	_	_	100	MHz
t _{CASC_OUTJITTER_PERIOD_DEDCLK}	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \ge 100 \text{ MHz}$)	_	_	425	ps
(8), (9)	Period jitter for dedicated clock output in cascaded PLLs (F _{OUT} < 100 MHz)			42.5	mUI

Table 1-25.	PLL Specifica	ations for Cyclo	ne IV Devices ⁽¹	I), (2)	(Part 2 of 2)
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Notes to Table 1-25:

- (1) This table is applicable for general purpose PLLs and multipurpose PLLs.
- (2) You must connect $V_{\text{CCD_PLL}}$ to V_{CCINT} through the decoupling capacitor and ferrite bead.
- (3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (4) The V_{C0} frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the V_{C0} post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VC0} specification.
- (5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.
- (6) Peak-to-peak jitter with a probability level of 10⁻¹² (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.
- (7) With 100-MHz scanclk frequency.
- (8) The cascaded PLLs specification is applicable only with the following conditions:
 - $\blacksquare \quad Upstream \ PLL {----}0.59 \ MHz \leq Upstream \ PLL \ bandwidth < 1 \ MHz$
 - Downstream PLL—Downstream PLL bandwidth > 2 MHz
- (9) PLL cascading is not supported for transceiver applications.

Table 1–29 lists the active configuration mode specifications for Cyclone IV devices.

Programming Mode	DCLK Range	Typical DCLK	Unit
Active Parallel (AP) (1)	20 to 40	33	MHz
Active Serial (AS)	20 to 40	33	MHz

Table 1–29. Active Configuration Mode Specifications for Cyclone IV Devices

Note to Table 1-29:

(1) AP configuration mode is only supported for Cyclone IV E devices.

Table 1-30 lists the JTAG timing parameters and values for Cyclone IV devices.

Table 1–30. JTAG Timing Parameters for Cyclone IV Devices (1)

Symbol	Parameter	Min	Max	Unit
t _{JCP}	TCK clock period	40	—	ns
t _{JCH}	TCK clock high time	19	—	ns
t _{JCL}	TCK clock low time	19	—	ns
t _{JPSU_TDI}	JTAG port setup time for TDI	1	—	ns
t _{JPSU_TMS}	JTAG port setup time for TMS	3	—	ns
t _{JPH}	JTAG port hold time	10	—	ns
t _{JPC0}	JTAG port clock to output ^{(2), (3)}	_	15	ns
t _{JPZX}	JTAG port high impedance to valid output ^{(2), (3)}	_	15	ns
t _{JPXZ}	JTAG port valid output to high impedance ^{(2), (3)}	_	15	ns
t _{JSSU}	Capture register setup time	5	_	ns
t _{JSH}	Capture register hold time	10	—	ns
t _{JSC0}	Update register clock to output	_	25	ns
t _{JSZX}	Update register high impedance to valid output		25	ns
t _{JSXZ}	Update register valid output to high impedance		25	ns

Notes to Table 1-30:

(1) For more information about JTAG waveforms, refer to "JTAG Waveform" in "Glossary" on page 1–37.

- (2) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 16 ns.
- (3) For EP4CGX22, EP4CGX30 (F324 and smaller package), EP4CGX110, and EP4CGX150 devices, the output time specification for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins is 16 ns. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 18 ns.

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/Os using the SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speeds. I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-LVTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.

- ***** For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interfaces Handbook*.
- Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 1–31 through Table 1–36 list the high-speed I/O timing for Cyclone IV devices. For definitions of high-speed timing specifications, refer to "Glossary" on page 1–37.

Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4) (Part 1 of 2)

0 milest			C6			C7, I	7		C8, A	7		C8L, I	8L		C9L		
Symbol	wodes	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
	×10	5		180	5		155.5	5	—	155.5	5		155.5	5		132.5	MHz
	×8	5		180	5	—	155.5	5	—	155.5	5		155.5	5	_	132.5	MHz
f _{HSCLK}	×7	5		180	5		155.5	5		155.5	5		155.5	5	—	132.5	MHz
(input clock frequency)	×4	5	_	180	5	—	155.5	5	—	155.5	5	_	155.5	5	_	132.5	MHz
, ,,	×2	5		180	5		155.5	5	_	155.5	5		155.5	5	_	132.5	MHz
	×1	5	_	360	5	—	311	5	—	311	5	_	311	5	_	265	MHz
	×10	100	_	360	100	_	311	100	—	311	100	_	311	100	_	265	Mbps
	×8	80		360	80		311	80	—	311	80		311	80		265	Mbps
Device	×7	70		360	70		311	70		311	70		311	70		265	Mbps
Mbps	×4	40		360	40		311	40		311	40		311	40	_	265	Mbps
	×2	20		360	20		311	20	—	311	20		311	20		265	Mbps
	×1	10		360	10		311	10		311	10		311	10	_	265	Mbps
t _{DUTY}	—	45	_	55	45	_	55	45	—	55	45	_	55	45	_	55	%
Transmitter channel-to- channel skew (TCCS)	_		_	200	_	_	200	_	_	200	_	_	200		_	200	ps
Output jitter (peak to peak)	_	_	_	500	_	_	500	_	_	550	_	_	600	_	_	700	ps
t _{RISE}	20 – 80%, C _{LOAD} = 5 pF	_	500	_	_	500	_	_	500	_	_	500	_	_	500	_	ps
t _{FALL}	20 - 80%, C _{LOAD} = 5 pF	_	500		_	500	_	_	500	_	_	500	_	_	500	_	ps

Symbol	Modes		C6			C7, I	7		C8, A	7		C8L, I	8L		C9L		Ilnit
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
t _{LOCK} (3)	_			1			1	_		1			1	_		1	ms

Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (2), (4)} (Part 2 of 2)

Notes to Table 1-31:

(1) Applicable for true RSDS and emulated RSDS_E_3R transmitter.

(2) Cyclone IV E devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated RSDS transmitter is supported at the output pin of all I/O Banks. Cyclone IV GX devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is only supported at the

pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
(3) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Symbol	Madaa		C6			C7, 17	1		C8, A	7		C8L, I8	BL		C9L		11
Symbol	wodes	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
	×10	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×8	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
f _{HSCLK} (input	×7	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
frequency)	×4	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×2	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×1	5	—	170	5	—	170	5	—	170	5	—	170	5	—	145	MHz
	×10	100	—	170	100	—	170	100	—	170	100	—	170	100	—	145	Mbps
	×8	80	—	170	80	—	170	80	—	170	80	—	170	80	—	145	Mbps
Device	×7	70	—	170	70	—	170	70	—	170	70	—	170	70	—	145	Mbps
Mbps	×4	40	—	170	40	—	170	40	—	170	40	—	170	40	—	145	Mbps
	×2	20	—	170	20	—	170	20	—	170	20	—	170	20	—	145	Mbps
	×1	10	—	170	10	—	170	10	—	170	10	—	170	10	—	145	Mbps
t _{DUTY}	_	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS	_	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	_	_	_	500	_	_	500	_	_	550	_	_	600	_	_	700	ps
t _{RISE}	20 - 80%, C _{LOAD} = 5 pF	_	500	_	_	500	_	_	500	_	_	500	_	_	500	_	ps
t _{FALL}	20 - 80%, C _{LOAD} = 5 pF	_	500	_	_	500	_	_	500	_	_	500	_	_	500	_	ps

Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 1 of 2)

Symbol	Madaa	C	6	C7	, 17	C8,	, A7	C8L	, 18L	C	9L	Unit
Symbol	modes	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
	×10	5	420	5	370	5	320	5	320	5	250	MHz
	×8	5	420	5	370	5	320	5	320	5	250	MHz
f _{HSCLK} (input	×7	5	420	5	370	5	320	5	320	5	250	MHz
frequency)	×4	5	420	5	370	5	320	5	320	5	250	MHz
1 37	×2	5	420	5	370	5	320	5	320	5	250	MHz
	×1	5	420	5	402.5	5	402.5	5	362	5	265	MHz
	×10	100	840	100	740	100	640	100	640	100	500	Mbps
	×8	80	840	80	740	80	640	80	640	80	500	Mbps
	×7	70	840	70	740	70	640	70	640	70	500	Mbps
ISIUDA	×4	40	840	40	740	40	640	40	640	40	500	Mbps
	×2	20	840	20	740	20	640	20	640	20	500	Mbps
	×1	10	420	10	402.5	10	402.5	10	362	10	265	Mbps
t _{DUTY}	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	—	_	200		200		200		200	_	200	ps
Output jitter (peak to peak)	_	_	500	_	500	_	550	_	600	_	700	ps
t _{LOCK} (2)	—		1	—	1	_	1	_	1	—	1	ms

Table 1–34. True LVDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)}

Notes to Table 1-34:

(1) Cyclone IV E—true LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Cyclone IV GX—true LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 1 of 2)

Symbol	Medee	C	6	C7,	, 17	C8,	A7	C8L,	, 18L	C	9L	Unit
Symbol	modes	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
	×10	5	320	5	320	5	275	5	275	5	250	MHz
	×8	5	320	5	320	5	275	5	275	5	250	MHz
f _{HSCLK} (input	×7	5	320	5	320	5	275	5	275	5	250	MHz
frequency)	×4	5	320	5	320	5	275	5	275	5	250	MHz
noquonoy)	×2	5	320	5	320	5	275	5	275	5	250	MHz
	×1	5	402.5	5	402.5	5	402.5	5	362	5	265	MHz
	×10	100	640	100	640	100	550	100	550	100	500	Mbps
	×8	80	640	80	640	80	550	80	550	80	500	Mbps
	×7	70	640	70	640	70	550	70	550	70	500	Mbps
HOIDDA	×4	40	640	40	640	40	550	40	550	40	500	Mbps
	×2	20	640	20	640	20	550	20	550	20	500	Mbps
	×1	10	402.5	10	402.5	10	402.5	10	362	10	265	Mbps

• For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interface Handbook*.

Table 1–37 lists the memory output clock jitter specifications for Cyclone IV devices.

Table 1–37. Memory Output Clock Jitter Specifications for Cyclone IV Devices (1), (2)

Parameter	Symbol	Min	Max	Unit
Clock period jitter	t _{JIT(per)}	-125	125	ps
Cycle-to-cycle period jitter	t _{JIT(cc)}	-200	200	ps
Duty cycle jitter	t _{JIT(duty)}	-150	150	ps

Notes to Table 1-37:

(1) Memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2 standard.

(2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock (GCLK) network.

Duty Cycle Distortion Specifications

Table 1–38 lists the worst case duty cycle distortion for Cyclone IV devices.

Table 1–38. Duty Cycle Distortion on Cyclone IV Devices I/O Pins (1), (2), (3)

Symbol	C	6	C 7	, 17	C8, I8	BL, A7	C	Unit	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Notes to Table 1-38:

(1) The duty cycle distortion specification applies to clock outputs from the PLLs, global clock tree, and IOE driving the dedicated and general purpose I/O pins.

(2) Cyclone IV devices meet the specified duty cycle distortion at the maximum output toggle rate for each combination of I/O standard and current strength.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

OCT Calibration Timing Specification

Table 1–39 lists the duration of calibration for series OCT with calibration at device power-up for Cyclone IV devices.

Table 1–39. Timing Specification for Series OCT with Calibration at Device Power-Up for Cyclone IV Devices $^{(1)}$

Symbol	Description	Maximum	Units
t _{octcal}	Duration of series OCT with calibration at device power-up	20	μs

Note to Table 1-39:

(1) OCT calibration takes place after device configuration and before entering user mode.

IOE Programmable Delay

Table 1–40 and Table 1–41 list the IOE programmable delay for Cyclone IV E 1.0 V core voltage devices.

Table 1–40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Device
--

Parameter		Number of Setting	umber Min of Offset etting	Max Offset					
	Paths Affected			Fast (orner	S	Unit		
				C8L	18L	C8L	C9L	18L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.054	1.924	3.387	4.017	3.411	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.010	1.875	3.341	4.252	3.367	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.641	0.631	1.111	1.377	1.124	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.971	0.931	1.684	2.298	1.684	ns

Notes to Table 1-40:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

		Numbor	Min Offset	Max Offset					
Parameter	Paths Affected	of Setting		Fast (Corner	S	Unit		
				C8L	18L	C8L	C9L	18L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.057	1.921	3.389	4.146	3.412	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.059	1.919	3.420	4.374	3.441	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.670	0.623	1.160	1.420	1.168	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.960	0.919	1.656	2.258	1.656	ns

Notes to Table 1-41:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

Parameter		Numbor	hor		Max Offset							
	Paths Affected	of Setting	Min Offset	Min Affset Fast Corner			Slow Corner					Unit
				C6	17	A7	C6	C7	C8	17	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.211	1.211	2.177	2.340	2.433	2.388	2.508	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.307	1.203	1.203	2.19	2.387	2.540	2.430	2.545	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.437	0.402	0.402	0.747	0.820	0.880	0.834	0.873	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.693	0.665	0.665	1.200	1.379	1.532	1.393	1.441	ns

Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices	(1),	(2)
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Notes to Table 1-42:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Parameter		Numbor		Max Offset								
	Paths Affected	of Setting	Min Offset	Min Offset Fast Corner			Slow Corner					Unit
				C6	17	A7	C6	C7	C8	17	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.209	1.209	2.201	2.386	2.510	2.429	2.548	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.207	1.207	2.202	2.402	2.558	2.447	2.557	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.458	0.419	0.419	0.783	0.861	0.924	0.875	0.915	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.686	0.657	0.657	1.185	1.360	1.506	1.376	1.422	ns

Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices (1), (2)

Notes to Table 1-43:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

Table 1-44.	IOE Programmable	Delay on Column	Pins for Cyclone	IV GX Devices ^{(1), (2)}
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		Numbor	Min Offset	Max Offset						
Parameter	Paths Affected	of Settings		Fast Corner		Slow Corner				Unit
				C6	17	C6	C7	C8	17	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.313	1.209	2.184	2.336	2.451	2.387	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.208	2.200	2.399	2.554	2.446	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.438	0.404	0.751	0.825	0.886	0.839	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.713	0.682	1.228	1.41	1.566	1.424	ns

Notes to Table 1-44:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

		Numbor	Min Offset	Max Offset						
Parameter	Paths Affected	of		Min Offset Fast Corner		Slow Corner				Unit
		Settings		C6	17	C6	C7	C8	17	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.210	2.209	2.398	2.526	2.443	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.313	1.208	2.205	2.406	2.563	2.450	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.461	0.421	0.789	0.869	0.933	0.884	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.712	0.682	1.225	1.407	1.562	1.421	ns

Table 1–45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices (1), (2)

Notes to Table 1-45:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software

Document Revision History

Table 1–47 lists the revision history for this chapter.

Date	Version	Changes
March 2016	2.0	Updated note (5) in Table 1–21 to remove support for the N148 package.
October 2014	1.9	Updated maximum value for V _{CCD_PLL} in Table 1–1.
		Removed extended temperature note in Table 1–3.
December 2013	1.8	Updated Table 1–21 by adding Note (15).
May 2013	1.7	Updated Table 1–15 by adding Note (4).
October 2012	1.6	■ Updated the maximum value for V _I , V _{CCD_PLL} , V _{CCIO} , V _{CC_CLKIN} , V _{CCH_GXB} , and V _{CCA_GXB} Table 1–1.
		■ Updated Table 1–11 and Table 1–22.
		 Updated Table 1–21 to include peak-to-peak differential input voltage for the Cyclone IV GX transceiver input reference clock.
		■ Updated Table 1–29 to include the typical DCLK value.
		■ Updated the minimum f _{HSCLK} value in Table 1–31, Table 1–32, Table 1–33, Table 1–34, and Table 1–35.
November 2011	1.5	 Updated "Maximum Allowed Overshoot or Undershoot Voltage", "Operating Conditions", and "PLL Specifications" sections.
		■ Updated Table 1–2, Table 1–3, Table 1–4, Table 1–5, Table 1–8, Table 1–9, Table 1–15, Table 1–18, Table 1–19, and Table 1–21.
		■ Updated Figure 1–1.
December 2010	1.4	 Updated for the Quartus II software version 10.1 release.
		■ Updated Table 1–21 and Table 1–25.
		Minor text edits.
	1.3	Updated for the Quartus II software version 10.0 release:
		■ Updated Table 1–3, Table 1–4, Table 1–21, Table 1–25, Table 1–28, Table 1–30, Table 1–40, Table 1–41, Table 1–42, Table 1–43, Table 1–44, and Table 1–45.
July 2010		■ Updated Figure 1–2 and Figure 1–3.
		Removed SW Requirement and TCCS for Cyclone IV Devices tables.
		 Minor text edits.
	1.2	Updated to include automotive devices:
		 Updated the "Operating Conditions" and "PLL Specifications" sections.
March 2010		■ Updated Table 1–1, Table 1–8, Table 1–9, Table 1–21, Table 1–26, Table 1–27, Table 1–31, Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–36, Table 1–37, Table 1–38, Table 1–40, Table 1–42, and Table 1–43.
		Added Table 1–5 to include ESD for Cyclone IV devices GPIOs and HSSI I/Os.
		 Added Table 1–44 and Table 1–45 to include IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.
		 Minor text edits.

Table 1–47. Document Revision History

Date	Version	Changes
February 2010	1.1	 Updated Table 1–3 through Table 1–44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release. Minor text edits.
November 2009	1.0	Initial release.