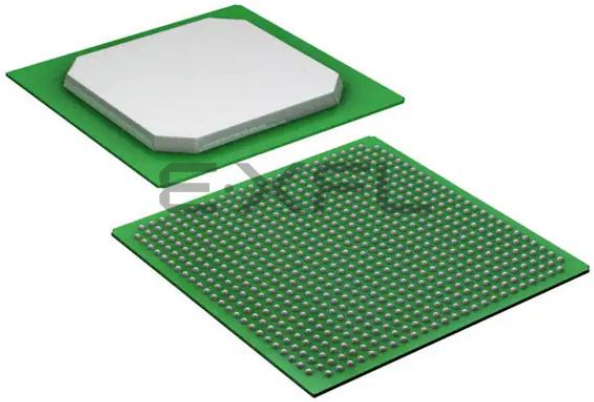

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Details	
Product Status	Active
Number of LABs/CLBs	3118
Number of Logic Elements/Cells	49888
Total RAM Bits	2562048
Number of I/O	310
Number of Gates	-
Voltage - Supply	1.16V ~ 1.24V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4cgx50df27i7n

Cyclone IV E industrial devices I7 are offered with extended operating temperature range.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone IV devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Table 1–1 lists the absolute maximum ratings for Cyclone IV devices.

CAUTION

Conditions beyond those listed in Table 1–1 cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time have adverse effects on the device.

Table 1–1. Absolute Maximum Ratings for Cyclone IV Devices *(1)*

Symbol	Parameter	Min	Max	Unit
V_{CCINT}	Core voltage, PCI Express® (PCIe®) hard IP block, and transceiver physical coding sublayer (PCS) power supply	–0.5	1.8	V
V_{CCA}	Phase-locked loop (PLL) analog power supply	–0.5	3.75	V
V_{CCD_PLL}	PLL digital power supply	–0.5	1.8	V
V_{CCIO}	I/O banks power supply	–0.5	3.75	V
V_{CC_CLKIN}	Differential clock input pins power supply	–0.5	4.5	V
V_{CCH_GXB}	Transceiver output buffer power supply	–0.5	3.75	V
V_{CCA_GXB}	Transceiver physical medium attachment (PMA) and auxiliary power supply	–0.5	3.75	V
V_{CCL_GXB}	Transceiver PMA and auxiliary power supply	–0.5	1.8	V
V_I	DC input voltage	–0.5	4.2	V
I_{OUT}	DC output current, per pin	–25	40	mA
T_{STG}	Storage temperature	–65	150	°C
T_J	Operating junction temperature	–40	125	°C

Note to Table 1–1:

(1) Supply voltage specifications apply to voltage readings taken at the device pins with respect to ground, not at the power supply.

Maximum Allowed Overshoot or Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to –2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns. Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device.

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone IV devices. Table 1–3 and Table 1–4 list the steady-state voltage and current values expected from Cyclone IV E and Cyclone IV GX devices. All supplies must be strictly monotonic without plateaus.

Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices (1), (2) (Part 1 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCINT} (3)	Supply voltage for internal logic, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply voltage for internal logic, 1.0-V operation	—	0.97	1.0	1.03	V
V_{CCIO} (3), (4)	Supply voltage for output buffers, 3.3-V operation	—	3.135	3.3	3.465	V
	Supply voltage for output buffers, 3.0-V operation	—	2.85	3	3.15	V
	Supply voltage for output buffers, 2.5-V operation	—	2.375	2.5	2.625	V
	Supply voltage for output buffers, 1.8-V operation	—	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	—	1.425	1.5	1.575	V
	Supply voltage for output buffers, 1.2-V operation	—	1.14	1.2	1.26	V
V_{CCA} (3)	Supply (analog) voltage for PLL regulator	—	2.375	2.5	2.625	V
V_{CCD_PLL} (3)	Supply (digital) voltage for PLL, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply (digital) voltage for PLL, 1.0-V operation	—	0.97	1.0	1.03	V
V_I	Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
		For extended temperature	–40	—	125	°C
		For automotive use	–40	—	125	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR) (5)	50 µs	—	50 ms	—
		Fast POR (6)	50 µs	—	3 ms	—

Table 1–4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA_GXB}	Transceiver PMA and auxiliary power supply	—	2.375	2.5	2.625	V
V_{CCL_GXB}	Transceiver PMA and auxiliary power supply	—	1.16	1.2	1.24	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	DC output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR) *(7)*	50 µs	—	50 ms	—
		Fast POR *(8)*	50 µs	—	3 ms	—
I_{Diode}	Magnitude of DC current across PCI-clamp diode when enabled	—	—	—	10	mA

Notes to Table 1–4:

(1) All VCCA pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.

(2) You must connect V_{CCD_PLL} to V_{CCINT} through a decoupling capacitor and ferrite bead.

(3) Power supplies must rise monotonically.

(4) V_{CCIO} for all I/O banks must be powered up during device operation. Configurations pins are powered up by V_{CCIO} of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support V_{CCIO} of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the V_{CCIO} level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.

(5) You must set V_{CC_CLKIN} to 2.5 V if you use CLKIN as a high-speed serial interface (HSSI) refclk or as a DIFFCLK input.

(6) The CLKIN pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.

(7) The POR time for Standard POR ranges between 50 and 200 ms. V_{CCINT}, V_{CCA}, and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.

(8) The POR time for Fast POR ranges between 3 and 9 ms. V_{CCINT}, V_{CCA}, and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1–5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

Table 1–5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os

Symbol	Parameter	Passing Voltage	Unit
V_{ESDHBM}	ESD voltage using the HBM (GPIOs) *(1)*	± 2000	V
	ESD using the HBM (HSSI I/Os) *(2)*	± 1000	V
V_{ESDCDM}	ESD using the CDM (GPIOs)	± 500	V
	ESD using the CDM (HSSI I/Os) *(2)*	± 250	V

Notes to Table 1–5:

(1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is ±1000V.

(2) This value is applicable only to Cyclone IV GX devices.

Example 1–1 shows how to calculate the change of 50-Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

Example 1–1. Impedance Change

$\Delta R_V = (3.15 – 3) \times 1000 \times –0.026 = –3.83$

$\Delta R_T = (85 – 25) \times 0.262 = 15.72$

Because ΔR_V is negative,

$MF_V = 1 / (3.83/100 + 1) = 0.963$

Because ΔR_T is positive,

$MF_T = 15.72/100 + 1 = 1.157$

$MF = 0.963 \times 1.157 = 1.114$

$R_{final} = 50 \times 1.114 = 55.71\ \Omega$

Pin Capacitance

Table 1–11 lists the pin capacitance for Cyclone IV devices.

Table 1–11. Pin Capacitance for Cyclone IV Devices *(1)*

Symbol	Parameter	Typical – Quad Flat Pack (QFP)	Typical – Quad Flat No Leads (QFN)	Typical – Ball-Grid Array (BGA)	Unit
C_{IOTB}	Input capacitance on top and bottom I/O pins	7	7	6	pF
C_{IOLR}	Input capacitance on right I/O pins	7	7	5	pF
C_{LVDSLR}	Input capacitance on right I/O pins with dedicated LVDS output	8	8	7	pF
C_{VREFLR} *(2)*	Input capacitance on right dual-purpose VREF pin when used as V_{REF} or user I/O pin	21	21	21	pF
C_{VREFTB} *(2)*	Input capacitance on top and bottom dual-purpose VREF pin when used as V_{REF} or user I/O pin	23 *(3)*	23	23	pF
C_{CLKTB}	Input capacitance on top and bottom dedicated clock input pins	7	7	6	pF
C_{CLKLR}	Input capacitance on right dedicated clock input pins	6	6	5	pF

Notes to Table 1–11:

(1) The pin capacitance applies to FBGA, UBGA, and MBGA packages.

(2) When you use the VREF pin as a regular input or output, you can expect a reduced performance of toggle rate and t_{CO} because of higher pin capacitance.

(3) C_{VREFTB} for the EP4CE22 device is 30 pF.

Internal Weak Pull-Up and Weak Pull-Down Resistor

Table 1–12 lists the weak pull-up and pull-down resistor values for Cyclone IV devices.

Table 1–12. Internal Weak Pull-Up and Weak Pull-Down Resistor Values for Cyclone IV Devices *(1)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{\_PU}$	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option	V_{CCIO} = 3.3 V ± 5% *(2), (3)*	7	25	41	kΩ
		V_{CCIO} = 3.0 V ± 5% *(2), (3)*	7	28	47	kΩ
		V_{CCIO} = 2.5 V ± 5% *(2), (3)*	8	35	61	kΩ
		V_{CCIO} = 1.8 V ± 5% *(2), (3)*	10	57	108	kΩ
		V_{CCIO} = 1.5 V ± 5% *(2), (3)*	13	82	163	kΩ
		V_{CCIO} = 1.2 V ± 5% *(2), (3)*	19	143	351	kΩ
$R_{\_PD}$	Value of the I/O pin pull-down resistor before and during configuration	V_{CCIO} = 3.3 V ± 5% *(4)*	6	19	30	kΩ
		V_{CCIO} = 3.0 V ± 5% *(4)*	6	22	36	kΩ
		V_{CCIO} = 2.5 V ± 5% *(4)*	6	25	43	kΩ
		V_{CCIO} = 1.8 V ± 5% *(4)*	7	35	71	kΩ
		V_{CCIO} = 1.5 V ± 5% *(4)*	8	50	112	kΩ

Notes to Table 1–12:

(1) All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(3) $R_{\_PU} = (V_{CCIO} – V_I)/I_{R\_PU}$
Minimum condition: –40°C; $V_{CCIO} = V_{CC}$ + 5%, $V_I = V_{CC}$ + 5% – 50 mV;
Typical condition: 25°C; $V_{CCIO} = V_{CC}$, V_I = 0 V;
Maximum condition: 100°C; $V_{CCIO} = V_{CC}$ – 5%, V_I = 0 V; in which V_I refers to the input voltage at the I/O pin.

(4) $R_{\_PD} = V_I/I_{R\_PD}$
Minimum condition: –40°C; $V_{CCIO} = V_{CC}$ + 5%, V_I = 50 mV;
Typical condition: 25°C; $V_{CCIO} = V_{CC}$, $V_I = V_{CC}$ – 5%;
Maximum condition: 100°C; $V_{CCIO} = V_{CC}$ – 5%, $V_I = V_{CC}$ – 5%; in which V_I refers to the input voltage at the I/O pin.

Hot-Socketing

Table 1–13 lists the hot-socketing specifications for Cyclone IV devices.

Table 1–13. Hot-Socketing Specifications for Cyclone IV Devices

Symbol	Parameter	Maximum
$I_{IOPIN(DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA *(1)*
$I_{XCVRTX(DC)}$	DC current per transceiver TX pin	100 mA
$I_{XCVRRX(DC)}$	DC current per transceiver RX pin	50 mA

Note to Table 1–13:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |IIOPIN| = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.

☞ During hot-socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

Table 1–16. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Cyclone IV Devices *(1)*

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V) *(2)*		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 x V_{CCIO} *(3)*	0.5 x V_{CCIO} *(3)*	0.52 x V_{CCIO} *(3)*	—	0.5 x V_{CCIO}	—
				0.47 x V_{CCIO} *(4)*	0.5 x V_{CCIO} *(4)*	0.53 x V_{CCIO} *(4)*			

Notes to Table 1–16:

(1) For an explanation of terms used in Table 1–16, refer to "Glossary" on page 1–37.
(2) V_{TT} of the transmitting device must track V_{REF} of the receiving device.
(3) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.
(4) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

Table 1–17. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone IV Devices

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.57	V_{TT} + 0.57	8.1	–8.1
SSTL-2 Class II	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.76	V_{TT} + 0.76	16.4	–16.4
SSTL-18 Class I	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	V_{TT} – 0.475	V_{TT} + 0.475	6.7	–6.7
SSTL-18 Class II	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	0.28	V_{CCIO} – 0.28	13.4	–13.4
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	14	–14

For more information about receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *I/O Features in Cyclone IV Devices* chapter.

Table 1–18. Differential SSTL I/O Standard Specifications for Cyclone IV Devices *(1)*

I/O Standard	V_{CCIO} (V)			$V_{Swing(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{Swing(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.7	V_{CCIO}	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$
SSTL-18 Class I, II	1.7	1.8	1.90	0.25	V_{CCIO}	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	V_{CCIO}	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$

Note to Table 1–18:

(1) Differential SSTL requires a V_{REF} input.

Table 1–19. Differential HSTL I/O Standard Specifications for Cyclone IV Devices *(1)*

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	$0.48 \times V_{CCIO}$	—	$0.52 \times V_{CCIO}$	$0.48 \times V_{CCIO}$	—	$0.52 \times V_{CCIO}$	0.3	$0.48 \times V_{CCIO}$

Note to Table 1–19:

(1) Differential HSTL requires a V_{REF} input.

Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices *(1)* **(Part 1 of 2)**

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) *(2)*			V_{OD} (mV) *(3)*			V_{OS} (V) *(3)*		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (Row I/Os) *(6)*	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq 500$ Mbps	1.80	—	—	—	—	—	—
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	$D_{MAX} >$ 700 Mbps	1.55						
LVPECL (Column I/Os) *(6)*	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.80	—	—	—	—	—	—
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	$D_{MAX} >$ 700 Mbps	1.55						
LVDS (Row I/Os)	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.80	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	$D_{MAX} >$ 700 Mbps	1.55						

Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices (1) (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (2)			V_{OD} (mV) (3)			V_{OS} (V) (3)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS (Column I/Os)	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.80	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	D_{MAX} > 700 Mbps	1.55						
BLVDS (Row I/Os) (4)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
BLVDS (Column I/Os) (4)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
mini-LVDS (Row I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1.0	1.2	1.4
mini-LVDS (Column I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1.0	1.2	1.4
RSDS® (Row I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
RSDS (Column I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
PPDS (Row I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4
PPDS (Column I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4

Notes to Table 1–20:

(1) For an explanation of terms used in Table 1–20, refer to "Glossary" on page 1–37.

(2) V_{IN} range: 0 V $\leq V_{IN} \leq$ 1.85 V.

(3) R_L range: 90 $\leq R_L \leq$ 110 Ω.

(4) There are no fixed V_{IN}, V_{OD}, and V_{OS} specifications for BLVDS. They depend on the system topology.

(5) The Mini-LVDS, RSDS, and PPDS standards are only supported at the output pins.

(6) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported for output pins.

Transceiver Performance Specifications

Table 1–21 lists the Cyclone IV GX transceiver specifications.

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 1 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	1.2 V PCML, 1.5 V PCML, 3.3 V PCML, Differential LVPECL, LVDS, HCSL										
Input frequency from REFCLK input pins	—	50	—	156.25	50	—	156.25	50	—	156.25	MHz
Spread-spectrum modulating clock frequency	Physical interface for PCI Express (PIPE) mode	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PIPE mode	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
Peak-to-peak differential input voltage	—	0.1	—	1.6	0.1	—	1.6	0.1	—	1.6	V
V_{ICM} (AC coupled)	—	1100 ± 5%			1100 ± 5%			1100 ± 5%			mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise *(1)*	Frequency offset = 1 MHz – 8 MHZ	—	—	–123	—	—	–123	—	—	–123	dBc/Hz
Transmitter REFCLK Total Jitter *(1)*		—	—	42.3	—	—	42.3	—	—	42.3	ps
R_{ref}	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clock											
cal_blk_clk clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 *(2)*	—	50	2.5/ 37.5 *(2)*	—	50	2.5/ 37.5 *(2)*	—	50	MHz
Delta time between reconfig_clk	—	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum power-down pulse width	—	—	1	—	—	1	—	—	1	—	µs

Figure 1–2 shows the lock time parameters in manual mode.

LTD = lock-to-data. LTR = lock-to-reference.

Figure 1–2. Lock Time Parameters for Manual Mode

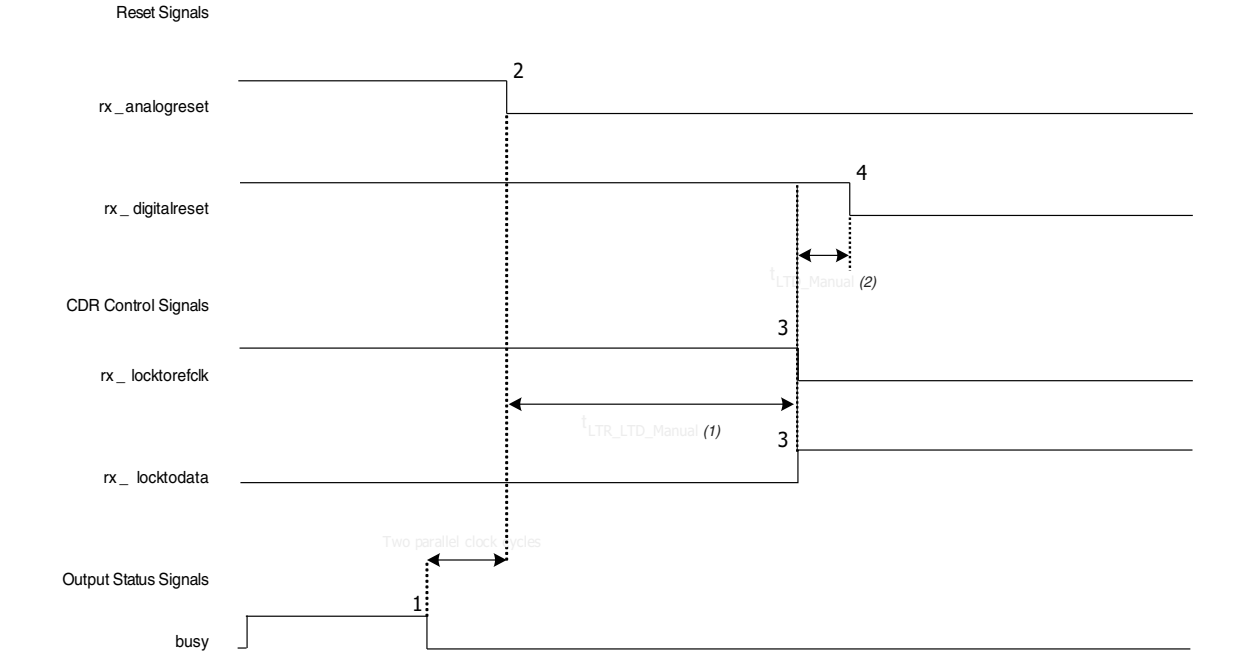
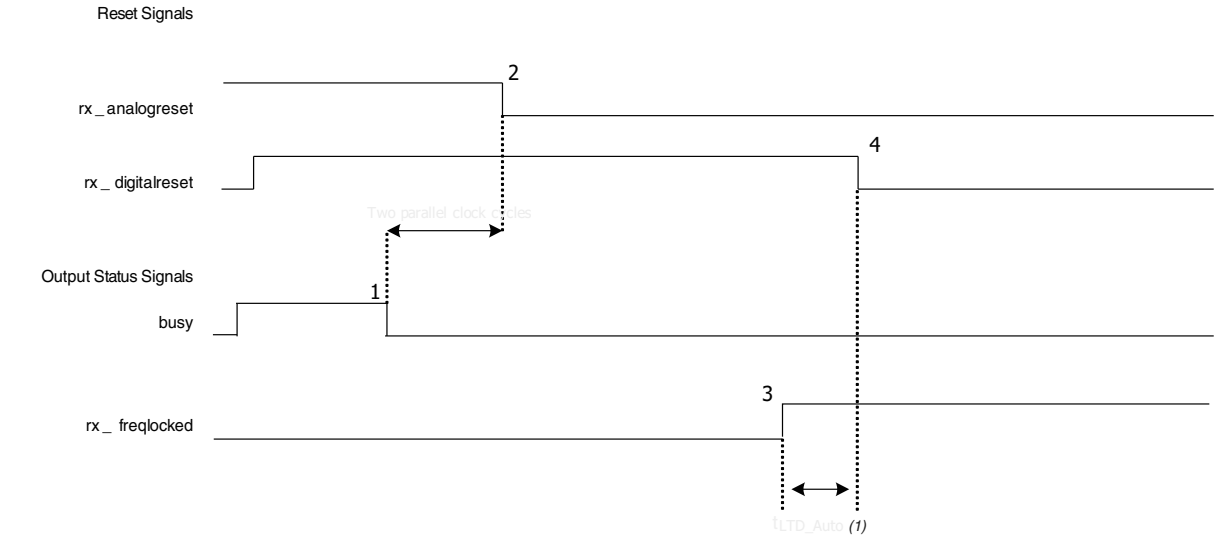


Figure 1–3 shows the lock time parameters in automatic mode.

Figure 1–3. Lock Time Parameters for Automatic Mode



Embedded Multiplier Specifications

Table 1–26 lists the embedded multiplier specifications for Cyclone IV devices.

Table 1–26. Embedded Multiplier Specifications for Cyclone IV Devices

Mode	Resources Used	Performance					Unit
	Number of Multipliers	C6	C7, I7, A7	C8	C8L, I8L	C9L	
9 × 9-bit multiplier	1	340	300	260	240	175	MHz
18 × 18-bit multiplier	1	287	250	200	185	135	MHz

Memory Block Specifications

Table 1–27 lists the M9K memory block specifications for Cyclone IV devices.

Table 1–27. Memory Block Performance Specifications for Cyclone IV Devices

Memory	Mode	Resources Used		Performance					Unit
		LEs	M9K Memory	C6	C7, I7, A7	C8	C8L, I8L	C9L	
M9K Block	FIFO 256 × 36	47	1	315	274	238	200	157	MHz
	Single-port 256 × 36	0	1	315	274	238	200	157	MHz
	Simple dual-port 256 × 36 CLK	0	1	315	274	238	200	157	MHz
	True dual port 512 × 18 single CLK	0	1	315	274	238	200	157	MHz

Configuration and JTAG Specifications

Table 1–28 lists the configuration mode specifications for Cyclone IV devices.

Table 1–28. Passive Configuration Mode Specifications for Cyclone IV Devices (1)

Programming Mode	V_{CCINT} Voltage Level (V)	DCLK f_{MAX}	Unit
Passive Serial (PS)	1.0 (3)	66	MHz
	1.2	133	MHz
Fast Passive Parallel (FPP) (2)	1.0 (3)	66	MHz
	1.2 (4)	100	MHz

Notes to Table 1–28:

(1) For more information about PS and FPP configuration timing parameters, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter.

(2) FPP configuration mode supports all Cyclone IV E devices (except for E144 package devices) and EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 only.

(3) V_{CCINT} = 1.0 V is only supported for Cyclone IV E 1.0 V core voltage devices.

(4) Cyclone IV E devices support 1.2 V V_{CCINT}. Cyclone IV E 1.2 V core voltage devices support 133 MHz DCLK f_{MAX} for EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, and EP4CE40 only.

Table 1–29 lists the active configuration mode specifications for Cyclone IV devices.

Table 1–29. Active Configuration Mode Specifications for Cyclone IV Devices

Programming Mode	DCLK Range	Typical DCLK	Unit
Active Parallel (AP) *(1)*	20 to 40	33	MHz
Active Serial (AS)	20 to 40	33	MHz

Note to Table 1–29:

(1) AP configuration mode is only supported for Cyclone IV E devices.

Table 1–30 lists the JTAG timing parameters and values for Cyclone IV devices.

Table 1–30. JTAG Timing Parameters for Cyclone IV Devices *(1)*

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	40	—	ns
t_{JCH}	TCK clock high time	19	—	ns
t_{JCL}	TCK clock low time	19	—	ns
t_{JPSU_TDI}	JTAG port setup time for TDI	1	—	ns
t_{JPSU_TMS}	JTAG port setup time for TMS	3	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output *(2), (3)*	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output *(2), (3)*	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance *(2), (3)*	—	15	ns
t_{JSSU}	Capture register setup time	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 1–30:

(1) For more information about JTAG waveforms, refer to "JTAG Waveform" in "Glossary" on page 1–37.

(2) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 16 ns.

(3) For EP4CGX22, EP4CGX30 (F324 and smaller package), EP4CGX110, and EP4CGX150 devices, the output time specification for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins is 16 ns. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 18 ns.

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/Os using the SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speeds. I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-LVTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.

Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 2 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{LOCK} (2)	—	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–32:

(1) Emulated RSDS_E_1R transmitter is supported at the output pin of all I/O Banks of Cyclone IV E devices and I/O Banks 3, 4, 5, 6, 7, 8, and 9 of Cyclone IV GX devices.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–33. Mini-LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×8	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×7	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×4	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×2	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×1	5	—	400	5	—	311	5	—	311	5	—	311	5	—	265	MHz
Device operation in Mbps	×10	100	—	400	100	—	311	100	—	311	100	—	311	100	—	265	Mbps
	×8	80	—	400	80	—	311	80	—	311	80	—	311	80	—	265	Mbps
	×7	70	—	400	70	—	311	70	—	311	70	—	311	70	—	265	Mbps
	×4	40	—	400	40	—	311	40	—	311	40	—	311	40	—	265	Mbps
	×2	20	—	400	20	—	311	20	—	311	20	—	311	20	—	265	Mbps
	×1	10	—	400	10	—	311	10	—	311	10	—	311	10	—	265	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	—	—	700	ps
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{LOCK} (3)	—	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–33:

(1) Applicable for true and emulated mini-LVDS transmitter.

(2) Cyclone IV E—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated mini-LVDS transmitter is supported at the output pin of all I/O banks.
Cyclone IV GX—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(3) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–34. True LVDS Transmitter Timing Specifications for Cyclone IV Devices *(1), (3)*

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{HSCLK} (input clock frequency)	×10	5	420	5	370	5	320	5	320	5	250	MHz
	×8	5	420	5	370	5	320	5	320	5	250	MHz
	×7	5	420	5	370	5	320	5	320	5	250	MHz
	×4	5	420	5	370	5	320	5	320	5	250	MHz
	×2	5	420	5	370	5	320	5	320	5	250	MHz
	×1	5	420	5	402.5	5	402.5	5	362	5	265	MHz
HSIODR	×10	100	840	100	740	100	640	100	640	100	500	Mbps
	×8	80	840	80	740	80	640	80	640	80	500	Mbps
	×7	70	840	70	740	70	640	70	640	70	500	Mbps
	×4	40	840	40	740	40	640	40	640	40	500	Mbps
	×2	20	840	20	740	20	640	20	640	20	500	Mbps
	×1	10	420	10	402.5	10	402.5	10	362	10	265	Mbps
t_{DUTY}	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	—	600	—	700	ps
t_{LOCK} *(2)*	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1–34:

(1) Cyclone IV E—true LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6.
Cyclone IV GX—true LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices *(1), (3)* **(Part 1 of 2)**

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{HSCLK} (input clock frequency)	×10	5	320	5	320	5	275	5	275	5	250	MHz
	×8	5	320	5	320	5	275	5	275	5	250	MHz
	×7	5	320	5	320	5	275	5	275	5	250	MHz
	×4	5	320	5	320	5	275	5	275	5	250	MHz
	×2	5	320	5	320	5	275	5	275	5	250	MHz
	×1	5	402.5	5	402.5	5	402.5	5	362	5	265	MHz
HSIODR	×10	100	640	100	640	100	550	100	550	100	500	Mbps
	×8	80	640	80	640	80	550	80	550	80	500	Mbps
	×7	70	640	70	640	70	550	70	550	70	500	Mbps
	×4	40	640	40	640	40	550	40	550	40	500	Mbps
	×2	20	640	20	640	20	550	20	550	20	500	Mbps
	×1	10	402.5	10	402.5	10	402.5	10	362	10	265	Mbps

For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interface Handbook*.

Table 1–37 lists the memory output clock jitter specifications for Cyclone IV devices.

Table 1–37. Memory Output Clock Jitter Specifications for Cyclone IV Devices *(1), (2)*

Parameter	Symbol	Min	Max	Unit
Clock period jitter	$t_{JIT(per)}$	–125	125	ps
Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–200	200	ps
Duty cycle jitter	$t_{JIT(duty)}$	–150	150	ps

Notes to Table 1–37:

(1) Memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2 standard.

(2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock (GCLK) network.

Duty Cycle Distortion Specifications

Table 1–38 lists the worst case duty cycle distortion for Cyclone IV devices.

Table 1–38. Duty Cycle Distortion on Cyclone IV Devices I/O Pins *(1), (2), (3)*

Symbol	C6		C7, I7		C8, I8L, A7		C9L		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Notes to Table 1–38:

(1) The duty cycle distortion specification applies to clock outputs from the PLLs, global clock tree, and IOE driving the dedicated and general purpose I/O pins.

(2) Cyclone IV devices meet the specified duty cycle distortion at the maximum output toggle rate for each combination of I/O standard and current strength.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

OCT Calibration Timing Specification

Table 1–39 lists the duration of calibration for series OCT with calibration at device power-up for Cyclone IV devices.

Table 1–39. Timing Specification for Series OCT with Calibration at Device Power-Up for Cyclone IV Devices *(1)*

Symbol	Description	Maximum	Units
t_{OCTCAL}	Duration of series OCT with calibration at device power-up	20	µs

Note to Table 1–39:

(1) OCT calibration takes place after device configuration and before entering user mode.

IOE Programmable Delay

Table 1–40 and Table 1–41 list the IOE programmable delay for Cyclone IV E 1.0 V core voltage devices.

Table 1–40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Devices *(1), (2)*

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset					Unit
				Fast Corner		Slow Corner			
				C8L	I8L	C8L	C9L	I8L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.054	1.924	3.387	4.017	3.411	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.010	1.875	3.341	4.252	3.367	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.641	0.631	1.111	1.377	1.124	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.971	0.931	1.684	2.298	1.684	ns

Notes to Table 1–40:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–41. IOE Programmable Delay on Row Pins for Cyclone IV E 1.0 V Core Voltage Devices *(1), (2)*

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset					Unit
				Fast Corner		Slow Corner			
				C8L	I8L	C8L	C9L	I8L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.057	1.921	3.389	4.146	3.412	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.059	1.919	3.420	4.374	3.441	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.670	0.623	1.160	1.420	1.168	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.960	0.919	1.656	2.258	1.656	ns

Notes to Table 1–41:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices *(1), (2)*

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset								Unit
				Fast Corner			Slow Corner					
				C6	I7	A7	C6	C7	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.211	1.211	2.177	2.340	2.433	2.388	2.508	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.307	1.203	1.203	2.19	2.387	2.540	2.430	2.545	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.437	0.402	0.402	0.747	0.820	0.880	0.834	0.873	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.693	0.665	0.665	1.200	1.379	1.532	1.393	1.441	ns

Notes to Table 1–42:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices *(1), (2)*

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset								Unit
				Fast Corner			Slow Corner					
				C6	I7	A7	C6	C7	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.209	1.209	2.201	2.386	2.510	2.429	2.548	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.207	1.207	2.202	2.402	2.558	2.447	2.557	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.458	0.419	0.419	0.783	0.861	0.924	0.875	0.915	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.686	0.657	0.657	1.185	1.360	1.506	1.376	1.422	ns

Notes to Table 1–43:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

I/O Timing

Use the following methods to determine I/O timing:

- the Excel-based I/O Timing
- the Quartus II timing analyzer

The Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get a timing budget estimation as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.

The Excel-based I/O Timing spreadsheet is downloadable from Cyclone IV Devices Literature website.

Glossary

Table 1–46 lists the glossary for this chapter.

Table 1–46. Glossary (Part 1 of 5)

Letter	Term	Definitions
A	—	—
B	—	—
C	—	—
D	—	—
E	—	—
F	f_{HSCLK}	High-speed I/O block: High-speed receiver/transmitter input and output clock frequency.
G	GCLK	Input pin directly to Global Clock network.
	GCLK PLL	Input pin to Global Clock network through the PLL.
H	HSIODR	High-speed I/O block: Maximum/minimum LVDS data transfer rate (HSIODR = 1/TUI).
I	Input Waveforms for the SSTL Differential I/O Standard	

Table 1–46. Glossary (Part 5 of 5)

Letter	Term	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	$V_{DIF(AC)}$	AC differential input voltage: The minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage: The minimum DC input differential voltage required for switching.
	V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V_{IH}	Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage.
	$V_{IH(DC)}$	High-level DC input voltage.
	V_{IL}	Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low.
	$V_{IL\ (AC)}$	Low-level AC input voltage.
	$V_{IL\ (DC)}$	Low-level DC input voltage.
	V_{IN}	DC input voltage.
	V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} – V_{OL}$.
	V_{OH}	Voltage output high: The maximum positive voltage from an output that the device considers is accepted as the minimum positive high level.
	V_{OL}	Voltage output low: The maximum positive voltage from an output that the device considers is accepted as the maximum positive low level.
	V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
	$V_{OX\ (AC)}$	AC differential output cross point voltage: the voltage at which the differential output signals must cross.
	V_{REF}	Reference voltage for the SSTL and HSTL I/O standards.
	$V_{REF\ (AC)}$	AC input reference voltage for the SSTL and HSTL I/O standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise. The peak-to-peak AC noise on V_{REF} must not exceed 2% of $V_{REF(DC)}$.
	$V_{REF\ (DC)}$	DC input reference voltage for the SSTL and HSTL I/O standards.
	$V_{SWING\ (AC)}$	AC differential input voltage: AC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	$V_{SWING\ (DC)}$	DC differential input voltage: DC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	V_{TT}	Termination voltage for the SSTL and HSTL I/O standards.
	$V_{X\ (AC)}$	AC differential input cross point voltage: The voltage at which the differential input signals must cross.
W	—	—
X	—	—
Y	—	—
Z	—	—

Table 1–47. Document Revision History

Date	Version	Changes
February 2010	1.1	■ Updated Table 1–3 through Table 1–44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release. ■ Minor text edits.
November 2009	1.0	Initial release.