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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	4620
Number of Logic Elements/Cells	73920
Total RAM Bits	4257792
Number of I/O	310
Number of Gates	-
Voltage - Supply	1.16V ~ 1.24V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep4cgx75df27c7">https://www.e-xfl.com/product-detail/intel/ep4cgx75df27c7</a>



Cyclone IV E industrial devices I7 are offered with extended operating temperature range.

## Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone IV devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Table 1–1 lists the absolute maximum ratings for Cyclone IV devices.



Conditions beyond those listed in Table 1–1 cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time have adverse effects on the device.

**Table 1–1. Absolute Maximum Ratings for Cyclone IV Devices <sup>(1)</sup>**


Symbol	Parameter	Min	Max	Unit
$V_{CCINT}$	Core voltage, PCI Express® (PCIe®) hard IP block, and transceiver physical coding sublayer (PCS) power supply	–0.5	1.8	V
$V_{CCA}$	Phase-locked loop (PLL) analog power supply	–0.5	3.75	V
$V_{CCD\_PLL}$	PLL digital power supply	–0.5	1.8	V
$V_{CCIO}$	I/O banks power supply	–0.5	3.75	V
$V_{CC\_CLKIN}$	Differential clock input pins power supply	–0.5	4.5	V
$V_{CCH\_GXB}$	Transceiver output buffer power supply	–0.5	3.75	V
$V_{CCA\_GXB}$	Transceiver physical medium attachment (PMA) and auxiliary power supply	–0.5	3.75	V
$V_{CCL\_GXB}$	Transceiver PMA and auxiliary power supply	–0.5	1.8	V
$V_I$	DC input voltage	–0.5	4.2	V
$I_{OUT}$	DC output current, per pin	–25	40	mA
$T_{STG}$	Storage temperature	–65	150	°C
$T_J$	Operating junction temperature	–40	125	°C

**Note to Table 1–1:**

(1) Supply voltage specifications apply to voltage readings taken at the device pins with respect to ground, not at the power supply.

## Maximum Allowed Overshoot or Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to –2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns. Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device.

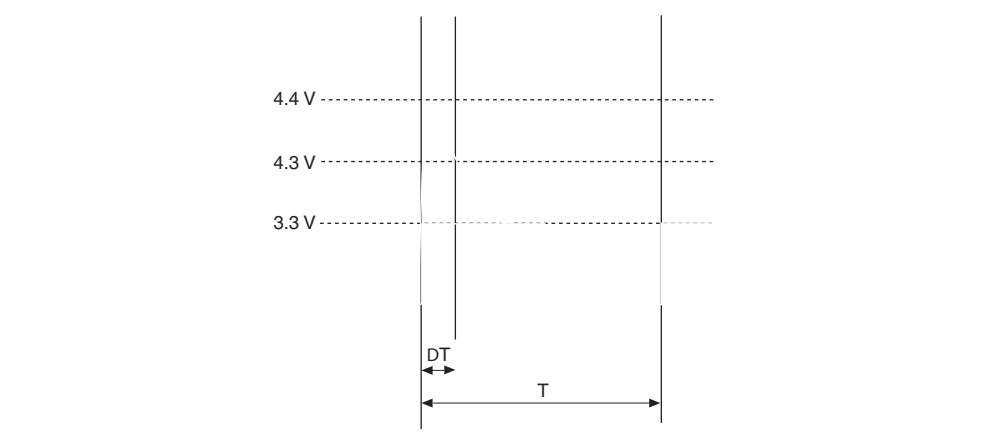
 A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

**Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices**

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit
$V_i$	AC Input Voltage	$V_i = 4.20$	100	%
		$V_i = 4.25$	98	%
		$V_i = 4.30$	65	%
		$V_i = 4.35$	43	%
		$V_i = 4.40$	29	%
		$V_i = 4.45$	20	%
		$V_i = 4.50$	13	%
		$V_i = 4.55$	9	%
		$V_i = 4.60$	6	%

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as  $([\Delta T]/T) \times 100$ . This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

**Figure 1–1. Cyclone IV Devices Overshoot Duration**



## Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone IV devices. Table 1–3 and Table 1–4 list the steady-state voltage and current values expected from Cyclone IV E and Cyclone IV GX devices. All supplies must be strictly monotonic without plateaus.

**Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices <sup>(1)</sup>, <sup>(2)</sup> (Part 1 of 2)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CCINT}^{(3)}$	Supply voltage for internal logic, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply voltage for internal logic, 1.0-V operation	—	0.97	1.0	1.03	V
$V_{CCIO}^{(3), (4)}$	Supply voltage for output buffers, 3.3-V operation	—	3.135	3.3	3.465	V
	Supply voltage for output buffers, 3.0-V operation	—	2.85	3	3.15	V
	Supply voltage for output buffers, 2.5-V operation	—	2.375	2.5	2.625	V
	Supply voltage for output buffers, 1.8-V operation	—	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	—	1.425	1.5	1.575	V
	Supply voltage for output buffers, 1.2-V operation	—	1.14	1.2	1.26	V
$V_{CCA}^{(3)}$	Supply (analog) voltage for PLL regulator	—	2.375	2.5	2.625	V
$V_{CCD\_PLL}^{(3)}$	Supply (digital) voltage for PLL, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply (digital) voltage for PLL, 1.0-V operation	—	0.97	1.0	1.03	V
$V_I$	Input voltage	—	–0.5	—	3.6	V
$V_O$	Output voltage	—	0	—	$V_{CCIO}$	V
$T_J$	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
		For extended temperature	–40	—	125	°C
		For automotive use	–40	—	125	°C
$t_{RAMP}$	Power supply ramp time	Standard power-on reset (POR) <sup>(5)</sup>	50 $\mu$ s	—	50 ms	—
		Fast POR <sup>(6)</sup>	50 $\mu$ s	—	3 ms	—

**Table 1-4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CCA\_GXB}$	Transceiver PMA and auxiliary power supply	—	2.375	2.5	2.625	V
$V_{CCL\_GXB}$	Transceiver PMA and auxiliary power supply	—	1.16	1.2	1.24	V
$V_I$	DC input voltage	—	-0.5	—	3.6	V
$V_O$	DC output voltage	—	0	—	$V_{CCIO}$	V
$T_J$	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	-40	—	100	°C
$t_{RAMP}$	Power supply ramp time	Standard power-on reset (POR) <sup>(7)</sup>	50 $\mu$ s	—	50 ms	—
		Fast POR <sup>(8)</sup>	50 $\mu$ s	—	3 ms	—
$I_{Diode}$	Magnitude of DC current across PCI-clamp diode when enabled	—	—	—	10	mA

**Notes to Table 1-4:**

- (1) All  $V_{CCA}$  pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- (2) You must connect  $V_{CCD\_PLL}$  to  $V_{CCINT}$  through a decoupling capacitor and ferrite bead.
- (3) Power supplies must rise monotonically.
- (4)  $V_{CCIO}$  for all I/O banks must be powered up during device operation. Configurations pins are powered up by  $V_{CCIO}$  of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support  $V_{CCIO}$  of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the  $V_{CCIO}$  level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.
- (5) You must set  $V_{CC\_CLKIN}$  to 2.5 V if you use  $CLKIN$  as a high-speed serial interface (HSSI)  $refclk$  or as a  $DIFFCLK$  input.
- (6) The  $CLKIN$  pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.
- (7) The POR time for Standard POR ranges between 50 and 200 ms.  $V_{CCINT}$ ,  $V_{CCA}$ , and  $V_{CCIO}$  of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.
- (8) The POR time for Fast POR ranges between 3 and 9 ms.  $V_{CCINT}$ ,  $V_{CCA}$ , and  $V_{CCIO}$  of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

## ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1-5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

**Table 1-5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os**

Symbol	Parameter	Passing Voltage	Unit
$V_{ESDHBM}$	ESD voltage using the HBM (GPIOs) <sup>(1)</sup>	$\pm 2000$	V
	ESD using the HBM (HSSI I/Os) <sup>(2)</sup>	$\pm 1000$	V
$V_{ESDCDM}$	ESD using the CDM (GPIOs)	$\pm 500$	V
	ESD using the CDM (HSSI I/Os) <sup>(2)</sup>	$\pm 250$	V

**Notes to Table 1-5:**

- (1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is  $\pm 1000$ V.
- (2) This value is applicable only to Cyclone IV GX devices.

**Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 2 of 2) <sup>(1)</sup>**

Parameter	Condition	V <sub>CCIO</sub> (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

**Note to Table 1–7:**

(1) Bus hold trip points are based on the calculated input voltages from the JEDEC standard.

## OCT Specifications

Table 1–8 lists the variation of OCT without calibration across process, temperature, and voltage (PVT).

**Table 1–8. Series OCT Without Calibration Specifications for Cyclone IV Devices**

Description	$V_{CCIO}$ (V)	Resistance Tolerance		Unit
		Commercial Maximum	Industrial, Extended industrial, and Automotive Maximum	
Series OCT without calibration	3.0	±30	±40	%
	2.5	±30	±40	%
	1.8	±40	±50	%
	1.5	±50	±50	%
	1.2	±50	±50	%

OCT calibration is automatically performed at device power-up for OCT-enabled I/Os.

Table 1–9 lists the OCT calibration accuracy at device power-up.

**Table 1–9. Series OCT with Calibration at Device Power-Up Specifications for Cyclone IV Devices**

Description	$V_{CCIO}$ (V)	Calibration Accuracy		Unit
		Commercial Maximum	Industrial, Extended industrial, and Automotive Maximum	
Series OCT with calibration at device power-up	3.0	±10	±10	%
	2.5	±10	±10	%
	1.8	±10	±10	%
	1.5	±10	±10	%
	1.2	±10	±10	%

**Table 1-16. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Cyclone IV Devices <sup>(1)</sup>**


I/O Standard	V <sub>CCIO</sub> (V)			V <sub>REF</sub> (V)			V <sub>TT</sub> (V) <sup>(2)</sup>		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V <sub>REF</sub> - 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V <sub>REF</sub> - 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 × V <sub>CCIO</sub> <sup>(3)</sup>	0.5 × V <sub>CCIO</sub> <sup>(3)</sup>	0.52 × V <sub>CCIO</sub> <sup>(3)</sup>	—	0.5 × V <sub>CCIO</sub>	—
				0.47 × V <sub>CCIO</sub> <sup>(4)</sup>	0.5 × V <sub>CCIO</sub> <sup>(4)</sup>	0.53 × V <sub>CCIO</sub> <sup>(4)</sup>			

**Notes to Table 1-16:**

- (1) For an explanation of terms used in Table 1-16, refer to “Glossary” on page 1-37.
- (2) V<sub>TT</sub> of the transmitting device must track V<sub>REF</sub> of the receiving device.
- (3) Value shown refers to DC input reference voltage, V<sub>REF(DC)</sub>.
- (4) Value shown refers to AC input reference voltage, V<sub>REF(AC)</sub>.

**Table 1-17. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone IV Devices**

I/O Standard	V <sub>IL(DC)</sub> (V)		V <sub>IH(DC)</sub> (V)		V <sub>IL(AC)</sub> (V)		V <sub>IH(AC)</sub> (V)		V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	I <sub>OL</sub> (mA)	I <sub>OH</sub> (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V <sub>REF</sub> - 0.18	V <sub>REF</sub> + 0.18	—	—	V <sub>REF</sub> - 0.35	V <sub>REF</sub> + 0.35	—	V <sub>TT</sub> - 0.57	V <sub>TT</sub> + 0.57	8.1	-8.1
SSTL-2 Class II	—	V <sub>REF</sub> - 0.18	V <sub>REF</sub> + 0.18	—	—	V <sub>REF</sub> - 0.35	V <sub>REF</sub> + 0.35	—	V <sub>TT</sub> - 0.76	V <sub>TT</sub> + 0.76	16.4	-16.4
SSTL-18 Class I	—	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125	—	—	V <sub>REF</sub> - 0.25	V <sub>REF</sub> + 0.25	—	V <sub>TT</sub> - 0.475	V <sub>TT</sub> + 0.475	6.7	-6.7
SSTL-18 Class II	—	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125	—	—	V <sub>REF</sub> - 0.25	V <sub>REF</sub> + 0.25	—	0.28	V <sub>CCIO</sub> - 0.28	13.4	-13.4
HSTL-18 Class I	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	—	0.4	V <sub>CCIO</sub> - 0.4	8	-8
HSTL-18 Class II	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	—	0.4	V <sub>CCIO</sub> - 0.4	16	-16
HSTL-15 Class I	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	—	0.4	V <sub>CCIO</sub> - 0.4	8	-8
HSTL-15 Class II	—	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	—	—	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	—	0.4	V <sub>CCIO</sub> - 0.4	16	-16
HSTL-12 Class I	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	-0.24	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	V <sub>CCIO</sub> + 0.24	0.25 × V <sub>CCIO</sub>	0.75 × V <sub>CCIO</sub>	8	-8
HSTL-12 Class II	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	-0.24	V <sub>REF</sub> - 0.15	V <sub>REF</sub> + 0.15	V <sub>CCIO</sub> + 0.24	0.25 × V <sub>CCIO</sub>	0.75 × V <sub>CCIO</sub>	14	-14

 For more information about receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *I/O Features in Cyclone IV Devices* chapter.

**Table 1–18. Differential SSTL I/O Standard Specifications for Cyclone IV Devices <sup>(1)</sup>**

I/O Standard	$V_{CCIO}$ (V)			$V_{Swing(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{Swing(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	$V_{CCIO}$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.7	$V_{CCIO}$	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$
SSTL-18 Class I, II	1.7	1.8	1.90	0.25	$V_{CCIO}$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO}$	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$

**Note to Table 1–18:**(1) Differential SSTL requires a  $V_{REF}$  input.**Table 1–19. Differential HSTL I/O Standard Specifications for Cyclone IV Devices <sup>(1)</sup>**

I/O Standard	$V_{CCIO}$ (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO}$	$0.48 \times V_{CCIO}$	—	$0.52 \times V_{CCIO}$	$0.48 \times V_{CCIO}$	—	$0.52 \times V_{CCIO}$	0.3	$0.48 \times V_{CCIO}$

**Note to Table 1–19:**(1) Differential HSTL requires a  $V_{REF}$  input.**Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices <sup>(1)</sup> (Part 1 of 2)**


I/O Standard	$V_{CCIO}$ (V)			$V_{ID}$ (mV)		$V_{ICM}$ (V) <sup>(2)</sup>			$V_{OD}$ (mV) <sup>(3)</sup>			$V_{OS}$ (V) <sup>(3)</sup>		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (Row I/Os) <sup>(6)</sup>	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq 500$ Mbps	1.80	—	—	—	—	—	—
						0.55	$500 \text{ Mbps} \leq D_{MAX} \leq 700$ Mbps	1.80						
						1.05	$D_{MAX} > 700$ Mbps	1.55						
LVPECL (Column I/Os) <sup>(6)</sup>	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq 500$ Mbps	1.80	—	—	—	—	—	—
						0.55	$500 \text{ Mbps} \leq D_{MAX} \leq 700$ Mbps	1.80						
						1.05	$D_{MAX} > 700$ Mbps	1.55						
LVDS (Row I/Os)	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq 500$ Mbps	1.80	247	—	600	1.125	1.25	1.375
						0.55	$500 \text{ Mbps} \leq D_{MAX} \leq 700$ Mbps	1.80						
						1.05	$D_{MAX} > 700$ Mbps	1.55						



Table 1-21. Transceiver Specification for Cyclone IV GX Devices (Part 2 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										
Data rate (F324 and smaller package) <sup>(15)</sup>	—	600	—	2500	600	—	2500	600	—	2500	Mbps
Data rate (F484 and larger package) <sup>(15)</sup>	—	600	—	3125	600	—	3125	600	—	2500	Mbps
Absolute V <sub>MAX</sub> for a receiver pin <sup>(3)</sup>	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V <sub>MAX</sub> for a receiver pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V <sub>MIN</sub> for a receiver pin	—	−0.4	—	—	−0.4	—	—	−0.4	—	—	V
Peak-to-peak differential input voltage V <sub>ID</sub> (diff p-p)	V <sub>ICM</sub> = 0.82 V setting, Data Rate = 600 Mbps to 3.125 Gbps	0.1	—	2.7	0.1	—	2.7	0.1	—	2.7	V
V <sub>ICM</sub>	V <sub>ICM</sub> = 0.82 V setting	—	820 ± 10%	—	—	820 ± 10%	—	—	820 ± 10%	—	mV
Differential on-chip termination resistors	100−Ω setting	—	100	—	—	100	—	—	100	—	Ω
	150−Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PIPE, Serial Rapid I/O SR, SATA, CPRI LV, SDI, XAUI	Compliant									—
Programmable ppm detector <sup>(4)</sup>	—	± 62.5, 100, 125, 200, 250, 300									ppm
Clock data recovery (CDR) ppm tolerance (without spread-spectrum clocking enabled)	—	—	—	±300 <sup>(5)</sup> , ±350 <sup>(6), (7)</sup>	—	—	±300 <sup>(5)</sup> , ±350 <sup>(6), (7)</sup>	—	—	±300 <sup>(5)</sup> , ±350 <sup>(6), (7)</sup>	ppm
CDR ppm tolerance (with synchronous spread-spectrum clocking enabled) <sup>(8)</sup>	—	—	—	350 to −5350 <sup>(7), (9)</sup>	—	—	350 to −5350 <sup>(7), (9)</sup>	—	—	350 to −5350 <sup>(7), (9)</sup>	ppm
Run length	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	No Equalization	—	—	1.5	—	—	1.5	—	—	1.5	dB
	Medium Low	—	—	4.5	—	—	4.5	—	—	4.5	dB
	Medium High	—	—	5.5	—	—	5.5	—	—	5.5	dB
	High	—	—	7	—	—	7	—	—	7	dB

Figure 1-2 shows the lock time parameters in manual mode.

 LTD = lock-to-data. LTR = lock-to-reference.

**Figure 1-2. Lock Time Parameters for Manual Mode**

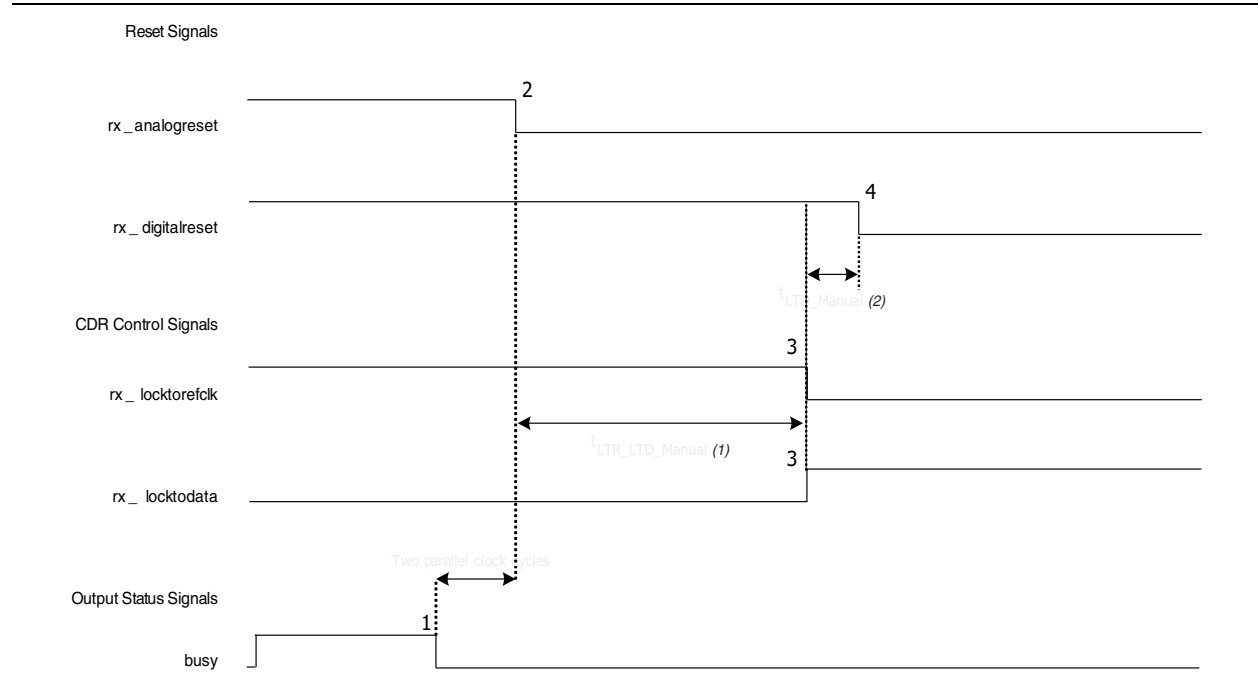


Figure 1-3 shows the lock time parameters in automatic mode.

**Figure 1-3. Lock Time Parameters for Automatic Mode**

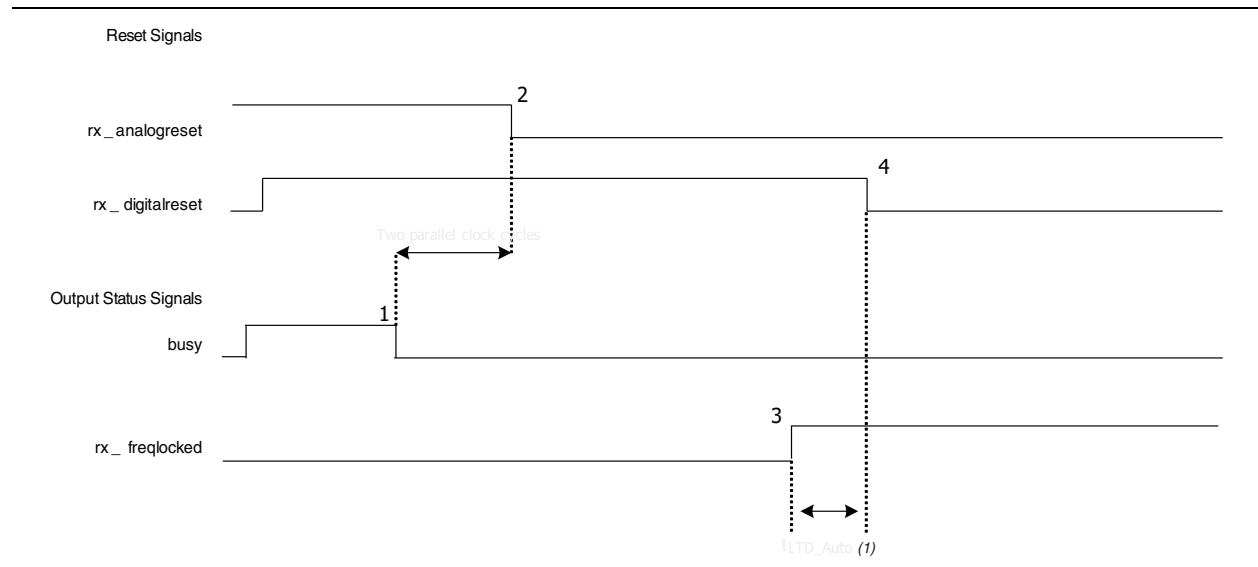


Table 1–23 lists the Cyclone IV GX transceiver block AC specifications.

**Table 1–23. Transceiver Block AC Specification for Cyclone IV GX Devices <sup>(1), (2)</sup>**

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PCIe Transmit Jitter Generation <sup>(3)</sup>											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	—	—	0.25	—	—	0.25	—	—	0.25	UI
PCIe Receiver Jitter Tolerance <sup>(3)</sup>											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	> 0.6			> 0.6			> 0.6			UI
GIGE Transmit Jitter Generation <sup>(4)</sup>											
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance <sup>(4)</sup>											
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI

**Notes to Table 1–23:**

- (1) Dedicated `refclk` pins were used to drive the input reference clocks.
- (2) The jitter numbers specified are valid for the stated conditions only.
- (3) The jitter numbers for PIPE are compliant to the PCIe Base Specification 2.0.
- (4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.

## Core Performance Specifications

The following sections describe the clock tree specifications, PLLs, embedded multiplier, memory block, and configuration specifications for Cyclone IV Devices.

### Clock Tree Specifications

Table 1–24 lists the clock tree specifications for Cyclone IV devices.

**Table 1–24. Clock Tree Performance for Cyclone IV Devices (Part 1 of 2)**

Device	Performance								Unit
	C6	C7	C8	C8L <sup>(1)</sup>	C9L <sup>(1)</sup>	I7	I8L <sup>(1)</sup>	A7	
EP4CE6	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE10	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE15	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE22	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE30	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE40	500	437.5	402	362	265	437.5	362	402	MHz

**Table 1-25. PLL Specifications for Cyclone IV Devices <sup>(1), (2)</sup> (Part 2 of 2)**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{DLOCK}$	Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or $\overline{areset}$ is deasserted)	—	—	1	ms
$t_{OUTJITTER\_PERIOD\_DEDCLK}^{(6)}$	Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER\_CCJ\_DEDCLK}^{(6)}$	Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER\_PERIOD\_IO}^{(6)}$	Regular I/O period jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER\_CCJ\_IO}^{(6)}$	Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{PLL\_PSERR}$	Accuracy of PLL phase shift	—	—	$\pm 50$	ps
$t_{ARESET}$	Minimum pulse width on $\overline{areset}$ signal.	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	3.5 <sup>(7)</sup>	—	SCANCLK cycles
$f_{SCANCLK}$	$scanclk$ frequency	—	—	100	MHz
$t_{CASC\_OUTJITTER\_PERIOD\_DEDCLK}^{(8), (9)}$	Period jitter for dedicated clock output in cascaded PLLs ( $F_{OUT} \geq 100$ MHz)	—	—	425	ps
	Period jitter for dedicated clock output in cascaded PLLs ( $F_{OUT} < 100$ MHz)	—	—	42.5	mUI

**Notes to Table 1-25:**

- (1) This table is applicable for general purpose PLLs and multipurpose PLLs.
- (2) You must connect  $V_{CCD\_PLL}$  to  $V_{CCINT}$  through the decoupling capacitor and ferrite bead.
- (3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (4) The  $V_{CO}$  frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the  $V_{CO}$  post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the  $f_{VCO}$  specification.
- (5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.
- (6) Peak-to-peak jitter with a probability level of  $10^{-12}$  (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.
- (7) With 100-MHz  $scanclk$  frequency.
- (8) The cascaded PLLs specification is applicable only with the following conditions:
  - Upstream PLL— $0.59 \text{ MHz} \leq \text{Upstream PLL bandwidth} < 1 \text{ MHz}$
  - Downstream PLL—Downstream PLL bandwidth  $> 2 \text{ MHz}$
- (9) PLL cascading is not supported for transceiver applications.

## Embedded Multiplier Specifications

Table 1–26 lists the embedded multiplier specifications for Cyclone IV devices.

**Table 1–26. Embedded Multiplier Specifications for Cyclone IV Devices**

Mode	Resources Used	Performance					Unit
	Number of Multipliers	C6	C7, I7, A7	C8	C8L, I8L	C9L	
9 × 9-bit multiplier	1	340	300	260	240	175	MHz
18 × 18-bit multiplier	1	287	250	200	185	135	MHz

## Memory Block Specifications

Table 1–27 lists the M9K memory block specifications for Cyclone IV devices.

**Table 1–27. Memory Block Performance Specifications for Cyclone IV Devices**

Memory	Mode	Resources Used		Performance					Unit
		LEs	M9K Memory	C6	C7, I7, A7	C8	C8L, I8L	C9L	
M9K Block	FIFO 256 × 36	47	1	315	274	238	200	157	MHz
	Single-port 256 × 36	0	1	315	274	238	200	157	MHz
	Simple dual-port 256 × 36 CLK	0	1	315	274	238	200	157	MHz
	True dual port 512 × 18 single CLK	0	1	315	274	238	200	157	MHz

## Configuration and JTAG Specifications

Table 1–28 lists the configuration mode specifications for Cyclone IV devices.

**Table 1–28. Passive Configuration Mode Specifications for Cyclone IV Devices <sup>(1)</sup>**

Programming Mode	V <sub>CCINT</sub> Voltage Level (V)	DCLK f <sub>MAX</sub>	Unit
Passive Serial (PS)	1.0 <sup>(3)</sup>	66	MHz
	1.2	133	MHz
Fast Passive Parallel (FPP) <sup>(2)</sup>	1.0 <sup>(3)</sup>	66	MHz
	1.2 <sup>(4)</sup>	100	MHz

**Notes to Table 1–28:**

- (1) For more information about PS and FPP configuration timing parameters, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter.
- (2) FPP configuration mode supports all Cyclone IV E devices (except for E144 package devices) and EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 only.
- (3) V<sub>CCINT</sub> = 1.0 V is only supported for Cyclone IV E 1.0 V core voltage devices.
- (4) Cyclone IV E devices support 1.2 V V<sub>CCINT</sub>. Cyclone IV E 1.2 V core voltage devices support 133 MHz DCLK f<sub>MAX</sub> for EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, and EP4CE40 only.

Table 1–29 lists the active configuration mode specifications for Cyclone IV devices.

**Table 1–29. Active Configuration Mode Specifications for Cyclone IV Devices**

Programming Mode	DCLK Range	Typical DCLK	Unit
Active Parallel (AP) <sup>(1)</sup>	20 to 40	33	MHz
Active Serial (AS)	20 to 40	33	MHz

**Note to Table 1–29:**

(1) AP configuration mode is only supported for Cyclone IV E devices.

Table 1–30 lists the JTAG timing parameters and values for Cyclone IV devices.

**Table 1–30. JTAG Timing Parameters for Cyclone IV Devices <sup>(1)</sup>**

Symbol	Parameter	Min	Max	Unit
t <sub>JCP</sub>	TCK clock period	40	—	ns
t <sub>JCH</sub>	TCK clock high time	19	—	ns
t <sub>JCL</sub>	TCK clock low time	19	—	ns
t <sub>JPSU_TDI</sub>	JTAG port setup time for TDI	1	—	ns
t <sub>JPSU_TMS</sub>	JTAG port setup time for TMS	3	—	ns
t <sub>JPH</sub>	JTAG port hold time	10	—	ns
t <sub>JPCO</sub>	JTAG port clock to output <sup>(2), (3)</sup>	—	15	ns
t <sub>JPZX</sub>	JTAG port high impedance to valid output <sup>(2), (3)</sup>	—	15	ns
t <sub>JPXZ</sub>	JTAG port valid output to high impedance <sup>(2), (3)</sup>	—	15	ns
t <sub>JSSU</sub>	Capture register setup time	5	—	ns
t <sub>JSH</sub>	Capture register hold time	10	—	ns
t <sub>JSCO</sub>	Update register clock to output	—	25	ns
t <sub>JSZX</sub>	Update register high impedance to valid output	—	25	ns
t <sub>JSXZ</sub>	Update register valid output to high impedance	—	25	ns

**Notes to Table 1–30:**

(1) For more information about JTAG waveforms, refer to “JTAG Waveform” in “Glossary” on page 1–37.


(2) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 16 ns.


(3) For EP4CGX22, EP4CGX30 (F324 and smaller package), EP4CGX110, and EP4CGX150 devices, the output time specification for 3.3-, 3.0-, and 2.5-V LVTTTL/LVCMOS operation of JTAG pins is 16 ns. For 1.8-V LVTTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 18 ns.

## Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/Os using the SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speeds. I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-LVTTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.

 For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interfaces Handbook*.

 Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specifications

Table 1–31 through Table 1–36 list the high-speed I/O timing for Cyclone IV devices. For definitions of high-speed timing specifications, refer to “Glossary” on page 1–37.

**Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices <sup>(1)</sup>, <sup>(2)</sup>, <sup>(4)</sup> (Part 1 of 2)**

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{HSCLK}}$ (input clock frequency)	×10	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×8	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×7	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×4	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×2	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×1	5	—	360	5	—	311	5	—	311	5	—	311	5	—	265	MHz
Device operation in Mbps	×10	100	—	360	100	—	311	100	—	311	100	—	311	100	—	265	Mbps
	×8	80	—	360	80	—	311	80	—	311	80	—	311	80	—	265	Mbps
	×7	70	—	360	70	—	311	70	—	311	70	—	311	70	—	265	Mbps
	×4	40	—	360	40	—	311	40	—	311	40	—	311	40	—	265	Mbps
	×2	20	—	360	20	—	311	20	—	311	20	—	311	20	—	265	Mbps
	×1	10	—	360	10	—	311	10	—	311	10	—	311	10	—	265	Mbps
$t_{\text{DUTY}}$	—	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
Transmitter channel-to-channel skew (TCCS)	—	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	—	—	700	ps
$t_{\text{RISE}}$	20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
$t_{\text{FALL}}$	20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps

**Table 1-31. RSDS Transmitter Timing Specifications for Cyclone IV Devices <sup>(1)</sup>, <sup>(2)</sup>, <sup>(4)</sup> (Part 2 of 2)**

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{\text{LOCK}}$ <sup>(3)</sup>	—	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

**Notes to Table 1-31:**

- (1) Applicable for true RSDS and emulated RSDS\_E\_3R transmitter.
- (2) Cyclone IV E devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated RSDS transmitter is supported at the output pin of all I/O Banks.  
Cyclone IV GX devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (3)  $t_{\text{LOCK}}$  is the time required for the PLL to lock from the end-of-device configuration.
- (4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

**Table 1-32. Emulated RSDS\_E\_1R Transmitter Timing Specifications for Cyclone IV Devices <sup>(1)</sup>, <sup>(3)</sup> (Part 1 of 2)**

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{HCLK}}$ (input clock frequency)	×10	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×8	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×7	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×4	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×2	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×1	5	—	170	5	—	170	5	—	170	5	—	170	5	—	145	MHz
Device operation in Mbps	×10	100	—	170	100	—	170	100	—	170	100	—	170	100	—	145	Mbps
	×8	80	—	170	80	—	170	80	—	170	80	—	170	80	—	145	Mbps
	×7	70	—	170	70	—	170	70	—	170	70	—	170	70	—	145	Mbps
	×4	40	—	170	40	—	170	40	—	170	40	—	170	40	—	145	Mbps
	×2	20	—	170	20	—	170	20	—	170	20	—	170	20	—	145	Mbps
	×1	10	—	170	10	—	170	10	—	170	10	—	170	10	—	145	Mbps
$t_{\text{DUTY}}$	—	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	—	—	700	ps
$t_{\text{RISE}}$	20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
$t_{\text{FALL}}$	20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps



**Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices <sup>(1), (3)</sup> (Part 2 of 2)**

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>DUTY</sub>	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	—	600	—	700	ps
t <sub>LOCK</sub> <sup>(2)</sup>	—	—	1	—	1	—	1	—	1	—	1	ms

**Notes to Table 1–35:**

- (1) Cyclone IV E—emulated LVDS transmitter is supported at the output pin of all I/O Banks.  
Cyclone IV GX—emulated LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2) t<sub>LOCK</sub> is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

**Table 1–36. LVDS Receiver Timing Specifications for Cyclone IV Devices <sup>(1), (3)</sup>**

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f <sub>HCLK</sub> (input clock frequency)	×10	10	437.5	10	370	10	320	10	320	10	250	MHz
	×8	10	437.5	10	370	10	320	10	320	10	250	MHz
	×7	10	437.5	10	370	10	320	10	320	10	250	MHz
	×4	10	437.5	10	370	10	320	10	320	10	250	MHz
	×2	10	437.5	10	370	10	320	10	320	10	250	MHz
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	MHz
HSIODR	×10	100	875	100	740	100	640	100	640	100	500	Mbps
	×8	80	875	80	740	80	640	80	640	80	500	Mbps
	×7	70	875	70	740	70	640	70	640	70	500	Mbps
	×4	40	875	40	740	40	640	40	640	40	500	Mbps
	×2	20	875	20	740	20	640	20	640	20	500	Mbps
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	Mbps
SW	—	—	400	—	400	—	400	—	550	—	640	ps
Input jitter tolerance	—	—	500	—	500	—	550	—	600	—	700	ps
t <sub>LOCK</sub> <sup>(2)</sup>	—	—	1	—	1	—	1	—	1	—	1	ms

**Notes to Table 1–36:**

- (1) Cyclone IV E—LVDS receiver is supported at all I/O Banks.  
Cyclone IV GX—LVDS receiver is supported at I/O Banks 3, 4, 5, 6, 7, 8, and 9.
- (2) t<sub>LOCK</sub> is the time required for the PLL to lock from the end-of-device configuration.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

## External Memory Interface Specifications

The external memory interfaces for Cyclone IV devices are auto-calibrating and easy to implement.

For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interface Handbook*.

Table 1–37 lists the memory output clock jitter specifications for Cyclone IV devices.

**Table 1–37. Memory Output Clock Jitter Specifications for Cyclone IV Devices <sup>(1), (2)</sup>**

Parameter	Symbol	Min	Max	Unit
Clock period jitter	$t_{JIT(per)}$	–125	125	ps
Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–200	200	ps
Duty cycle jitter	$t_{JIT(duty)}$	–150	150	ps

**Notes to Table 1–37:**

- (1) Memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2 standard.
- (2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock (GCLK) network.

## Duty Cycle Distortion Specifications

Table 1–38 lists the worst case duty cycle distortion for Cyclone IV devices.

**Table 1–38. Duty Cycle Distortion on Cyclone IV Devices I/O Pins <sup>(1), (2), (3)</sup>**

Symbol	C6		C7, I7		C8, I8L, A7		C9L		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

**Notes to Table 1–38:**

- (1) The duty cycle distortion specification applies to clock outputs from the PLLs, global clock tree, and IOE driving the dedicated and general purpose I/O pins.
- (2) Cyclone IV devices meet the specified duty cycle distortion at the maximum output toggle rate for each combination of I/O standard and current strength.
- (3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

## OCT Calibration Timing Specification

Table 1–39 lists the duration of calibration for series OCT with calibration at device power-up for Cyclone IV devices.

**Table 1–39. Timing Specification for Series OCT with Calibration at Device Power-Up for Cyclone IV Devices <sup>(1)</sup>**

Symbol	Description	Maximum	Units
$t_{OCTCAL}$	Duration of series OCT with calibration at device power-up	20	μs

**Note to Table 1–39:**

- (1) OCT calibration takes place after device configuration and before entering user mode.

## IOE Programmable Delay

Table 1–40 and Table 1–41 list the IOE programmable delay for Cyclone IV E 1.0 V core voltage devices.

**Table 1–40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Devices <sup>(1), (2)</sup>**

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset					Unit
				Fast Corner		Slow Corner			
				C8L	I8L	C8L	C9L	I8L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.054	1.924	3.387	4.017	3.411	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.010	1.875	3.341	4.252	3.367	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.641	0.631	1.111	1.377	1.124	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.971	0.931	1.684	2.298	1.684	ns

**Notes to Table 1–40:**

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

**Table 1–41. IOE Programmable Delay on Row Pins for Cyclone IV E 1.0 V Core Voltage Devices <sup>(1), (2)</sup>**

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset					Unit
				Fast Corner		Slow Corner			
				C8L	I8L	C8L	C9L	I8L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.057	1.921	3.389	4.146	3.412	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.059	1.919	3.420	4.374	3.441	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.670	0.623	1.160	1.420	1.168	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.960	0.919	1.656	2.258	1.656	ns

**Notes to Table 1–41:**

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

**Table 1–44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices <sup>(1), (2)</sup>**

Parameter	Paths Affected	Number of Settings	Min Offset	Max Offset						Unit
				Fast Corner		Slow Corner				
				C6	I7	C6	C7	C8	I7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.313	1.209	2.184	2.336	2.451	2.387	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.208	2.200	2.399	2.554	2.446	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.438	0.404	0.751	0.825	0.886	0.839	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.713	0.682	1.228	1.41	1.566	1.424	ns

**Notes to Table 1–44:**

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

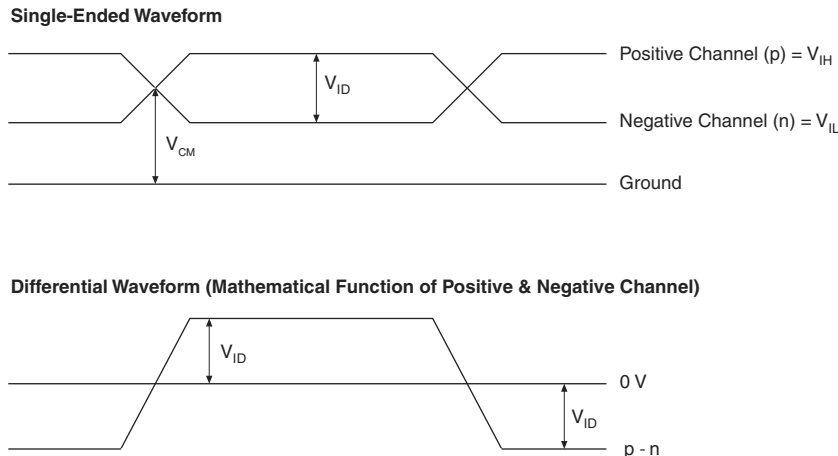
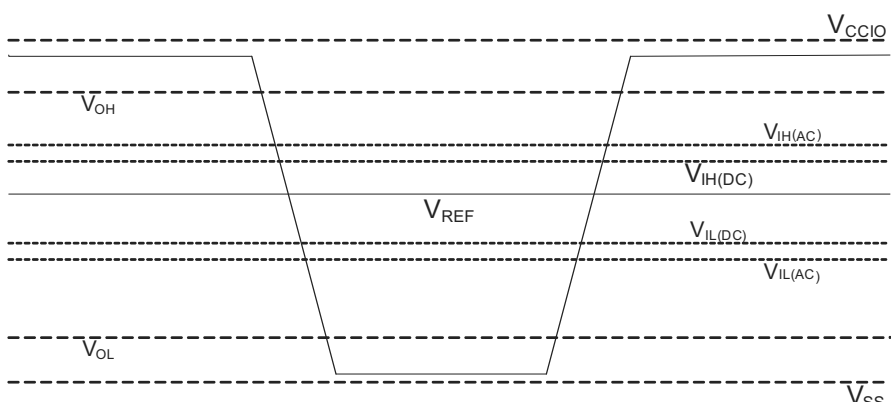
**Table 1–45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices <sup>(1), (2)</sup>**

Parameter	Paths Affected	Number of Settings	Min Offset	Max Offset						Unit
				Fast Corner		Slow Corner				
				C6	I7	C6	C7	C8	I7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.210	2.209	2.398	2.526	2.443	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.313	1.208	2.205	2.406	2.563	2.450	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.461	0.421	0.789	0.869	0.933	0.884	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.712	0.682	1.225	1.407	1.562	1.421	ns

**Notes to Table 1–45:**

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software

Table 1-46. Glossary (Part 3 of 5)

Letter	Term	Definitions
R	$R_L$	Receiver differential input discrete resistor (external to Cyclone IV devices).
	Receiver Input Waveform	<p>Receiver input waveform for LVDS and LVPECL differential standards:</p> 
	Receiver input skew margin (RSKM)	High-speed I/O block: The total margin left after accounting for the sampling window and TCCS. $RSKM = (TUI - SW - TCCS) / 2$ .
S	Single-ended voltage-referenced I/O Standard	 <p>The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform <i>ringing</i>.</p>
	SW (Sampling Window)	High-speed I/O block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window.