Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), CANbus, LINbus, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f580-iq

1. System Overview

C8051F58x/F59x devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 50 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- Controller Area Network (CAN 2.0B) Controller with 32 message objects, each with its own indentifier mask (C8051F580/2/4/6/8-F590)
- LIN 2.1 peripheral (fully backwards compatible, master and slave modes) (C8051F580/2/4/6/8-F590)
- True 12-bit 200 ksps 32-channel single-ended ADC with analog multiplexer
- Precision programmable 24 MHz internal oscillator that is within ±0.5% across the temperature range and for VDD voltages greater than or equal to the on-chip voltage regulator minimum output at the low setting. The oscillator is within ±1.0% for VDD voltages below this minimum output setting.
- On-chip Clock Multiplier to reach up to 50 MHz
- 128 kB (C8051F580/1/2/3/8/9) or 96 kB (C8051F584/5/6/7-F590/1) of on-chip Flash memory
- 8448 bytes of on-chip RAM
- SMBus/I2C, Two Enhanced UARTs, and Enhanced SPI serial interfaces implemented in hardware
- Six general-purpose 16-bit timers
- External Data Memory Interface (C8051F580/1/4/5) with 64 kB address space
- Two Programmable Counter/Timer Array (PCA) modules with six capture/compare modules each and one with a Watchdog Timer function
- Three Voltage Comparators
- On-chip Voltage Regulator
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- 40, 33 or 25 Port I/O (5 V push-pull)

With an on-chip Voltage Regulator, Power-On Reset and V_{DD} monitors, Watchdog Timer, and clock oscillator, the C8051F58x/F59x devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

The devices are specified for 1.8 V to 5.25 V operation over the automotive temperature range (–40 to +125 °C). The Port I/O and $\overline{RST}$ pins can interface to 5 V logic by setting the VIO pin to 5 V. The C8051F580/1/4/5 devices are available in 48-pin QFP and QFN packages, and the C8051F588/9-F590/1 devices are available in a 40-pin QFN package, and the C8051F582/3/6/7 devices are available in 32-pin QFP and QFN packages. All package options are lead-free and RoHS compliant. See Table 2.1 for ordering information. Block diagrams are included in Figure 1.1 and Figure 1.3.

For example, if ADC0GNH = 0xFC, ADC0GNL = 0x00, and GAINADD = 1, GAIN = 0xFC0 = 4032, and the resulting equation is as follows:

$$GAIN = \left(\frac{4032}{4096}\right) + 1 \times \left(\frac{1}{64}\right) = 0.984 + 0.016 = 1.0$$

The table below equates values in the ADC0GNH, ADC0GNL, and ADC0GNA registers to the equivalent gain using this equation.

ADC0GNH Value	ADC0GNL Value	GAINADD Value	GAIN Value	Equivalent Gain
0xFC (default)	0x00 (default)	1 (default)	4032 + 64	1.0 (default)
0x7C	0x00	1	1984 + 64	0.5
0xBC	0x00	1	3008 + 64	0.75
0x3C	0x00	1	960 + 64	0.25
0xFF	0xF0	0	4095 + 0	~1.0
0xFF	0xF0	1	4096 + 64	1.016

For any desired gain value, the GAIN registers can be calculated by the following:

$$GAIN = \left(gain - GAINADD \times \left(\frac{1}{64}\right)\right) \times 4096$$

Equation 6.3. Calculating the ADC0GNH and ADC0GNL Values from the Desired Gain

Where:
GAIN is the 12-bit word of ADC0GNH[7:0] and ADC0GNL[7:4]
GAINADD is the value of the GAINADD bit (ADC0GNA.0)
gain is the equivalent gain value from 0 to 1.016

When calculating the value of GAIN to load into the ADC0GNH and ADC0GNL registers, the GAINADD bit can be turned on or off to reach a value closer to the desired gain value.

For example, the initial example in this section requires a gain of 0.44 to convert 5 V full scale to 2.2 V full scale. Using Equation 6.3:

$$GAIN = \left(0.44 - GAINADD \times \left(\frac{1}{64}\right)\right) \times 4096$$

If GAINADD is set to 1, this makes the equation:

$$GAIN = \left(0.44 - 1 \times \left(\frac{1}{64}\right)\right) \times 4096 = 0.424 \times 4096 = 1738 = 0x06CA$$

The actual gain from setting GAINADD to 1 and ADC0GNH and ADC0GNL to 0x6CA is 0.4399. A similar gain can be achieved if GAINADD is set to 0 with a different value for ADC0GNH and ADC0GNL.

SFR Definition 6.4. ADC0CF: ADC0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	AD0SC[4:0]					AD0RPT[1:0]		GAINEN
Type	R/W					R/W	R/W	R/W
Reset	1	1	1	1	1	0	0	0

SFR Address = 0xBC; SFR Page = 0x00

Bit	Name	Function
7:3	AD0SC[4:0]	**ADC0 SAR Conversion Clock Period Bits.** SAR Conversion clock is derived from system clock by the following equation, where *AD0SC* refers to the 5-bit value held in bits AD0SC4–0. SAR Conversion clock requirements are given in the ADC specification table BURSTEN = 0: FCLK is the current system clock BURSTEN = 1: FLCLK is a maximum of 30 Mhz, independent of the current system clock.. $AD0SC = \frac{FCLK}{CLK_{SAR}} - 1$ **Note:** Round up the result of the calculation for AD0SC
2:1	A0RPT[1:0]	**ADC0 Repeat Count.** Controls the number of conversions taken and accumulated between ADC0 End of Conversion (ADCINT) and ADC0 Window Comparator (ADCWINT) interrupts. A convert start is required for each conversion unless Burst Mode is enabled. In Burst Mode, a single convert start can initiate multiple self-timed conversions. Results in both modes are accumulated in the ADC0H:ADC0L register. **When AD0RPT1–0 are set to a value other than '00', the AD0LJST bit in the ADC0CN register must be set to '0' (right justified).** 00: 1 conversion is performed. 01: 4 conversions are performed and accumulated. 10: 8 conversions are performed and accumulated. 11: 16 conversions are performed and accumulated.
0	GAINEN	**Gain Enable Bit.** Controls the gain programming. Refer to Section “6.3. Selectable Gain” on page 60 for information about using this bit.

SFR Definition 9.9. CPT2MX: Comparator2 MUX Selection

Bit	7	6	5	4	3	2	1	0
Name	CMX2N[3:0]				CMX2P[3:0]			
Type	R/W				R/W			
Reset	0	1	1	1	0	1	1	1

SFR Address = 0x9C; SFR Page = 0x10

Bit	Name	Function
7:4	CMX2N[3:0]	**Comparator2 Negative Input MUX Selection.** 0000: P0.1 0001: P0.3 0010: P0.5 0011: P0.7 0100: P1.1 0101: P1.3 0110: P1.5 0111: P1.7 1000: P2.1 1001: P2.3 1010: P2.5 1011: P2.7 1100–1111: None
3:0	CMX2P[3:0]	**Comparator2 Positive Input MUX Selection.** 0000: P0.0 0001: P0.2 0010: P0.4 0011: P0.6 0100: P1.0 0101: P1.2 0110: P1.4 0111: P1.6 1000: P2.0 1001: P2.2 1010: P2.4 1011: P2.6 1100–1111: None

12. Memory Organization

The memory organization of the CIP-51 System Controller is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. The memory organization is shown in Figure 12.1

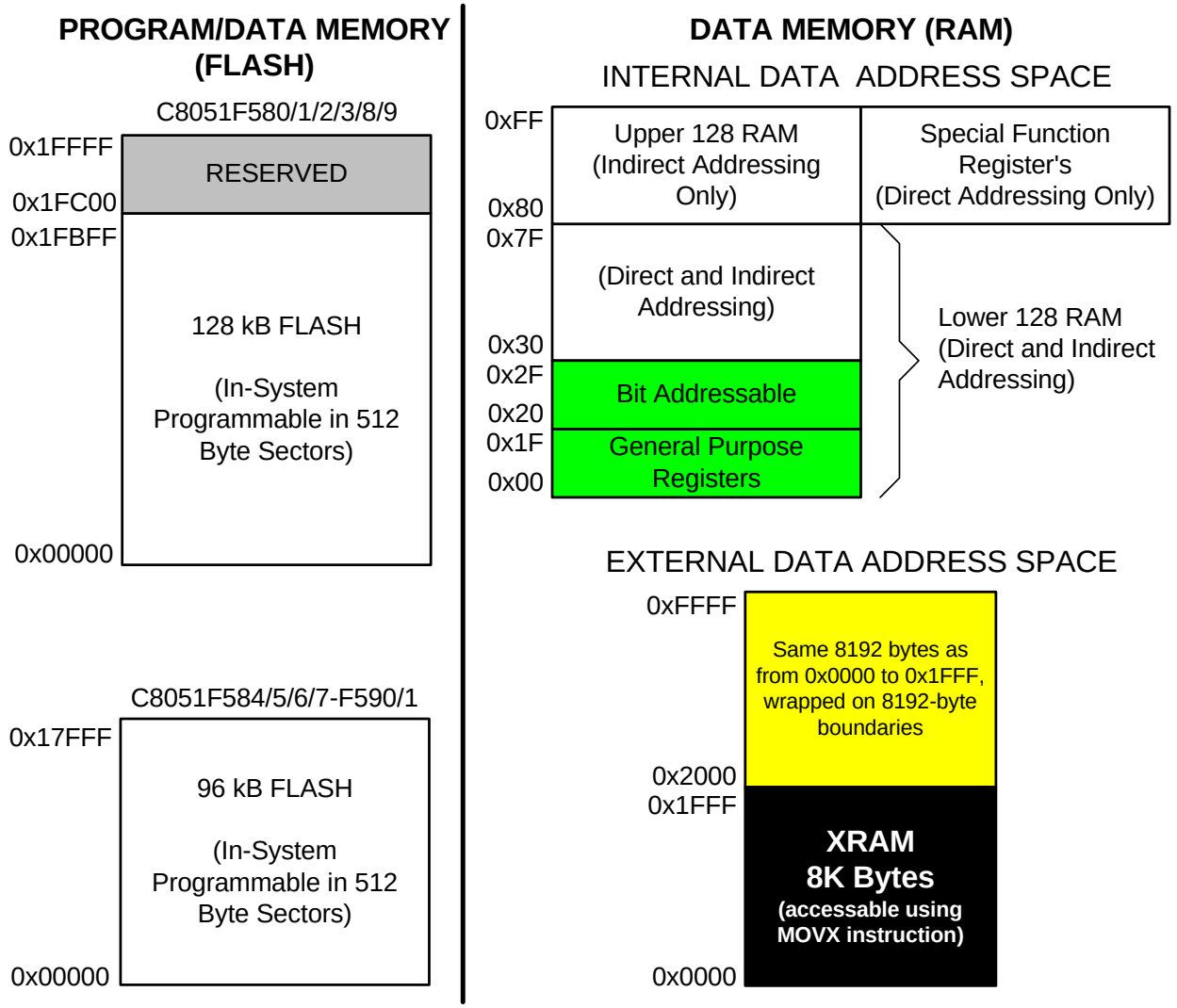

Figure 12.1. C8051F58x/F59x Memory Map

12.1. Program Memory

The C8051F580/1/2/3/8/9 devices have a 128 kB program memory space and the C8051F584/5/6/7-F590/1 devices have 96 kB program memory space. The MCU implements this program memory space as in-system re-programmable Flash memory in either four or three 32 kB code banks. A common code bank (Bank 0) of 32 kB is always accessible from addresses 0x0000 to 0x7FFF. The three or two upper code banks (Bank 1, Bank 2, and Bank 3) are each mapped to addresses 0x8000 to 0xFFFF, depending on the selection of bits in the PSBANK register, as described in SFR Definition 12.1.

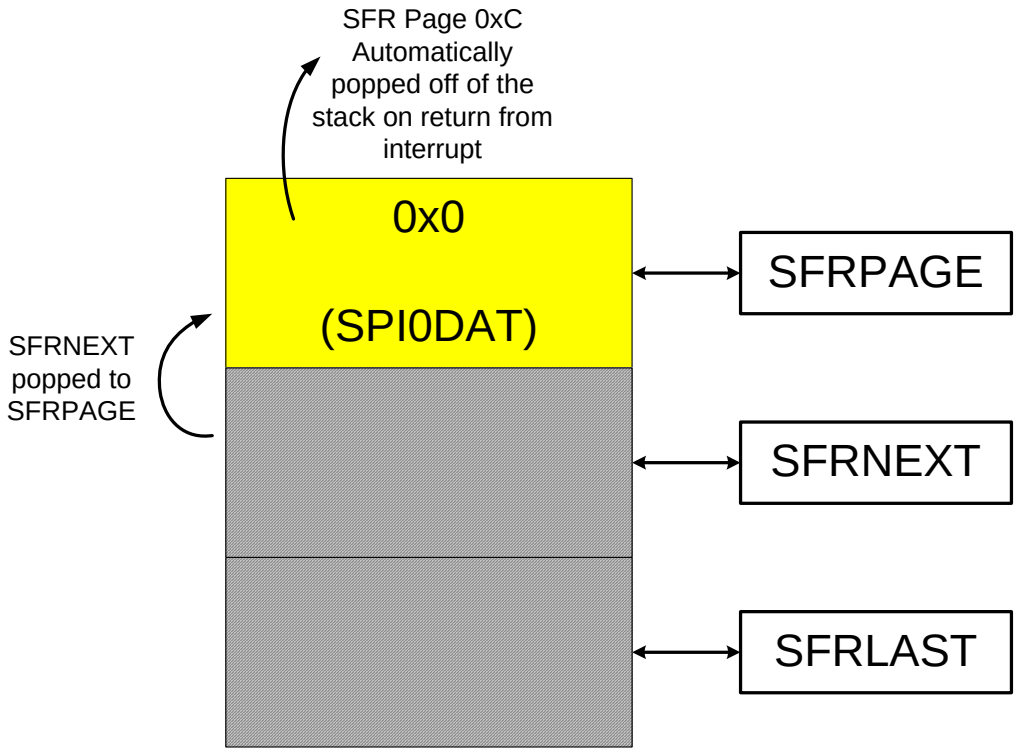

Figure 13.6. SFR Page Stack Upon Return From CAN0 Interrupt

In the example above, all three bytes in the SFR Page Stack are accessible via the SFRPAGE, SFRNEXT, and SFRLAST special function registers. If the stack is altered while servicing an interrupt, it is possible to return to a different SFR Page upon interrupt exit than selected prior to the interrupt call. Direct access to the SFR Page stack can be useful to enable real-time operating systems to control and manage context switching between multiple tasks.

Push operations on the SFR Page Stack only occur on interrupt service, and pop operations only occur on interrupt exit (execution on the RETI instruction). The automatic switching of the SFRPAGE and operation of the SFR Page Stack as described above can be disabled in software by clearing the SFR Automatic Page Enable Bit (SFRPGEN) in the SFR Page Control Register (SFR0CN). See SFR Definition 13.1.

Table 13.1. Special Function Register (SFR) Memory Map for Pages 0x00, 0x10, and 0x0F

Address	Page	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
F8	00 10 0F	SPI0CN	PCA0L PCA1L SN0	PCA0H PCA1H SN1	PCA0CPL0 PCA1CPL6 SN2	PCA0CPH0 PCA1CPH6 SN3	PCACPL4 PCA1CPL10	PCACPH4 PCA1CPH10	VDM0CN
F0	00 10 0F	B (All Pages)	P0MAT P0MDIN	P0MASK P1MDIN	P1MAT P2MDIN	P1MASK P3MDIN	PSBANK (All Pages)	EIP1 EIP1	EIP2 EIP2
E8	00 10 0F	ADC0CN	PCA0CPL1 PCA1CPL7	PCA0CPH1 PCA1CPH7	PCA0CPL2 PCA1CPL8	PCA0CPH2 PCA1CPH8	PCA0CPL3 PCA1CPL9	PCA0CPL3 PCA1CPL9	RSTSRC
E0	00 10 0F	ACC (All Pages)	XBR0	XBR1	CCH0CN	IT01CF		EIE1 (All Pages)	EIE2 (All Pages)
D8	00 10 0F	PCA0CN PCA1CN	PCA0MD PCA1MD PCA0PWM	PCA0CPM0 PCA1CPM6	PCA0CPM1 PCA1CPM7	PCA0CPM2 PCA1CPM8	PCA0CPM3P CA1CPM9	PCA0CPM4P CA1CPM10	PCA0CPM5 PCA1CPM11
D0	00 10 0F	PSW (All Pages)	REF0CN	LIN0DATA	LIN0ADDR	P0SKIP	P1SKIP	P2SKIP	P3SKIP
C8	00 10 0F	TMR2CN TMR4CN	REG0CN TMR4CF LIN0CF	TMR2RLL TMR4CAPL	TMR2RLH TMR4CAPH	TMR2L TMR4L	TMR2H TMR4H	PCA0CPL5 PCA1CPL11	PCA0CPH5 PCA1CPH11
C0	00 10 0F	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH XBR3	 XBR2
B8	00 10 0F	IP (All Pages)		ADC0TK	ADC0MX	ADC0CF	ADC0L	ADC0H	
B0	00 10 0F	P3 (All Pages)	P2MAT	P2MASK EMI0CF			P4 (All Pages)	FLSCL (All Pages)	FLKEY (All Pages)
A8	00 10 0F	IE (All Pages)	SMOD0	EMI0CN EMI0TC	 SBCON0	 SBRLL0	 SBRLH0	P3MAT P3MDOUT	P3MASK P4MDOUT
A0	00 10 0F	P2 (All Pages)	SPI0CFG OSCICN	SPI0CKR OSCICRS	SPI0DAT	 P0MDOUT	 P1MDOUT	 P2MDOUT	SFRPAGE (All Pages)
98	00 10 0F	SCON0 SCON1	SBUF0 SBUF1	CPT0CN CPT2CN	CPT0MD CPT2MD	CPT0MX CPT2MX	CPT1CN	CPT1MD OSCIFIN	CPT1MX OSCXCN
		0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

(bit addressable)

Table 13.2. Special Function Register (SFR) Memory Map for Page 0x0C

	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
F8			CAN0IF2DA2L	CAN0IF2DA2H	CAN0IF2DB1L	CAN0IF2DB1H	CAN0IF2DB2L	CAN0IF2DB2H
F0	B (All Pages)		CAN0IF2A2L	CAN0IF2A2H			CAN0IF2DA1L	CAN0IF2DA1H
E8			CAN0IF2M1L	CAN0IF2M1H	CAN0IF2M2L	CAN0IF2M2H	CAN0IF2A1L	CAN0IF2A1H
E0	ACC (All Pages)		CAN0IF2CML	CAN0IF2CMH			EIE1 (All Pages)	EIE2 (All Pages)
D8			CAN0IF1DB1L	CAN0IF1DB1H	CAN0IF1DB2L	CAN0IF1DB2H	CAN0IF2CRL	CAN0IF2CRH
D0	PSW (All Pages)		CAN0IF1MCL	CAN0IF1MCH	CAN0IF1DA1L	CAN0IF1DA1H	CAN0IF1DA2L	CAN0IF1DA2H
C8			CAN0IF1A1L	CAN0IF1A1H	CAN0IF1A2L	CAN0IF1A2H	CAN0IF2MCL	CAN0IF2MCH
C0	CAN0CN		CAN0IF1CML	CAN0IF1CMH	CAN0IF1M1L	CAN0IF1M1H	CAN0IF1M2L	CAN0IF1M2H
B8	IP (All Pages)		CAN0MV1L	CAN0MV1H	CAN0MV2L	CAN0MV2H	CAN0IF1CRL	CAN0IF1CRH
B0	P3 (All Pages)		CAN0IP2L	CAN0IP2H		P4 (All Pages)	FLSCL (All Pages)	FLKEY (All Pages)
A8	IE (All Pages)		CAN0ND1L	CAN0ND1H	CAN0ND2L	CAN0ND2H	CAN0IP1L	CAN0IP1H
A0	P2 (All Pages)	CAN0BRPE	CAN0TR1L	CAN0TR1H	CAN0TR2L	CAN0TR2H		SFRPAGE (All Pages)
98	SCON0 (All Pages)		CAN0BTL	CAN0BTH	CAN0IIDL	CAN0IIDH	CAN0TST	
90	P1 (All Pages)		CAN0CFG		CAN0STAT		CAN0ERRL	CAN0ERRH
88	TCON (All Pages)	TMOD (All Pages)	TL0 (All Pages)	TL1 (All Pages)	TH0 (All Pages)	TH1 (All Pages)	CKCON (All Pages)	
80	P0 (All Pages)	SP (All Pages)	DPL (All Pages)	DPH (All Pages)		SFRNEXT (All Pages)	SFRLAST (All Pages)	PCON (All Pages)
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

(bit addressable)

Table 13.3. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
ACC	0xE0	Accumulator	99
ADC0CF	0xBC	ADC0 Configuration	65
ADC0CN	0xE8	ADC0 Control	67
ADC0GTH	0xC4	ADC0 Greater-Than Compare High	69
ADC0GTL	0xC3	ADC0 Greater-Than Compare Low	69
ADC0H	0xBE	ADC0 High	66
ADC0L	0xBD	ADC0 Low	66
ADC0LTH	0xC6	ADC0 Less-Than Compare Word High	70
ADC0LTL	0xC5	ADC0 Less-Than Compare Word Low	70
ADC0MX	0xBB	ADC0 Mux Configuration	73
ADC0TK	0xBA	ADC0 Tracking Mode Select	68
B	0xF0	B Register	99
CCH0CN	0xE3	Cache Control	148
CKCON	0x8E	Clock Control	286
CLKMUL	0x97	Clock Multiplier	182
CLKSEL	0x8F	Clock Select	177
CPT0CN	0x9A	Comparator0 Control	79
CPT0MD	0x9B	Comparator0 Mode Selection	80
CPT0MX	0x9C	Comparator0 MUX Selection	86
CPT1CN	0x9D	Comparator1 Control	79
CPT1MD	0x9E	Comparator1 Mode Selection	80
CPT1MX	0x9F	Comparator1 MUX Selection	86
CPT2CN	0x9A	Comparator2 Control	83
CPT2MD	0x9B	Comparator2 Mode Selection	84
CPT2MX	0x9C	Comparator2 MUX Selection	88
DPH	0x83	Data Pointer High	98
DPL	0x82	Data Pointer Low	98
EIE1	0xE6	Extended Interrupt Enable 1	132
EIE2	0xE7	Extended Interrupt Enable 2	132
EIP1	0xF6	Extended Interrupt Priority 1	133
EIP2	0xF7	Extended Interrupt Priority 2	134
EMI0CF	0xB2	External Memory Interface Configuration	163
EMI0CN	0xAA	External Memory Interface Control	162
EMI0TC	0xAA	External Memory Interface Timing Control	168
FLKEY	0xB7	Flash Lock and Key	146

SFR Definition 14.5. EIE2: Extended Interrupt Enable 2

Bit	7	6	5	4	3	2	1	0
Name	ET5	ET4	ECP2	EPCA1	ES1	EMAT	ECAN0	EREG0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE7; SFR Page = All Pages

Bit	Name	Function
7	ET5	**Enable Timer 5 Interrupt.** This bit sets the masking of the Timer 5 interrupt. 0: Disable Timer 5 interrupts. 1: Enable interrupt requests generated by the TF5L or TF5H flags.
6	ET4	**Enable Timer 4 Interrupt.** This bit sets the masking of the Timer 4 interrupt. 0: Disable Timer 4 interrupts. 1: Enable interrupt requests generated by the TF4L or TF4H flags.
5	ECP2	**Enable Comparator2 (CP2) Interrupt.** This bit sets the masking of the CP2 interrupt. 0: Disable CP2 interrupts. 1: Enable interrupt requests generated by the CP2RIF or CP2FIF flags.
4	EPCA1	**Enable Programmable Counter Array (PCA1) Interrupt.** This bit sets the masking of the PCA1 interrupts. 0: Disable all PCA1 interrupts. 1: Enable interrupt requests generated by PCA1
3	ES1	**Enable UART1 Interrupt.** This bit sets the masking of the UART1 interrupt. 0: Disable UART1 interrupt. 1: Enable UART1 interrupt
2	EMAT	**Enable Port Match Interrupt.** This bit sets the masking of the Port Match interrupt. 0: Disable all Port Match interrupts. 1: Enable interrupt requests generated by a Port Match
1	ECAN0	**Enable CAN0 Interrupts.** This bit sets the masking of the CAN0 interrupt. 0: Disable all CAN0 interrupts. 1: Enable interrupt requests generated by CAN0.
0	EREG0	**Enable Voltage Regulator Dropout Interrupt.** This bit sets the masking of the Voltage Regulator Dropout interrupt. 0: Disable the Voltage Regulator Dropout interrupt. 1: Enable the Voltage Regulator Dropout interrupt.

SFR Definition 15.1. PSCTL: Program Store R/W Control

Bit	7	6	5	4	3	2	1	0
Name							PSEE	PSWE
Type	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8F; SFR Page = 0x00

Bit	Name	Function
7:2	Unused	Read = 000000b, Write = don't care.
1	PSEE	**Program Store Erase Enable.** Setting this bit (in combination with PSWE) allows an entire page of Flash program memory to be erased. If this bit is logic 1 and Flash writes are enabled (PSWE is logic 1), a write to Flash memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter. 0: Flash program memory erasure disabled. 1: Flash program memory erasure enabled.
0	PSWE	**Program Store Write Enable.** Setting this bit allows writing a byte of data to the Flash program memory using the MOVX write instruction. The Flash location should be erased before writing data. 0: Writes to Flash program memory disabled. 1: Writes to Flash program memory enabled; the MOVX write instruction targets Flash memory.

19.2. Programmable Internal Oscillator

All C8051F58x/F59x devices include a programmable internal high-frequency oscillator that defaults as the system clock after a system reset. The internal oscillator period can be adjusted via the OSCICRS and OSCIFIN registers defined in SFR Definition 19.3 and SFR Definition 19.4. On C8051F58x/F59x devices, OSCICRS and OSCIFIN are factory calibrated to obtain a 24 MHz base frequency. Note that the system clock may be derived from the programmed internal oscillator divided by 1, 2, 4, 8, 16, 32, 64, or 128, as defined by the IFCN bits in register OSCICN. The divide value defaults to 128 following a reset.

19.2.1. Internal Oscillator Suspend Mode

When software writes a logic 1 to SUSPEND (OSCICN.5), the internal oscillator is suspended. If the system clock is derived from the internal oscillator, the input clock to the peripheral or CIP-51 will be stopped until one of the following events occur:

- Port 0 Match Event.
- Port 1 Match Event.
- Port 2 Match Event.
- Port 3 Match Event.
- Comparator 0 enabled and output is logic 0.

When one of the oscillator awakening events occur, the internal oscillator, CIP-51, and affected peripherals resume normal operation, regardless of whether the event also causes an interrupt. The CPU resumes execution at the instruction following the write to SUSPEND.

Note: When entering suspend mode, firmware must be the ZTCEN bit in REF0CN (SFR Definition 8.1).

Important Note on Crossbar Configuration: If a Port pin is claimed by a peripheral without use of the Crossbar, its corresponding PnSKIP bit should be set. This applies to P0.0 if VREF is used, P0.1 if the ADC is configured to use the external conversion start signal (CNVSTR), P0.3 and/or P0.2 if the external oscillator circuit is enabled, and any selected ADC or Comparator inputs. The Crossbar skips selected pins as if they were already assigned, and moves to the next unassigned pin.

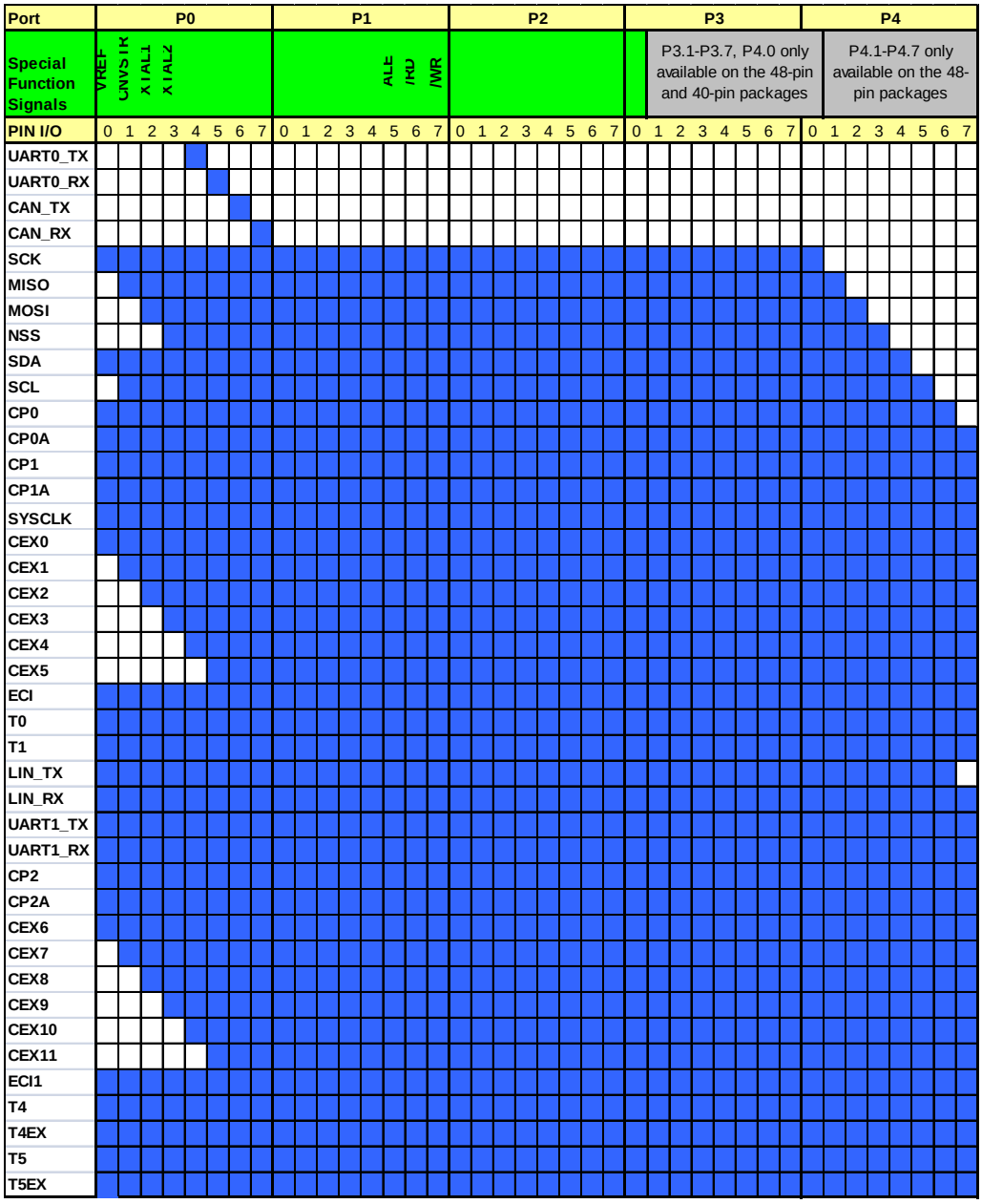

Figure 20.3. Peripheral Availability on Port I/O Pins

Registers XBR0, XBR1, XBR2, and XBR3 are used to assign the digital I/O resources to the physical I/O Port pins. Note that when the SMBus is selected, the Crossbar assigns both pins associated with the SMBus (SDA and SCL); and similarly when the UART, CAN or LIN are selected, the Crossbar assigns both pins associated with the peripheral (TX and RX).

UART0 pin assignments are fixed for bootloading purposes: UART TX0 is always assigned to P0.4; UART RX0 is always assigned to P0.5. CAN0 pin assignments are fixed to P0.6 for CAN_TX and P0.7 for CAN_RX. Standard Port I/Os appear contiguously after the prioritized functions have been assigned.

Important Note: The SPI can be operated in either 3-wire or 4-wire modes, pending the state of the NSSMD1–NSSMD0 bits in register SPI0CN. According to the SPI mode, the NSS signal may or may not be routed to a Port pin.

As an example configuration, if CAN0, SPI0 in 4-wire mode, and PCA0 Modules 0, 1, and 2, 6, and 7 are enabled on the crossbar with P0.1, P0.2, and P0.5 skipped, the registers should be set as follows: XBR0 = 0x06 (CAN0 and SPI0 enabled), XBR1 = 0x0C (PCA0 modules 0, 1, and 2 enabled), XBR2 = 0x40 (Crossbar enabled), XBR3 = 0x02 (PCA1 modules 6 and 7) and P0SKIP = 0x26 (P0.1, P0.2, and P0.5 skipped). The resulting crossbar would look as shown in Figure 20.4.

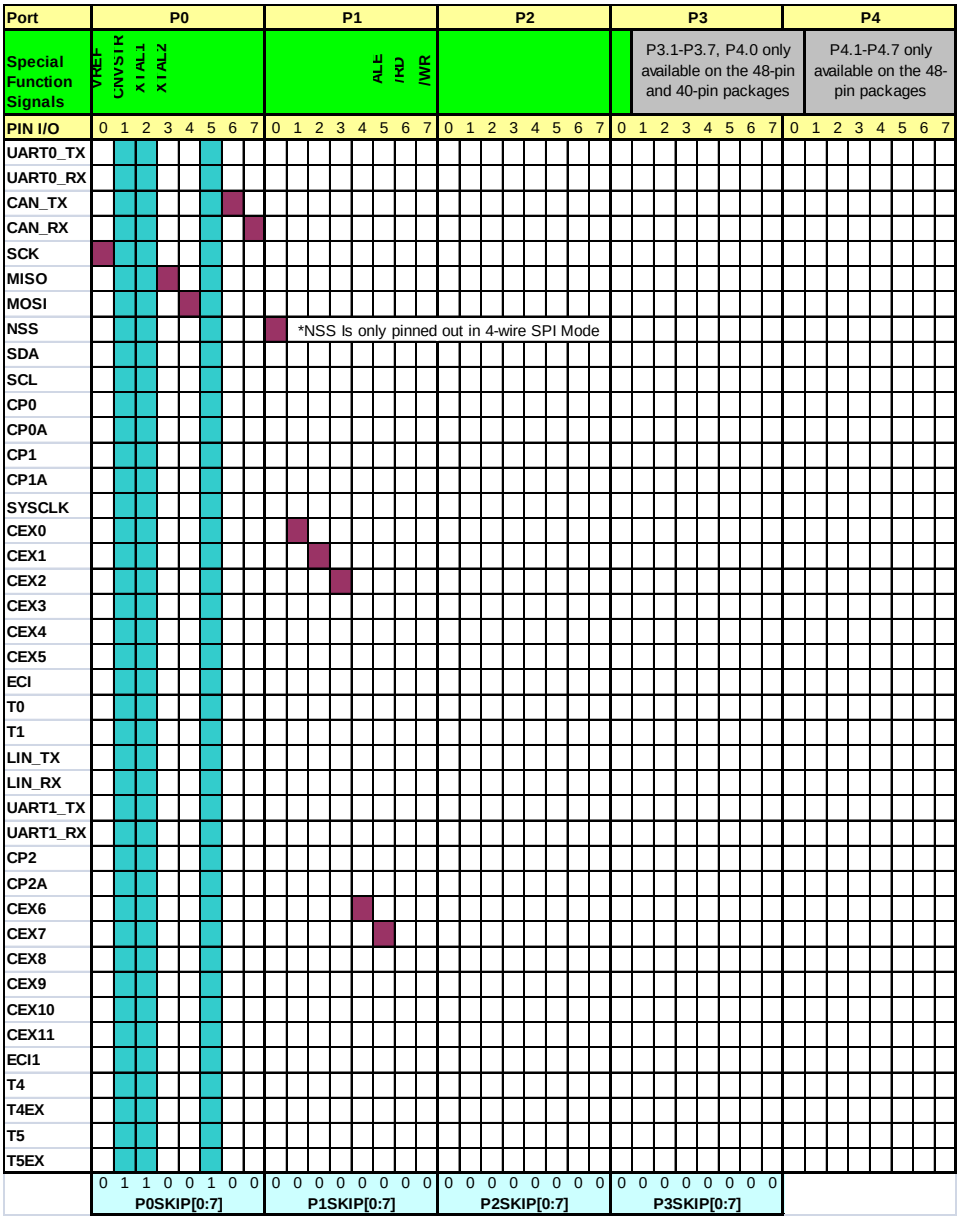

Figure 20.4. Crossbar Priority Decoder in Example Configuration

24. UART0

UART0 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates (details in Section “24.1. Baud Rate Generator” on page 256). A received data FIFO allows UART0 to receive up to three data bytes before data is lost and an overflow occurs.

UART0 has six associated SFRs. Three are used for the Baud Rate Generator (SBCON0, SBRLH0, and SBRLL0), two are used for data formatting, control, and status functions (SCON0, SMOD0), and one is used to send and receive data (SBUF0). The single SBUF0 location provides access to both transmit and receive registers. **Writes to SBUF0 always access the Transmit register. Reads of SBUF0 always access the buffered Receive register; it is not possible to read data from the Transmit register.**

With UART0 interrupts enabled, an interrupt is generated each time a transmit is completed (TI0 is set in SCON0), or a data byte has been received (RI0 is set in SCON0). The UART0 interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine. They must be cleared manually by software, allowing software to determine the cause of the UART0 interrupt (transmit complete or receive complete). If additional bytes are available in the Receive FIFO, the RI0 bit cannot be cleared by software.

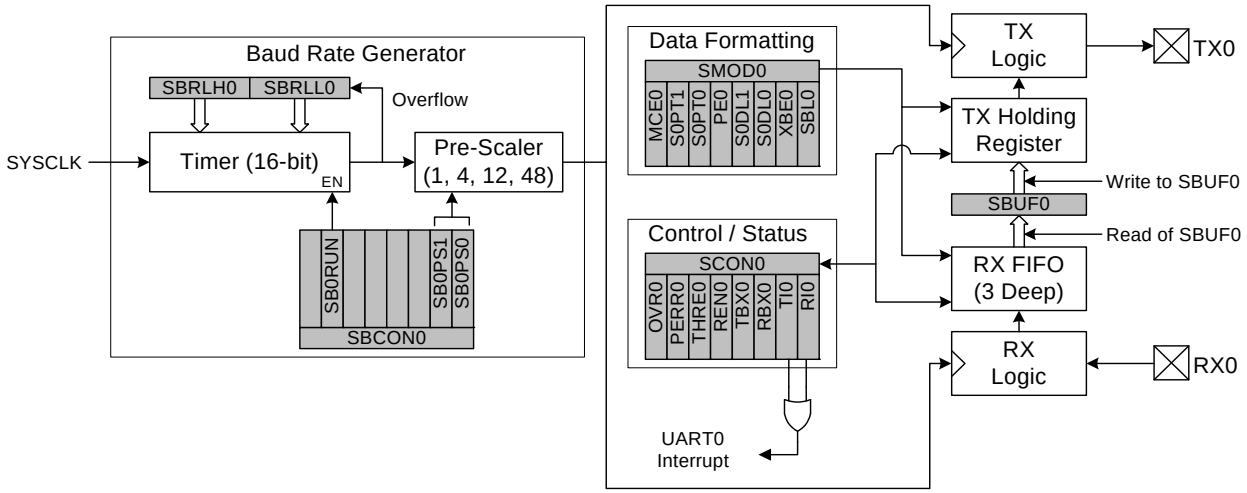

Figure 24.1. UART0 Block Diagram

24.1. Baud Rate Generator

The UART0 baud rate is generated by a dedicated 16-bit timer which runs from the controller’s core clock (SYSCLK) and has prescaler options of 1, 4, 12, or 48. The timer and prescaler options combined allow for a wide selection of baud rates over many clock frequencies.

The baud rate generator is configured using three registers: SBCON0, SBRLH0, and SBRLL0. The UART0 Baud Rate Generator Control Register (SBCON0, SFR Definition 24.4) enables or disables the baud rate generator, selects the clock source for the baud rate generator, and selects the prescaler value for the timer. The baud rate generator must be enabled for UART0 to function. Registers SBRLH0 and SBRLL0 contain a 16-bit reload value for the dedicated 16-bit timer. The internal timer counts up from the reload value on every clock tick. On timer overflows (0xFFFF to 0x0000), the timer is reloaded. The baud rate for UART0 is defined in Equation 24.1, where “BRG Clock” is the baud rate generator’s selected clock source. For reliable UART operation, it is recommended that the UART baud rate is not configured for baud rates faster than SYSCLK/16.

SFR Definition 27.8. TMR2CN: Timer 2 Control

Bit	7	6	5	4	3	2	1	0
Name	TF2H	TF2L	TF2LEN	TF2CEN	T2SPLIT	TR2		T2XCLK
Type	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC8; Bit-Addressable; SFR Page = 0x00

Bit	Name	Function
7	TF2H	**Timer 2 High Byte Overflow Flag.** Set by hardware when the Timer 2 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 2 overflows from 0xFFFF to 0x0000. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF2L	**Timer 2 Low Byte Overflow Flag.** Set by hardware when the Timer 2 low byte overflows from 0xFF to 0x00. TF2L will be set when the low byte overflows regardless of the Timer 2 mode. This bit is not automatically cleared by hardware.
5	TF2LEN	**Timer 2 Low Byte Interrupt Enable.** When set to 1, this bit enables Timer 2 Low Byte interrupts. If Timer 2 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 2 overflows.
4	TF2CEN	**Timer 2 Capture Mode Enable.** 0: Timer 2 Capture Mode is disabled. 1: Timer 2 Capture Mode is enabled.
3	T2SPLIT	**Timer 2 Split Mode Enable.** When this bit is set, Timer 2 operates as two 8-bit timers with auto-reload. 0: Timer 2 operates in 16-bit auto-reload mode. 1: Timer 2 operates as two 8-bit auto-reload timers.
2	TR2	**Timer 2 Run Control.** Timer 2 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR2H only; TMR2L is always enabled in split mode.
1	Unused	Read = 0b; Write = Don't Care
0	T2XCLK	**Timer 2 External Clock Select.** This bit selects the external clock source for Timer 2. If Timer 2 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 2 Clock Select bits (T2MH and T2ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 0: Timer 2 clock is the system clock divided by 12. 1: Timer 2 clock is the external clock divided by 8 (synchronized with SYSCLK).

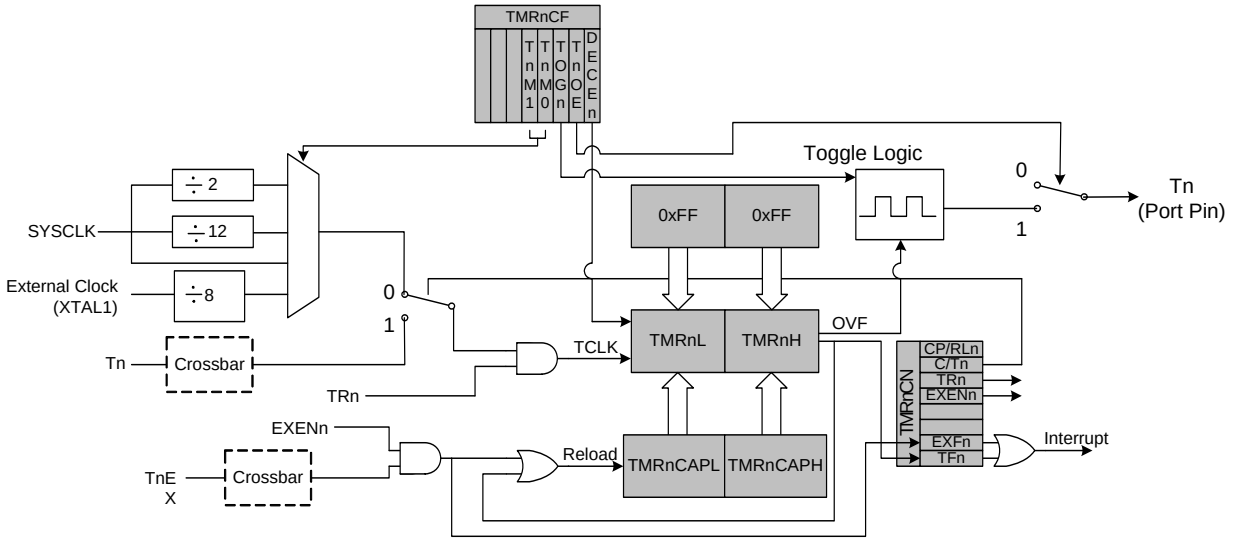

Figure 27.11. Timer 4 and 5 Auto Reload and Toggle Mode Block Diagram

27.4.4. Toggle Output Mode

Timers 4 and 5 have the capability to toggle the state of their respective output port pins (T4 or T5) to produce a 50% duty cycle waveform output. The port pin state will change upon the overflow or underflow of the respective timer (depending on whether the timer is counting *up* or *down*). The toggle frequency is determined by the clock source of the timer and the values loaded into TMRnCAPH and TMRnCAPL. When counting down, the auto-reload value for the timer is 0xFFFF, and underflow will occur when the value in the timer matches the value stored in TMRnCAPH:TMRCAPL. When counting up, the auto-reload value for the timer is TMRnCAPH:TMRCAPL, and overflow will occur when the value in the timer transitions from 0xFFFF to the reload value.

To output a square wave, the timer is placed in reload mode (the Capture/Reload Select Bit in TMRnCN and the Timer/Counter Select Bit in TMRnCN are cleared to 0). The timer output is enabled by setting the Timer Output Enable Bit in TMRnCF to 1. The timer should be configured via the timer clock source and reload/underflow values such that the timer overflow/underflows at 1/2 the desired output frequency. The port pin assigned by the crossbar as the timer's output pin should be configured as a digital output (see **Section "20. Port Input/Output" on page 188**). Setting the timer's Run Bit (TRn) to 1 will start the toggle of the pin. A Read/Write of the Timer's Toggle Output State Bit (TMRnCF.2) is used to read the state of the toggle output, or to force a value of the output. This is useful when it is desired to start the toggle of a pin in a known state, or to force the pin into a desired state when the toggle mode is halted.

$$F_{sq} = \frac{F_{TCLK}}{2 \times (65536 - TMRnCAP)}$$

Equation 27.1. Square Wave Frequency

SFR Definition 27.22. TMRnL: Timer 4 and 5 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMRnL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

TMR4L SFR Address = 0xCC; TMR5L SFR Address = 0x94; SFR Page = 0x10

Bit	Name	Function
7:0	TMRnL[7:0]	**Timer n Low Byte.** In 16-bit mode, the TMRnL register contains the low byte of the 16-bit Timer n. In 8-bit mode, TMRnL contains the 8-bit low byte timer value.

SFR Definition 27.23. TMRnH Timer 4 and 5 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMRnH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

TMR4H SFR Address = 0xCD; TMR5H SFR Address = 0x95; SFR Page = 0x10

Bit	Name	Function
7:0	TMRnH[7:0]	**Timer n High Byte.** In 16-bit mode, the TMRnH register contains the high byte of the 16-bit Timer n. In 8-bit mode, TMRnH contains the 8-bit high byte timer value.

29.3.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes PCA1 to capture the value of the PCA1 counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA1CPLn and PCA1CPHn). The CAPP1n and CAPN1n bits in the PCA1CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA1CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPP1n and CAPN1n bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.

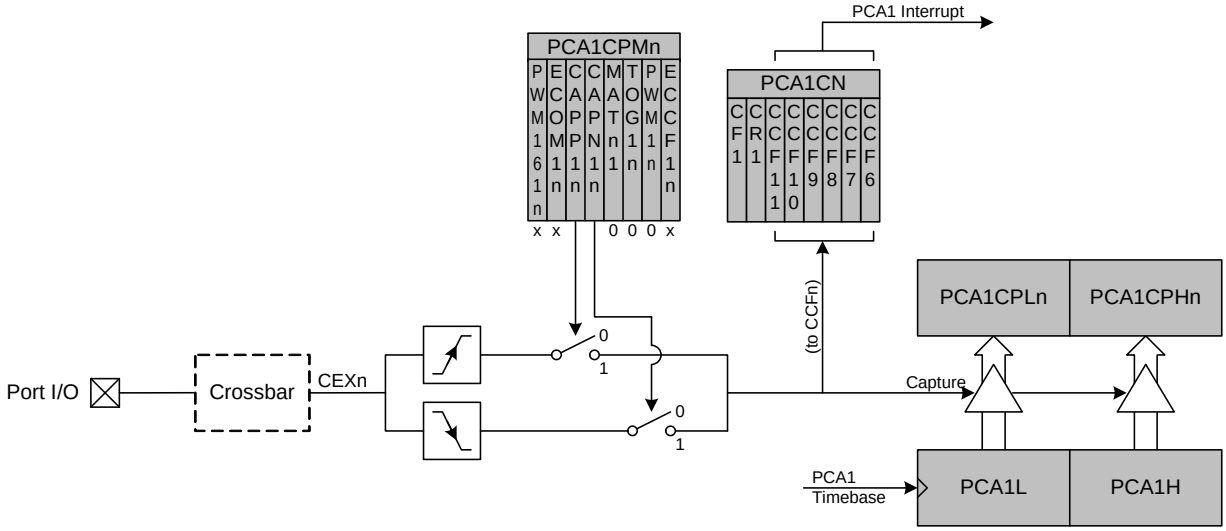

Figure 29.4. PCA1 Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.