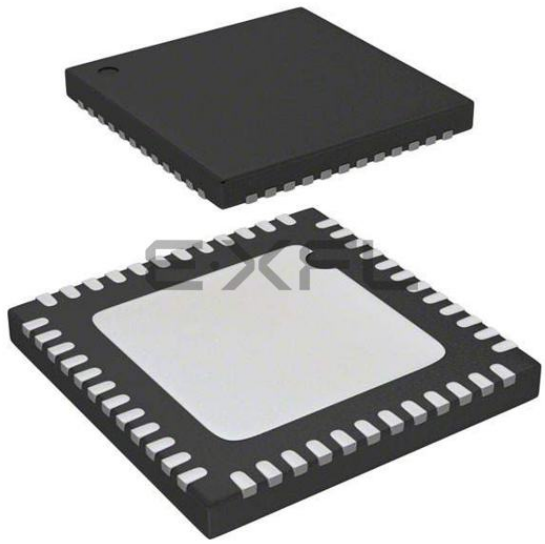

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f581-im

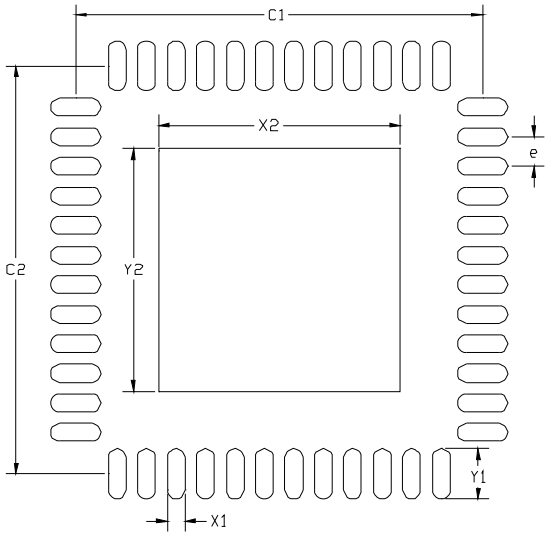

Figure 4.4. QFN-48 Landing Diagram

Table 4.4. QFN-48 Landing Diagram Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	6.80	6.90	X2	4.00	4.10
C2	6.80	6.90	Y1	0.75	0.85
e	0.50 BSC		Y2	4.00	4.10
X1	0.20	0.30			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimension and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-SM-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
9. A 3x3 array of 1.20 mm x 1.10mm openings on a 1.40 mm pitch should be used for the center pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

4.5. QFN-32 Package Specifications

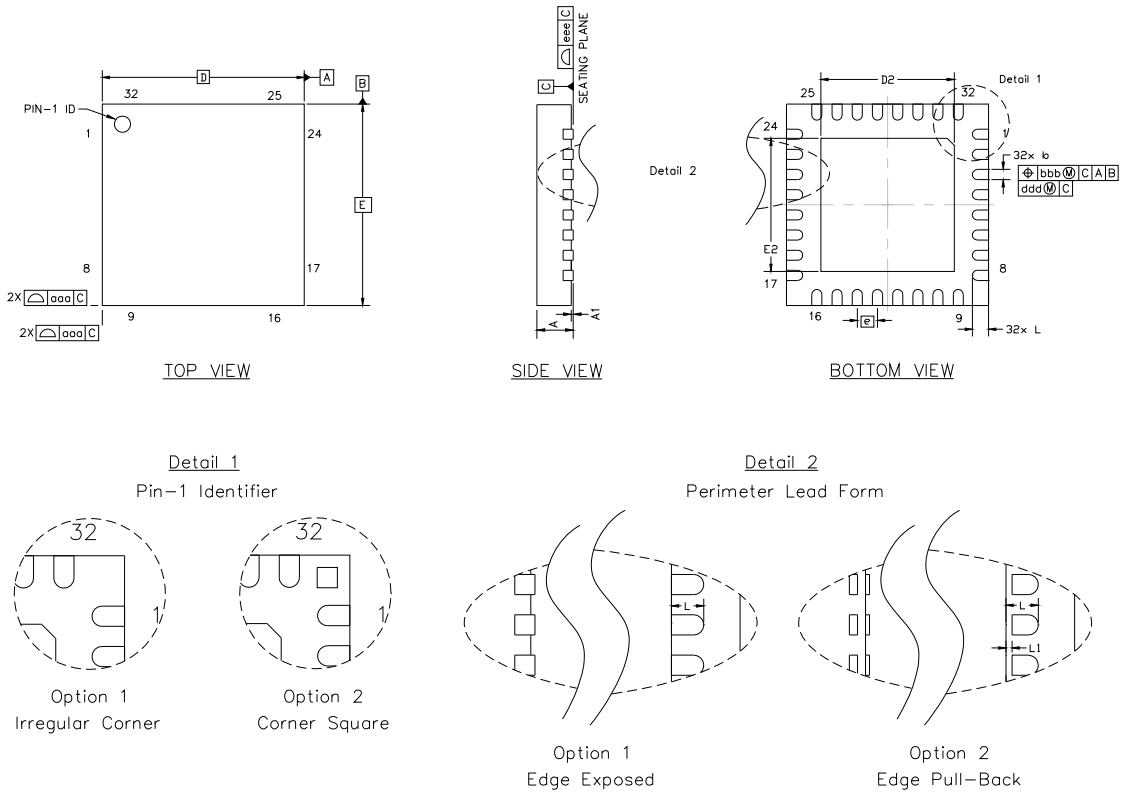

Figure 4.9. QFN-32 Package Drawing

Table 4.9. QFN-32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.9	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		5.00 BSC.	
D2	3.20	3.30	3.40
e		0.50 BSC.	
E		5.00 BSC.	

Dimension	Min	Typ	Max
E2	3.20	3.30	3.40
L	0.30	0.40	0.50
L1	0.00	—	0.15
aaa	—	—	0.15
bbb	—	—	0.15
ddd	—	—	0.05
eee	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VGGD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

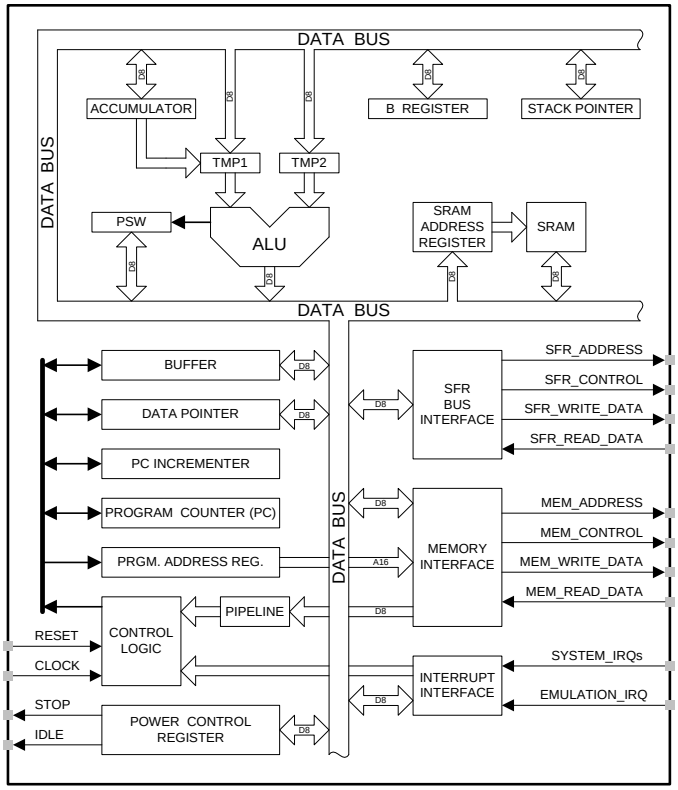

Figure 11.1. CIP-51 Block Diagram

With the CIP-51's maximum system clock at 50 MHz, it has a peak throughput of 50 MIPS. The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

Programming and Debugging Support

In-system programming of the Flash program memory and communication with on-chip debug support logic is accomplished via the Silicon Labs 2-Wire Development Interface (C2).

The on-chip debug support logic facilitates full speed in-circuit debugging, allowing the setting of hardware breakpoints, starting, stopping and single stepping through program execution (including interrupt service routines), examination of the program's call stack, and reading/writing the contents of registers and memory. This method of on-chip debugging is completely non-intrusive, requiring no RAM, Stack, timers, or other on-chip resources. C2 details can be found in “C2 Interface” on page 351.

The CIP-51 is supported by development tools from Silicon Labs and third party vendors. Silicon Labs provides an integrated development environment (IDE) including editor, debugger and programmer. The IDE's debugger and programmer interface to the CIP-51 via the C2 interface to provide fast and efficient in-system device programming and debugging. Third party macro assemblers and C compilers are also available.

Table 11.1. CIP-51 Instruction Set Summary (Prefetch-Enabled) (Continued)

Mnemonic	Description	Bytes	Clock Cycles
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement Carry	1	1
CPL bit	Complement direct bit	2	2
ANL C, bit	AND direct bit to Carry	2	2
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2
JC rel	Jump if Carry is set	2	2/(4-6)*
JNC rel	Jump if Carry is not set	2	2/(4-6)*
JB bit, rel	Jump if direct bit is set	3	3/(5-7)*
JNB bit, rel	Jump if direct bit is not set	3	3/(5-7)*
JBC bit, rel	Jump if direct bit is set and clear bit	3	3/(5-7)*
Program Branching			
ACALL addr11	Absolute subroutine call	2	4-6*
LCALL addr16	Long subroutine call	3	5-7*
RET	Return from subroutine	1	6-8*
RETI	Return from interrupt	1	6-8*
AJMP addr11	Absolute jump	2	4-6*
LJMP addr16	Long jump	3	5-7*
SJMP rel	Short jump (relative address)	2	4-6*
JMP @A+DPTR	Jump indirect relative to DPTR	1	3-5*
JZ rel	Jump if A equals zero	2	2/(4-6)*
JNZ rel	Jump if A does not equal zero	2	2/(4-6)*
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	4/(6-8)*
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/(6-8)*
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/(5-7)*
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/(6-8)*
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/(4-6)*
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/(5-7)*
NOP	No operation	1	1

Note: Certain instructions take a variable number of clock cycles to execute depending on instruction alignment and the FLRT setting (SFR Definition 15.3).

SFR Definition 13.4. SFRLAST: SFR Last

Bit	7	6	5	4	3	2	1	0
Name	SFRLAST[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA7; SFR Page = All Pages

Bit	Name	Function
7:0	SFRLAST[7:0]	**SFR Page Stack Bits.** This is the value that will go to the SFRNEXT register upon a return from interrupt. Write: Sets the SFR Page in the last entry of the SFR Stack. This will cause the SFRNEXT SFR to have this SFR page value upon a return from interrupt. Read: Returns the value of the SFR page contained in the last entry of the SFR stack. SFR page context is retained upon interrupts/return from interrupts in a 3 byte SFR Page Stack: SFRPAGE is the first entry, SFRNEXT is the second, and SFRLAST is the third entry. The SFR stack bytes may be used alter the context in the SFR Page Stack, and will not cause the stack to “push” or “pop”. Only interrupts and return from interrupts cause pushes and pops of the SFR Page Stack.

SFR Definition 15.2. FLKEY: Flash Lock and Key

Bit	7	6	5	4	3	2	1	0
Name	FLKEY[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB7; SFR Page = All Pages

Bit	Name	Function
7:0	FLKEY[7:0]	**Flash Lock and Key Register.** Write: This register provides a lock and key function for Flash erasures and writes. Flash writes and erases are enabled by writing 0xA5 followed by 0xF1 to the FLKEY register. Flash writes and erases are automatically disabled after the next write or erase is complete. If any writes to FLKEY are performed incorrectly, or if a Flash write or erase operation is attempted while these operations are disabled, the Flash will be permanently locked from writes or erasures until the next device reset. If an application never writes to Flash, it can intentionally lock the Flash by writing a non-0xA5 value to FLKEY from software. Read: When read, bits 1–0 indicate the current Flash lock state. 00: Flash is write/erase locked. 01: The first key code has been written (0xA5). 10: Flash is unlocked (writes/erases allowed). 11: Flash writes/erases disabled until the next reset.

Table 18.2. EMIF Pinout (C8051F588/9-F590/1)

Multiplexed Mode	
Signal Name	**Port Pin**
$\overline{RD}$	P1.6
$\overline{WR}$	P1.7
ALE	P1.5
D0/A0	P3.0
D1/A1	P3.1
D2/A2	P3.2
D3/A3	P3.3
D4/A4	P3.4
D5/A5	P3.5
D6/A6	P3.6
D7/A7	P3.7
A8	P2.0
A9	P2.1
A10	P2.2
A11	P2.3
A12	P2.4
A13	P2.5
A14	P2.6
A15	P2.7

SFR Definition 18.1. EMI0CN: External Memory Interface Control

Bit	7	6	5	4	3	2	1	0
Name	PGSEL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xAA; SFR Page = 0x00

Bit	Name	Function
7:0	PGSEL[7:0]	**XRAM Page Select Bits.** The XRAM Page Select Bits provide the high byte of the 16-bit external data memory address when using an 8-bit MOVX command, effectively selecting a 256-byte page of RAM. 0x00: 0x0000 to 0x00FF 0x01: 0x0100 to 0x01FF ... 0xFE: 0xFE00 to 0xFEFF 0xFF: 0xFF00 to 0xFFFF

19.2. Programmable Internal Oscillator

All C8051F58x/F59x devices include a programmable internal high-frequency oscillator that defaults as the system clock after a system reset. The internal oscillator period can be adjusted via the OSCICRS and OSCIFIN registers defined in SFR Definition 19.3 and SFR Definition 19.4. On C8051F58x/F59x devices, OSCICRS and OSCIFIN are factory calibrated to obtain a 24 MHz base frequency. Note that the system clock may be derived from the programmed internal oscillator divided by 1, 2, 4, 8, 16, 32, 64, or 128, as defined by the IFCN bits in register OSCICN. The divide value defaults to 128 following a reset.

19.2.1. Internal Oscillator Suspend Mode

When software writes a logic 1 to SUSPEND (OSCICN.5), the internal oscillator is suspended. If the system clock is derived from the internal oscillator, the input clock to the peripheral or CIP-51 will be stopped until one of the following events occur:

- Port 0 Match Event.
- Port 1 Match Event.
- Port 2 Match Event.
- Port 3 Match Event.
- Comparator 0 enabled and output is logic 0.

When one of the oscillator awakening events occur, the internal oscillator, CIP-51, and affected peripherals resume normal operation, regardless of whether the event also causes an interrupt. The CPU resumes execution at the instruction following the write to SUSPEND.

Note: When entering suspend mode, firmware must be the ZTCEN bit in REF0CN (SFR Definition 8.1).

UART0 pin assignments are fixed for bootloading purposes: UART TX0 is always assigned to P0.4; UART RX0 is always assigned to P0.5. CAN0 pin assignments are fixed to P0.6 for CAN_TX and P0.7 for CAN_RX. Standard Port I/Os appear contiguously after the prioritized functions have been assigned.

Important Note: The SPI can be operated in either 3-wire or 4-wire modes, pending the state of the NSSMD1–NSSMD0 bits in register SPI0CN. According to the SPI mode, the NSS signal may or may not be routed to a Port pin.

As an example configuration, if CAN0, SPI0 in 4-wire mode, and PCA0 Modules 0, 1, and 2, 6, and 7 are enabled on the crossbar with P0.1, P0.2, and P0.5 skipped, the registers should be set as follows: XBR0 = 0x06 (CAN0 and SPI0 enabled), XBR1 = 0x0C (PCA0 modules 0, 1, and 2 enabled), XBR2 = 0x40 (Crossbar enabled), XBR3 = 0x02 (PCA1 modules 6 and 7) and P0SKIP = 0x26 (P0.1, P0.2, and P0.5 skipped). The resulting crossbar would look as shown in Figure 20.4.

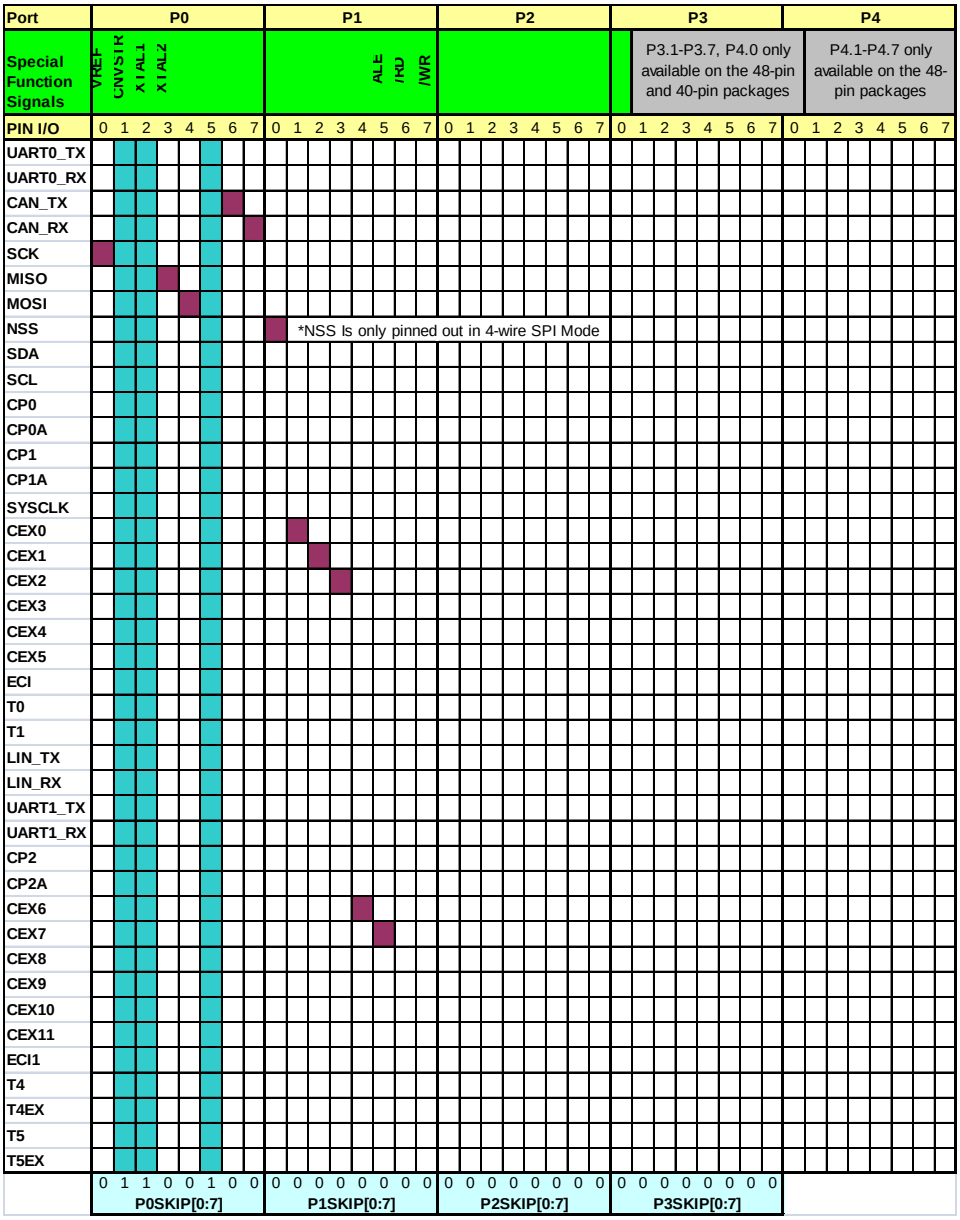

Figure 20.4. Crossbar Priority Decoder in Example Configuration

SFR Definition 20.30. P4MDOUT: Port 4 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P4MDOUT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xAF; SFR Page = 0x0F

Bit	Name	Function
7:0	P4MDOUT[7:0]	**Output Configuration Bits for P4.7–P4.0 (respectively).** 0: Corresponding P4.n Output is open-drain. 1: Corresponding P4.n Output is push-pull.

Note: Port 4.0 is only available on the 48-pin and 40-pin packages.; P4.1-P4.7 is only available on the 48-pin packages.

21.7. LIN Registers

The following Special Function Registers (SFRs) and indirect registers are available for the LIN controller.

21.7.1. LIN Direct Access SFR Registers Definitions

SFR Definition 21.1. LIN0ADR: LIN0 Indirect Address Register

Bit	7	6	5	4	3	2	1	0
Name	LIN0ADR[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD3; SFR Page = 0x00

Bit	Name	Function
7:0	LIN0ADR[7:0]	**LIN Indirect Address Register Bits.** This register hold an 8-bit address used to indirectly access the LIN0 core registers. Table 21.4 lists the LIN0 core registers and their indirect addresses. Reads and writes to LIN0DAT will target the register indicated by the LIN0ADR bits.

SFR Definition 21.2. LIN0DAT: LIN0 Indirect Data Register

Bit	7	6	5	4	3	2	1	0
Name	LIN0DAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD2; SFR Page = 0x00

Bit	Name	Function
7:0	LIN0DAT[7:0]	**LIN Indirect Data Register Bits.** When this register is read, it will read the contents of the LIN0 core register pointed to by LIN0ADR. When this register is written, it will write the value to the LIN0 core register pointed to by LIN0ADR.

LIN Register Definition 21.11. LIN0ID: LIN0 Identifier Register

Bit	7	6	5	4	3	2	1	0
Name			ID[5:0]					
Type	R	R	R/W					
Reset	0	0	0	0	0	0	0	0

Indirect Address = 0x0E

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don't Care.
5:0	ID[5:0]	**LIN Identifier Bits.** These bits form the data identifier. If the LINSIZE bits (LIN0SIZE[3:0]) are 1111b, bits ID[5:4] are used to determine the data size and are interpreted as follows: 00: 2 bytes 01: 2 bytes 10: 4 bytes 11: 8 bytes

The CAN controller clock must be less than or equal to 25 MHz. If the CIP-51 system clock is above 25 MHz, the divider in the CAN0CFG register must be set to divide the CAN controller clock down to an appropriate speed.

22.1.2. CAN Register Access

The CAN controller clock divider selected in the CAN0CFG SFR affects how the CAN registers can be accessed. If the divider is set to 1, then a CAN SFR can immediately be read after it is written. If the divider is set to a value other than 1, then a read of a CAN SFR that has just been written must be delayed by a certain number of cycles. This delay can be performed using a NOP or some other instruction that does not attempt to read the register. This access limitation applies to read and read-modify-write instructions that occur immediately after a write. The full list of affected instructions is ANL, ORL, MOV, XCH, and XRL.

For example, with the CAN0CFG divider set to 1, the CAN0CN SFR can be accessed as follows:

```
MOV CAN0CN, #041          ; Enable access to Bit Timing Register
MOV R7, CAN0CN            ; Copy CAN0CN to R7
```

With the CAN0CFG divider set to /2, the same example code requires an additional NOP:

```
MOV CAN0CN, #041          ; Enable access to Bit Timing Register
NOP                       ; Wait for write to complete
MOV R7, CAN0CN            ; Copy CAN0CN to R7
```

The number of delay cycles required is dependent on the divider setting. With a divider of 2, the read must wait for 1 system clock cycle. With a divider of 4, the read must wait 3 system clock cycles, and with the divider set to 8, the read must wait 7 system clock cycles. The delay only needs to be applied when reading the same register that was written. The application can write and read other CAN SFRs without any delay.

22.1.3. Example Timing Calculation for 1 Mbit/Sec Communication

This example shows how to configure the CAN controller timing parameters for a 1 Mbit/Sec bit rate. Table 18.1 shows timing-related system parameters needed for the calculation.

Table 22.1. Background System Information

Parameter	Value	Description
CIP-51 system clock (SYSCLK)	24 MHz	Internal Oscillator Max
CAN controller clock (f_{sys})	24 MHz	CAN0CFG divider set to 1
CAN clock period (t_{sys})	41.667 ns	Derived from $1/f_{sys}$
CAN time quantum (t_q)	41.667 ns	Derived from t_{sys} x BRP[1,2]
CAN bus length	10 m	5 ns/m signal delay between CAN nodes
Propogation delay time[3]	400 ns	2 x (transceiver loop delay + bus line delay)

Notes:
1. The CAN time quantum is the smallest unit of time recognized by the CAN controller. Bit timing parameters are specified in integer multiples of the time quantum.
2. The Baud Rate Prescaler (BRP) is defined as the value of the BRP Extension Register plus 1. The BRP extension register has a reset value of 0x0000. The BRP has a reset value of 1.
3. Based on an ISO-11898 compliant transceiver. CAN does not specify a physical layer.

Each bit transmitted on a CAN network has 4 segments (Sync_Seg, Prop_Seg, Phase_Seg1, and Phase_Seg2), as shown in Figure 18.3. The sum of these segments determines the CAN bit time (1/bit rate). In this example, the desired bit rate is 1 Mbit/sec; therefore, the desired bit time is 1000 ns.

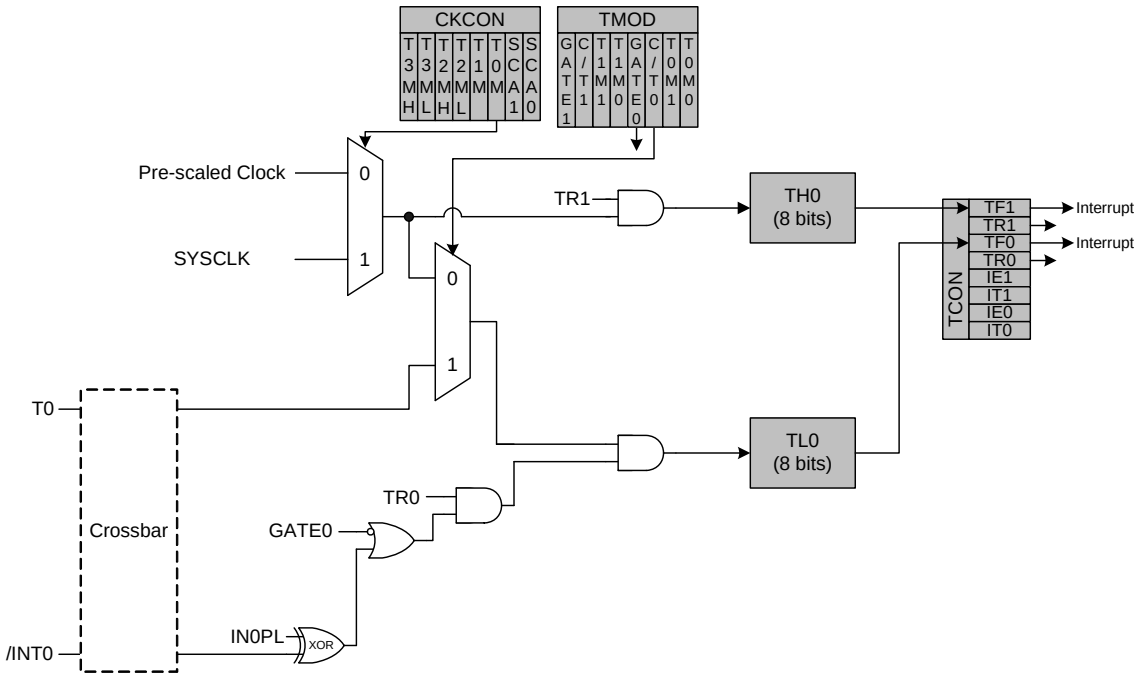

Figure 27.3. T0 Mode 3 Block Diagram

SFR Definition 27.6. TH0: Timer 0 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8C; SFR Page = All Pages

Bit	Name	Function
7:0	TH0[7:0]	**Timer 0 High Byte.** The TH0 register is the high byte of the 16-bit Timer 0.

SFR Definition 27.7. TH1: Timer 1 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8D; SFR Page = All Pages

Bit	Name	Function
7:0	TH1[7:0]	**Timer 1 High Byte.** The TH1 register is the high byte of the 16-bit Timer 1.

SFR Definition 27.9. TMR2RLL: Timer 2 Reload Register Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2RLL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCA; SFR Page = 0x00

Bit	Name	Function
7:0	TMR2RLL[7:0]	**Timer 2 Reload Register Low Byte.** TMR2RLL holds the low byte of the reload value for Timer 2.

SFR Definition 27.10. TMR2RLH: Timer 2 Reload Register High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2RLH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCB; SFR Page = 0x00

Bit	Name	Function
7:0	TMR2RLH[7:0]	**Timer 2 Reload Register High Byte.** TMR2RLH holds the high byte of the reload value for Timer 2.

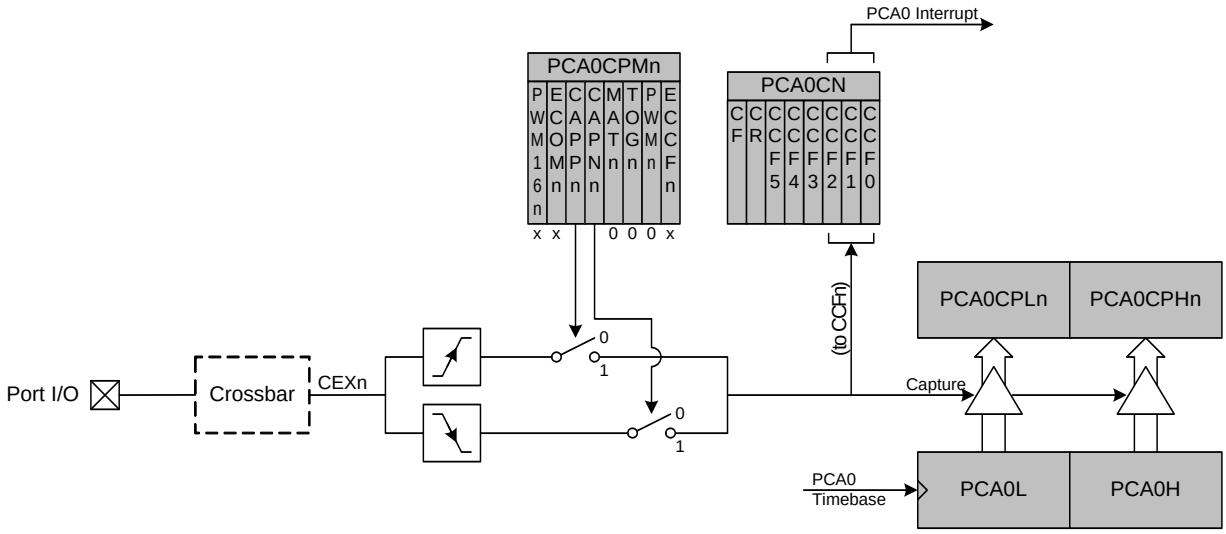

Figure 28.4. PCA0 Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.

28.3.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA0 counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

SFR Definition 28.5. PCA0L: PCA0 Counter/Timer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF9; SFR Page = 0x00

Bit	Name	Function
7:0	PCA0[7:0]	**PCA0 Counter/Timer Low Byte.** The PCA0L register holds the low byte (LSB) of the 16-bit PCA0 Counter/Timer.
Note: When the WDTE bit is set to 1, the PCA0L register cannot be modified by software. To change the contents of the PCA0L register, the Watchdog Timer must first be disabled.		

SFR Definition 28.6. PCA0H: PCA0 Counter/Timer High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xFA; SFR Page = 0x00

Bit	Name	Function
7:0	PCA0[15:8]	**PCA0 Counter/Timer High Byte.** The PCA0H register holds the high byte (MSB) of the 16-bit PCA0 Counter/Timer. Reads of this register will read the contents of a “snapshot” register, whose contents are updated only when the contents of PCA0L are read (see Section 28.1).
Note: When the WDTE bit is set to 1, the PCA0H register cannot be modified by software. To change the contents of the PCA0H register, the Watchdog Timer must first be disabled.		

SFR Definition 29.4. PCA1CPMn: PCA1 Capture/Compare Mode

Bit	7	6	5	4	3	2	1	0
Name	PWM161n	ECOM1n	CAPP1n	CAPN1n	MAT1n	TOG1n	PWM1n	ECCF1n
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: PCA1CPM6 = 0xDA, PCA1CPM7 = 0xDB, PCA1CPM8 = 0xDC; PCA1CPM9 = 0xDD, PCA1CPM10 = 0xDE, PCA1CPM11 = 0xDF, SFR Page (all registers) = 0x10

Bit	Name	Function
7	PWM161n	**16-bit Pulse Width Modulation Enable.** This bit enables 16-bit mode when Pulse Width Modulation mode is enabled. 0: 8 to 11-bit PWM selected. 1: 16-bit PWM selected.
6	ECOM1n	**Comparator Function Enable.** This bit enables the comparator function for PCA1 module n when set to 1.
5	CAPP1n	**Capture Positive Function Enable.** This bit enables the positive edge capture for PCA1 module n when set to 1.
4	CAPN1n	**Capture Negative Function Enable.** This bit enables the negative edge capture for PCA1 module n when set to 1.
3	MAT1n	**Match Function Enable.** This bit enables the match function for PCA1 module n when set to 1. When enabled, matches of the PCA1 counter with a module's capture/compare register cause the CCFn bit in PCA1MD register to be set to logic 1.
2	TOG1n	**Toggle Function Enable.** This bit enables the toggle function for PCA1 module n when set to 1. When enabled, matches of the PCA1 counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode.
1	PWM1n	**Pulse Width Modulation Mode Enable.** This bit enables the PWM function for PCA1 module n when set to 1. When enabled, a pulse width modulated signal is output on the CEXn pin. 8 to 11-bit PWM is used if PWM16n is cleared; 16-bit mode is used if PWM16n is set to logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0	ECCF1n	**Capture/Compare Flag Interrupt Enable.** This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt. 0: Disable CCFn interrupts. 1: Enable a Capture/Compare Flag interrupt request when CCFn is set.