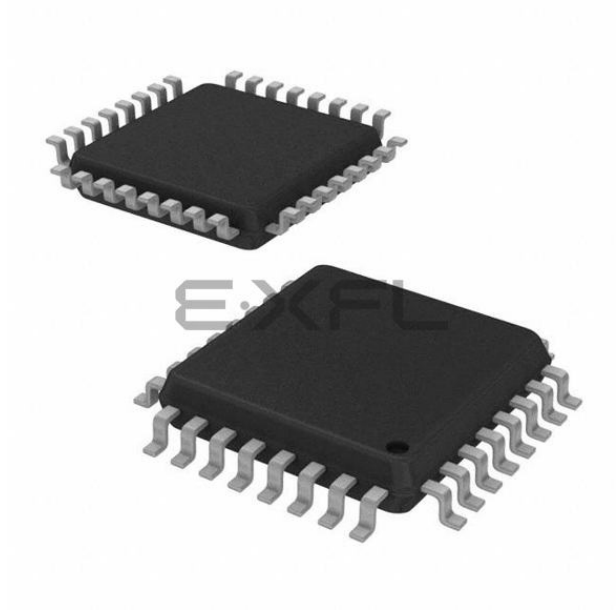

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), CANbus, LINbus, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 25x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f582-iq

List of Registers

2. Ordering Information

The following features are common to all devices in this family:

- 50 MHz system clock and 50 MIPS throughput (peak)
- 8448 bytes of RAM (256 internal bytes and 8192 XRAM bytes
- SMBus/I^2C, Enhanced SPI, Two UARTs
- Six Timers
- 12 Programmable Counter Array channels
- 12-bit, 200 ksps ADC
- Internal 24 MHz oscillator
- Internal Voltage Regulator
- Internal Voltage Reference and Temperature Sensor
- Three Analog Comparators

Table 2.1 shows the feature that differentiate the devices in this family.

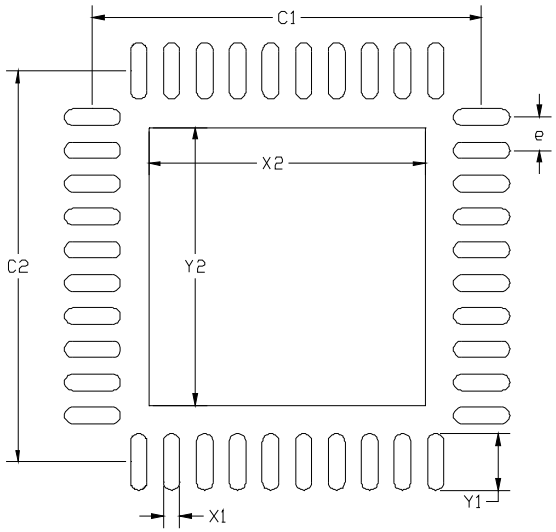

Figure 4.6. QFN-40 Landing Diagram

Table 4.6. QFN-40 Landing Diagram Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	5.80	5.90	X2	4.10	4.20
C2	5.80	5.90	Y1	0.75	0.85
e	0.50 BSC		Y2	4.10	4.20
X1	0.15	0.25			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimension and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-SM-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
9. A 4x4 array of 0.80 mm square openings on a 1.05 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Post-Tracking Mode is selected when AD0TM is set to 01b. A programmable tracking time based on AD0TK is started immediately following the convert start signal. Conversions are started after the programmed tracking time ends. After a conversion is complete, ADC0 does not track the input. Rather, the sampling capacitor remains disconnected from the input making the input pin high-impedance until the next convert start signal.

Dual-Tracking Mode is selected when AD0TM is set to 11b. A programmable tracking time based on AD0TK is started immediately following the convert start signal. Conversions are started after the programmed tracking time ends. After a conversion is complete, ADC0 tracks continuously until the next conversion is started.

Depending on the output connected to the ADC input, additional tracking time, more than is specified in Table 5.10, may be required after changing MUX settings. See the settling time requirements described in Section “6.2.1. Settling Time Requirements” on page 59.

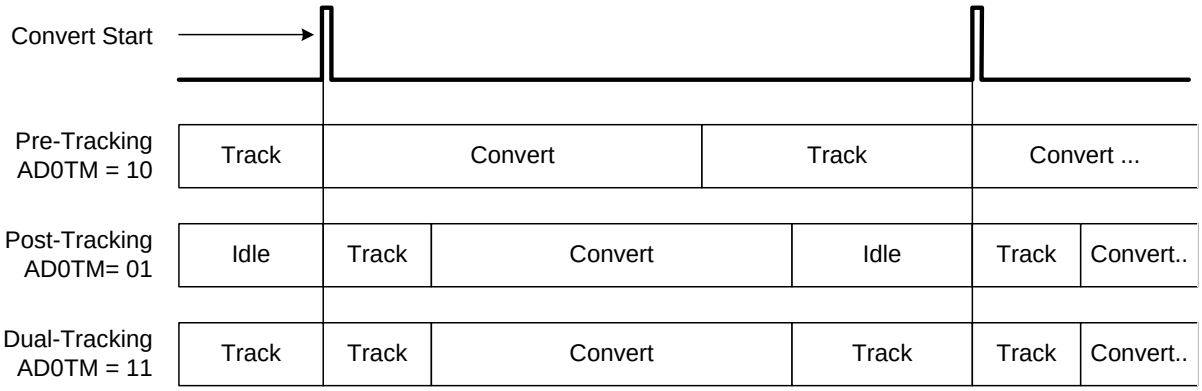

Figure 6.2. ADC0 Tracking Modes

6.1.3. Timing

ADC0 has a maximum conversion speed specified in Table 5.10. ADC0 is clocked from the ADC0 Subsystem Clock (FCLK). The source of FCLK is selected based on the BURSTEN bit. When BURSTEN is logic 0, FCLK is derived from the current system clock. When BURSTEN is logic 1, FCLK is derived from the Burst Mode Oscillator, an independent clock source with a maximum frequency of 25 MHz.

When ADC0 is performing a conversion, it requires a clock source that is typically slower than FCLK. The ADC0 SAR conversion clock (SAR clock) is a divided version of FCLK. The divide ratio can be configured using the AD0SC bits in the ADC0CF register. The maximum SAR clock frequency is listed in Table 5.10.

ADC0 can be in one of three states at any given time: tracking, converting, or idle. Tracking time depends on the tracking mode selected. For Pre-Tracking Mode, tracking is managed by software and ADC0 starts conversions immediately following the convert start signal. For Post-Tracking and Dual-Tracking Modes, the tracking time after the convert start signal is equal to the value determined by the AD0TK bits plus 2 FCLK cycles. Tracking is immediately followed by a conversion. The ADC0 conversion time is always 13 SAR clock cycles plus an additional 2 FCLK cycles to start and complete a conversion. Figure 6.4 shows timing diagrams for a conversion in Pre-Tracking Mode and tracking plus conversion in Post-Tracking or Dual-Tracking Mode. In this example, repeat count is set to one.

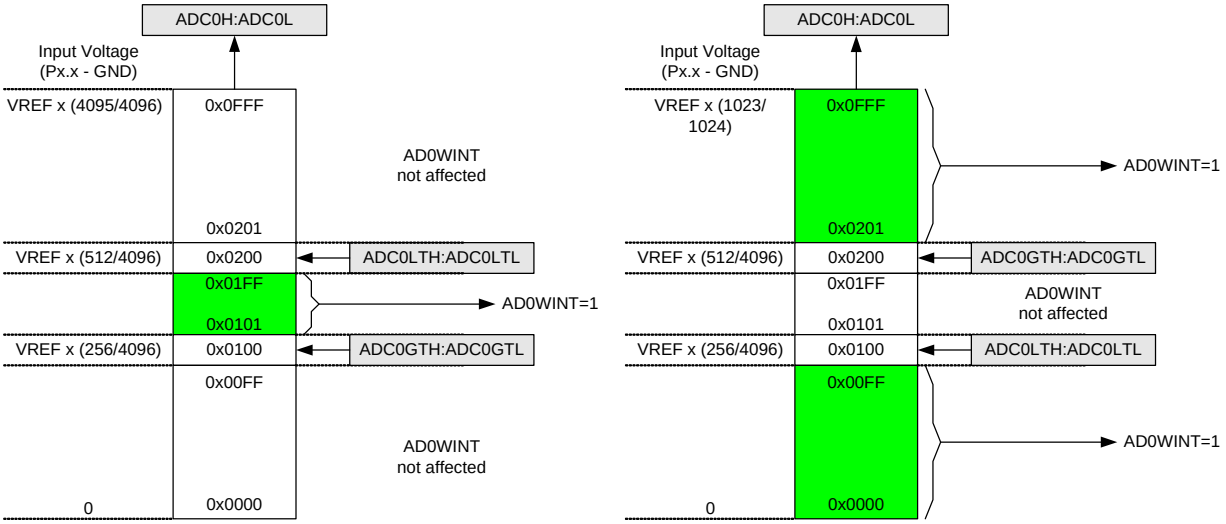

Figure 6.6. ADC Window Compare Example: Right-Justified Data

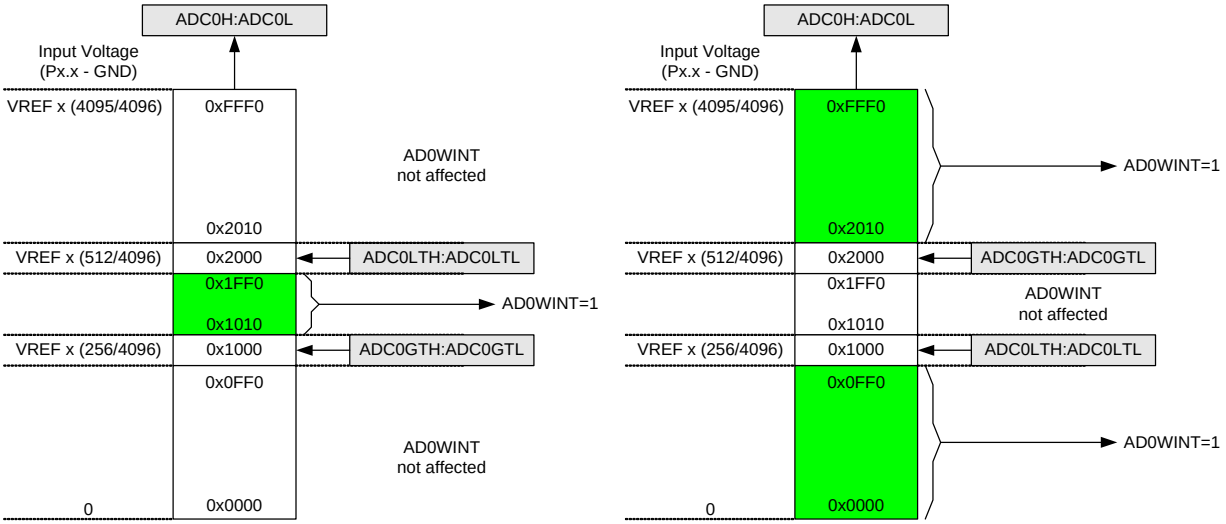

Figure 6.7. ADC Window Compare Example: Left-Justified Data

SFR Definition 6.13. ADC0MX: ADC0 Channel Select

Bit	7	6	5	4	3	2	1	0
Name			ADC0MX[5:0]					
Type	R	R	R/W					
Reset	0	0	1	1	1	1	1	1

SFR Address = 0xBB; SFR Page = 0x00;

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don't Care.
5:0	AMX0P[5:0]	**AMUX0 Positive Input Selection.** 000000: P0.0 000001: P0.1 000010: P0.2 000011: P0.3 000100: P0.4 000101: P0.5 000110: P0.6 000111: P0.7 001000: P1.0 001001: P1.1 001010: P1.2 001011: P1.3 001100: P1.4 001101: P1.5 001110: P1.6 001111: P1.7 010000: P2.0 010001: P2.1 010010: P2.2 010011: P2.3 010100: P2.4 010101: P2.5 010110: P2.6 010111: P2.7 011000: P3.0 011001: P3.1 (Available on 48-pin and 40-pin package devices) 011010: P3.2 (Available on 48-pin and 40-pin package devices) 011011: P3.3 (Available on 48-pin and 40-pin package devices) 011100: P3.4 (Available on 48-pin and 40-pin package devices) 011101: P3.5 (Available on 48-pin and 40-pin package devices) 011110: P3.6 (Available on 48-pin and 40-pin package devices) 011111: P3.7 (Available on 48-pin and 40-pin package devices) 100000–101111: Reserved 110000: Temp Sensor 110001: V_{DD} 110010–111111: GND

15. Flash Memory

On-chip, re-programmable Flash memory is included for program code and non-volatile data storage. The Flash memory can be programmed in-system, a single byte at a time, through the C2 interface or by software using the MOVX instruction. Once cleared to logic 0, a Flash bit must be erased to set it back to logic 1. Flash bytes would typically be erased (set to 0xFF) before being reprogrammed. The write and erase operations are automatically timed by hardware for proper execution; data polling to determine the end of the write/erase operation is not required. Code execution is stalled during a Flash write/erase operation. Refer to Table 5.5 for complete Flash memory electrical characteristics.

15.1. Programming The Flash Memory

The simplest means of programming the Flash memory is through the C2 interface using programming tools provided by Silicon Labs or a third party vendor. This is the only means for programming a non-initialized device. For details on the C2 commands to program Flash memory, see Section “30. C2 Interface” on page 351.

The on-chip V_{DD} Monitor must be enabled and set to the high threshold when executing code that writes and/or erases Flash memory from software. Systems that reprogram the Flash memory from software must use an external supply monitor and reprogram the high monitor threshold to ensure no issues with the uncalibrated internal regulator. See Section 15.4 for more details. Before performing any Flash write or erase procedure, set the FLEWT bit in Flash Scale register (FLSCL) to 1. Also, note that 8-bit MOVX instructions cannot be used to erase or write to Flash memory at addresses higher than 0x00FF.

For –I (Industrial Grade) parts, parts programmed at a cold temperature below 0 °C may exhibit weakly programmed flash memory bits. If programmed at 0 °C or higher, there is no problem reading Flash across the entire temperature range of -40 °C to 125 °C. This temperature restriction does not apply to –A (Automotive Grade) devices.

15.1.1. Reprogramming the VDD Monitor High Threshold

The output of the internal voltage regulator is calibrated by the MCU immediately after any reset event. The output of the un-calibrated internal regulator could be below the high threshold setting of the VDD Monitor. If this is the case and the MCU receives a non-power on reset (POR) when the VDD Monitor is set to the high threshold setting, the MCU will remain in reset until a POR occurs (i.e. V_{DD} Monitor will keep the device in reset). A POR will force the VDD Monitor to the low threshold setting, which is guaranteed to be below the un-calibrated output of the internal regulator. The device will then exit reset and resume normal operation. It is for this reason Silicon Labs strongly recommends that the VDD Monitor is always left in the low threshold setting (i.e. default value upon POR). When programming the Flash in-system, the VDD Monitor must be set to the high threshold setting.

To prevent this issue from happening and ensure the highest system reliability, firmware can change the VDD Monitor high threshold, and the system can use an external supply monitor that meets the Flash VDD requirement listed in Table 5.5 on page 48. To change the V_{DD} Monitor high threshold, perform the following steps:

1. Disable interrupts.
2. Write 0x01 to the SFRPAGE register.
3. Copy the value from SFR address 0x93 to SFR address 0x94.
4. Return the SFRPAGE register to its previous value.

17.1. Power-On Reset

During power-up, the device is held in a reset state and the $\overline{\text{RST}}$ pin is driven low until V_{DD} settles above V_{RST}. A delay occurs before the device is released from reset; the delay decreases as the V_{DD} ramp time increases (V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST}). Figure 17.2. plots the power-on and V_{DD} monitor reset timing. The maximum V_{DD} ramp time is 1 ms; slower ramp times may cause the device to be released from reset before V_{DD} reaches the V_{RST} level. For ramp times less than 1 ms, the power-on reset delay ($T_{PORDelay}$) is typically less than 0.3 ms.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000) software can read the PORSF flag to determine if a power-up was the cause of reset. The content of internal data memory should be assumed to be undefined after a power-on reset. The V_{DD} monitor is enabled following a power-on reset.

Note: For devices with a date code before year 2011, work week 24 (1124), if the /RST pin is held low for more than 1 second while power is applied to the device, and then /RST is released, a percentage of devices may lock up and fail to execute code. Toggling the /RST pin does not clear the condition. The condition is cleared by cycling power. Most devices that are affected will show the lock up behavior only within a narrow range of temperatures (a 5 to 10 °C window). Parts with a date code of year 2011, work week 24 (1124) or later do not have any restrictions on /RST low time. The date code is included in the bottom-most line of the package top side marking. The date code is a four-digit number with the format YYWW, where YY is the two-digit calendar year and WW is the two digit work week.

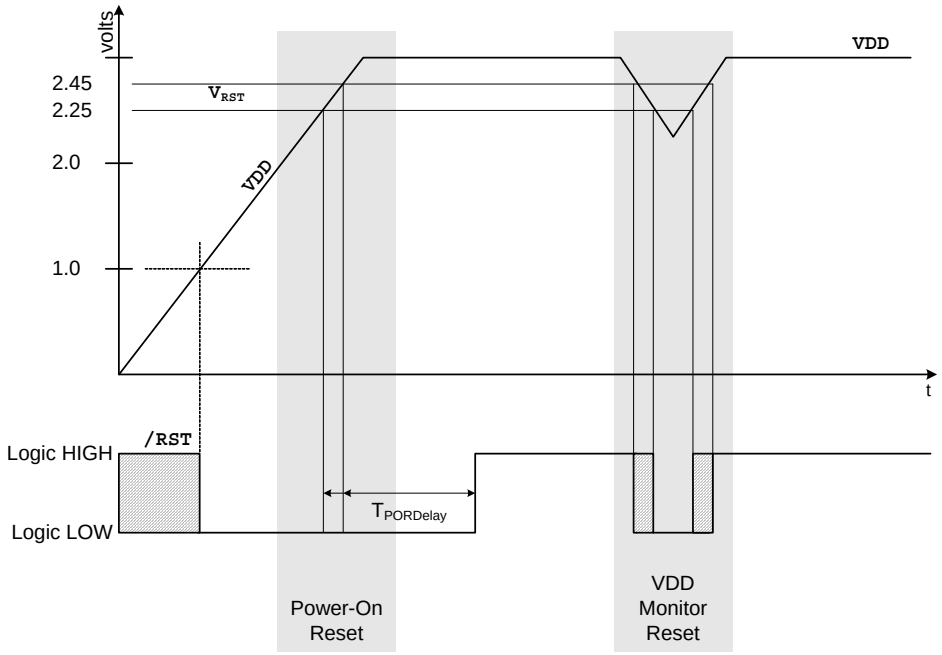

Figure 17.2. Power-On and V_{DD} Monitor Reset Timing

18.6.1.3. 8-bit MOVX with Bank Select: EMI0CF[4:2] = 110

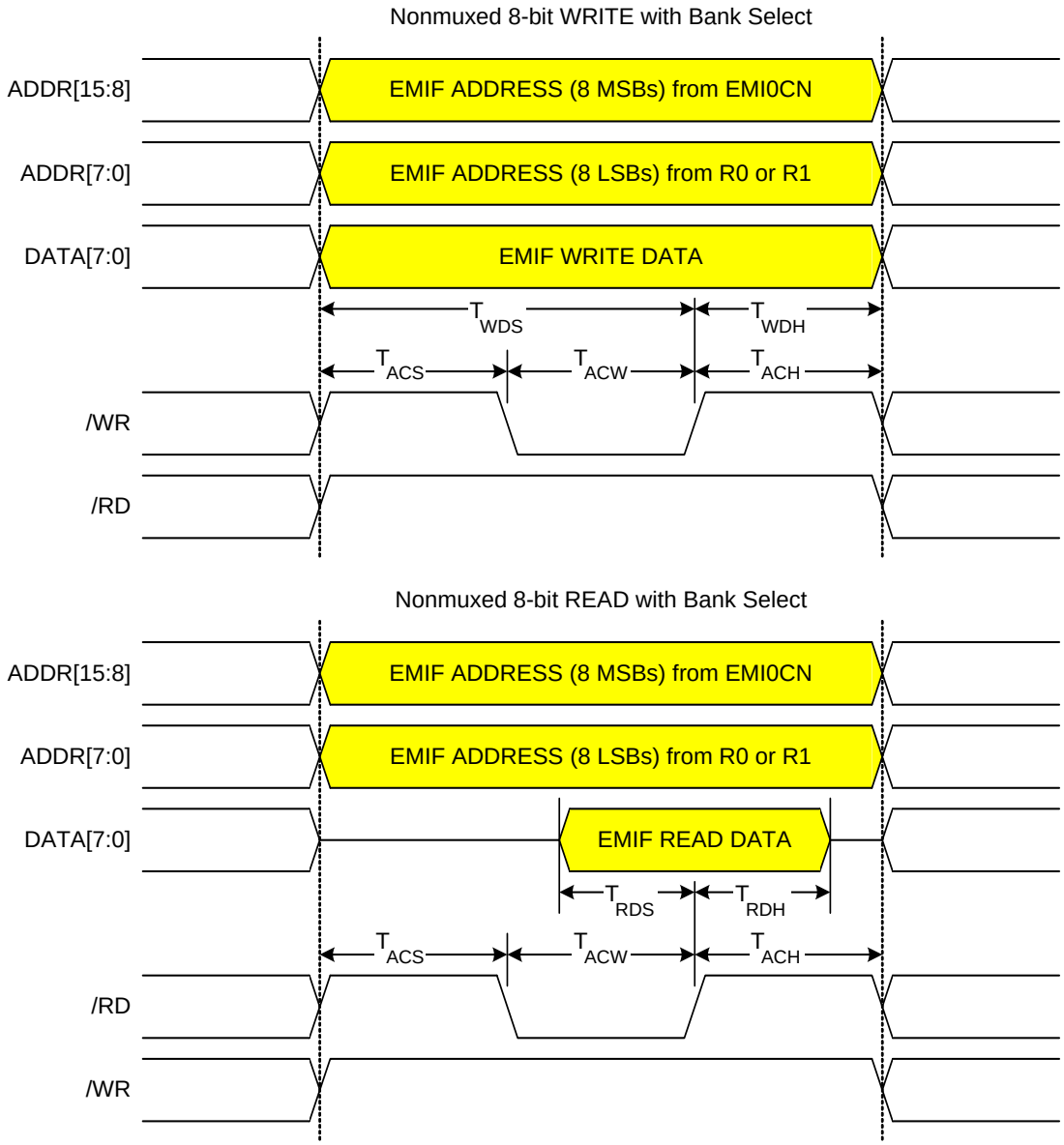

Figure 18.6. Non-multiplexed 8-bit MOVX with Bank Select Timing

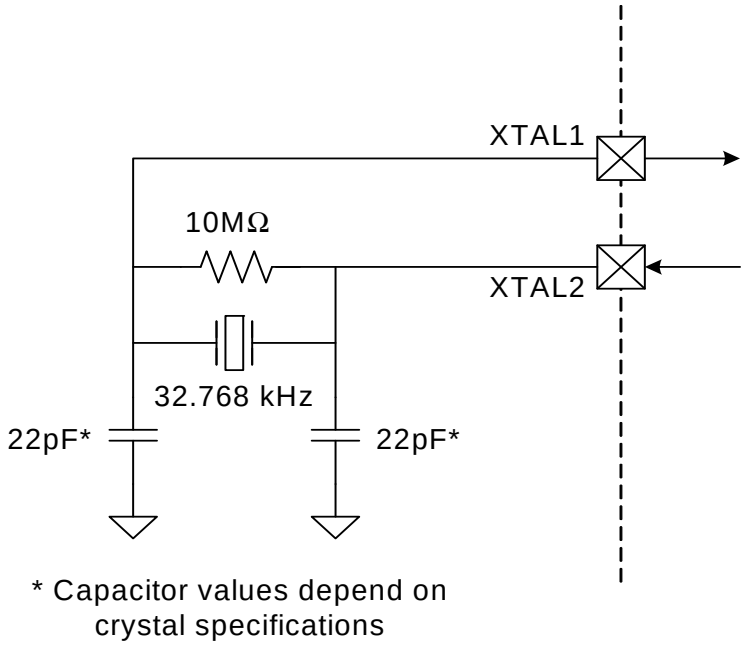

Figure 19.3. External 32.768 kHz Quartz Crystal Oscillator Connection Diagram

19.4.2. External RC Example

If an RC network is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 19.1, Option 2. The capacitor should be no greater than 100 pF; however for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, first select the RC network value to produce the desired frequency of oscillation, according to Equation , where f = the frequency of oscillation in MHz, C = the capacitor value in pF, and R = the pull-up resistor value in kΩ.

$$f = 1.23 \times 10^3 / (R \times C)$$

Equation 19.1. RC Mode Oscillator Frequency

For example: If the frequency desired is 100 kHz, let R = 246 kΩ and C = 50 pF:

f = 1.23(10^3)/RC = 1.23(10^3)/[246 x 50] = 0.1 MHz = 100 kHz

Referring to the table in SFR Definition 19.6, the required XFCN setting is 010b.

19.4.3. External Capacitor Example

If a capacitor is used as an external oscillator for the MCU, the circuit should be configured as shown in Figure 19.1, Option 3. The capacitor should be no greater than 100 pF; however for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, select the capacitor to be used and find the frequency of oscillation according to Equation , where f = the frequency of oscillation in MHz, C = the capacitor value in pF, and V_{DD} = the MCU power supply in volts.

SFR Definition 20.2. XBR1: Port I/O Crossbar Register 1

Bit	7	6	5	4	3	2	1	0
Name	T1E	T0E	ECIE	PCA0ME[2:0]			SYSCKE	Reserved
Type	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE2; SFR Page = 0x0F

Bit	Name	Function
7	T1E	**T1 Enable.** 0: T1 unavailable at Port pin. 1: T1 routed to Port pin.
6	T0E	**T0 Enable.** 0: T0 unavailable at Port pin. 1: T0 routed to Port pin.
5	ECIE	**PCA0 External Counter Input Enable.** 0: ECI unavailable at Port pin. 1: ECI routed to Port pin.
4:2	PCA0ME[2:0]	**PCA0 Module I/O Enable Bits.** 000: All PCA0 I/O unavailable at Port pins. 001: CEX0 routed to Port pin. 010: CEX0, CEX1 routed to Port pins. 011: CEX0, CEX1, CEX2 routed to Port pins. 100: CEX0, CEX1, CEX2, CEX3 routed to Port pins. 101: CEX0, CEX1, CEX2, CEX3, CEX4 routed to Port pins. 110: CEX0, CEX1, CEX2, CEX3, CEX4, CEX5 routed to Port pins. 111: RESERVED
1	SYSCKE	**$\overline{\text{SYSCLK}}$ Output Enable.** 0: $\overline{\text{SYSCLK}}$ unavailable at Port pin. 1: $\overline{\text{SYSCLK}}$ output routed to Port pin.
0	Reserved	Always Write to 0.

SFR Definition 20.18. P1MDIN: Port 1 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xF2; SFR Page = 0x0F

Bit	Name	Function
7:0	P1MDIN[7:0]	**Analog Configuration Bits for P1.7–P1.0 (respectively).** Port pins configured for analog mode have their weak pull-up and digital receiver disabled. For analog mode, the pin also needs to be configured for open-drain mode in the P1MDOUT register. 0: Corresponding P1.n pin is configured for analog mode. 1: Corresponding P1.n pin is not configured for analog mode.

SFR Definition 20.19. P1MDOUT: Port 1 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDOUT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA5; SFR Page = 0x0F

Bit	Name	Function
7:0	P1MDOUT[7:0]	**Output Configuration Bits for P1.7–P1.0 (respectively).** These bits are ignored if the corresponding bit in register P1MDIN is logic 0. 0: Corresponding P1.n Output is open-drain. 1: Corresponding P1.n Output is push-pull.

SFR Definition 20.20. P1SKIP: Port 1 Skip

Bit	7	6	5	4	3	2	1	0
Name	P1SKIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD5; SFR Page = 0x0F

Bit	Name	Function
7:0	P1SKIP[7:0]	**Port 1 Crossbar Skip Enable Bits.** These bits select Port 1 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar. 0: Corresponding P1.n pin is not skipped by the Crossbar. 1: Corresponding P1.n pin is skipped by the Crossbar.

SFR Definition 20.21. P2: Port 2

Bit	7	6	5	4	3	2	1	0
Name	P2[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xA0; SFR Page = All Pages; Bit-Addressable

Bit	Name	Description	Write	Read
7:0	P2[7:0]	**Port 2Data.** Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P2.n Port pin is logic LOW. 1: P2.n Port pin is logic HIGH.

Table 21.2. Manual Baud Rate Parameters Examples

	Baud (bits/sec)														
	20 K			19.2 K			9.6 K			4.8 K			1 K		
SYSCLK (MHz)	Mult.	Pres.	Div.	Mult.	Pres.	Div.	Mult.	Pres.	Div.	Mult.	Pres.	Div.	Mult.	Pres.	Div.
25	0	1	312	0	1	325	1	1	325	3	1	325	19	1	312
24.5	0	1	306	0	1	319	1	1	319	3	1	319	19	1	306
24	0	1	300	0	1	312	1	1	312	3	1	312	19	1	300
22.1184	0	1	276	0	1	288	1	1	288	3	1	288	19	1	276
16	0	1	200	0	1	208	1	1	208	3	1	208	19	1	200
12.25	0	0	306	0	0	319	1	0	319	3	0	319	19	0	306
12	0	0	300	0	0	312	1	0	312	3	0	312	19	0	300
11.0592	0	0	276	0	0	288	1	0	288	3	0	288	19	0	276
8	0	0	200	0	0	208	1	0	208	3	0	208	19	0	200

21.2.4. Baud Rate Calculations—Automatic Mode

If the LIN controller is configured for slave mode, only the prescaler and divider need to be calculated:

$$\text{prescaler} = \ln\left[\frac{\text{SYSCLK}}{4000000}\right] \times \frac{1}{\ln 2} - 1$$

$$\text{divider} = \frac{\text{SYSCLK}}{2^{(\text{prescaler}+1)} \times 20000}$$

The following example calculates the values of these variables for a 24 MHz system clock:

$$\text{prescaler} = \ln\left[\frac{24000000}{4000000}\right] \times \frac{1}{\ln 2} - 1 = 1.585 \cong 1$$

$$\text{divider} = \frac{24000000}{2^{(1+1)} \times 20000} = 300$$

Table 21.3 presents some typical values of system clock and baud rate along with their factors.

LIN Register Definition 21.6. LIN0ST: LIN0 Status Register

Bit	7	6	5	4	3	2	1	0
Name	ACTIVE	IDLTOUT	ABORT	DTREQ	LININT	ERROR	WAKEUP	DONE
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Indirect Address = 0x09

Bit	Name	Function
7	ACTIVE	**LIN Active Indicator Bit.** 0: No transmission activity detected on the LIN bus. 1: Transmission activity detected on the LIN bus.
6	IDLT	**Bus Idle Timeout Bit. (slave mode only)** 0: The bus has not been idle for four seconds. 1: No bus activity has been detected for four seconds, but the bus is not yet in Sleep mode.
5	ABORT	**Aborted Transmission Bit. (slave mode only)** 0: The current transmission has not been interrupted or stopped. This bit is reset to 0 after receiving a SYNCH BREAK that does not interrupt a pending transmission. 1: New SYNCH BREAK detected before the end of the last transmission or the STOP bit (LIN0CTRL.7) has been set.
4	DTREQ	**Data Request Bit. (slave mode only)** 0: Data identifier has not been received. 1: Data identifier has been received.
3	LININT	**Interrupt Request Bit.** 0: An interrupt is not pending. This bit is cleared by setting RSTINT (LIN0CTRL.3) 1: There is a pending LIN0 interrupt.
2	ERROR	**Communication Error Bit.** 0: No error has been detected. This bit is cleared by setting RSTERR (LIN0CTRL.2) 1: An error has been detected.
1	WAKEUP	**Wakeup Bit.** 0: A wakeup signal is not being transmitted and has not been received. 1: A wakeup signal is being transmitted or has been received
0	DONE	**Transmission Complete Bit.** 0: A transmission is not in progress or has not been started. This bit is cleared at the start of a transmission. 1: The current transmission is complete.

23.5.3. Write Sequence (Slave)

During a write sequence, an SMBus master writes data to a slave device. The slave in this transfer will be a receiver during the address byte, and a receiver during all data bytes. When slave events are enabled (INH = 0), the interface enters Slave Receiver Mode when a START followed by a slave address and direction bit (WRITE in this case) is received. Upon entering Slave Receiver Mode, an interrupt is generated and the ACKRQ bit is set. The software must respond to the received slave address with an ACK, or ignore the received slave address with a NACK.

If the received slave address is ignored, slave interrupts will be inhibited until the next START is detected. If the received slave address is acknowledged, zero or more data bytes are received. Software must write the ACK bit at that time to ACK or NACK the received byte.

The interface exits Slave Receiver Mode after receiving a STOP. Note that the interface will switch to Slave Transmitter Mode if SMB0DAT is written while an active Slave Receiver. Figure 23.7 shows a typical slave write sequence. Two received data bytes are shown, though any number of bytes may be received. Notice that the 'data byte transferred' interrupts occur **before** the ACK in this mode.

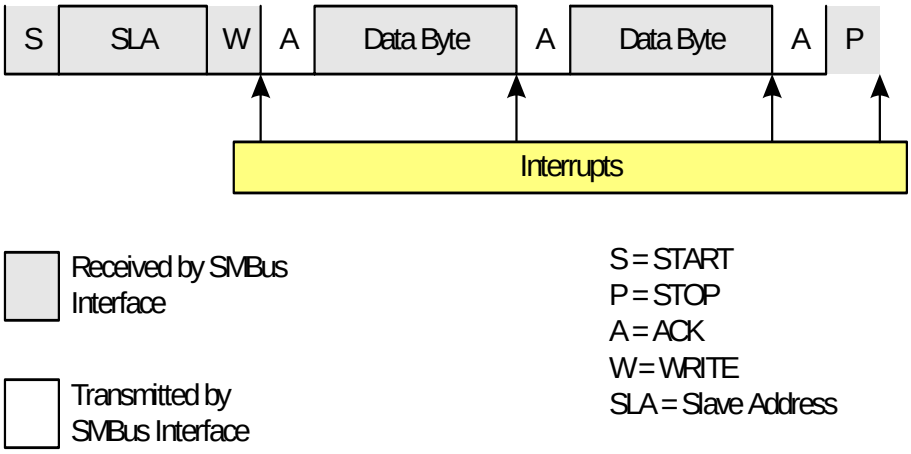

Figure 23.7. Typical Slave Write Sequence

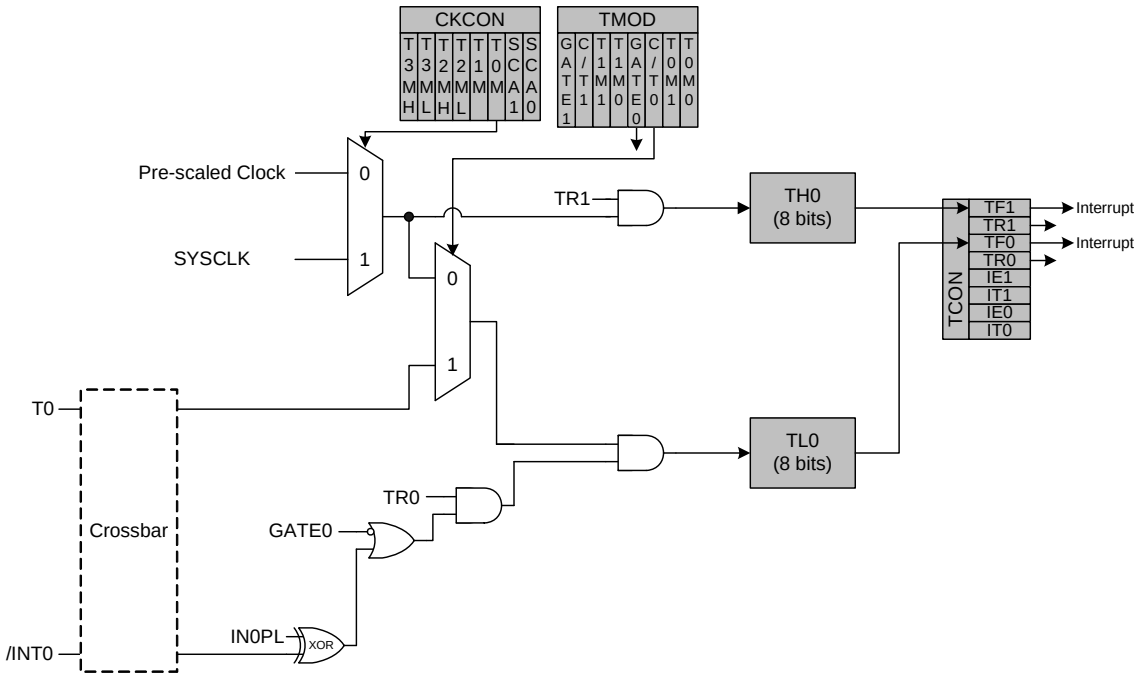

Figure 27.3. T0 Mode 3 Block Diagram

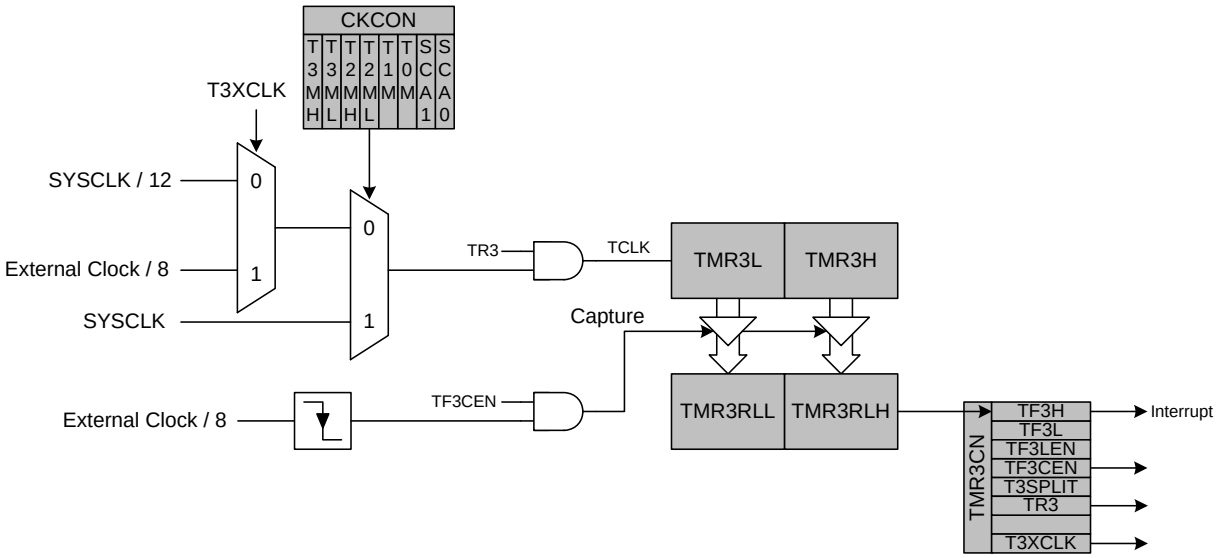

Figure 27.9. Timer 3 External Oscillator Capture Mode Block Diagram

SFR Definition 27.13. TMR3CN: Timer 3 Control

Bit	7	6	5	4	3	2	1	0
Name	TF3H	TF3L	TF3LEN	TF3CEN	T3SPLIT	TR3		T3XCLK
Type	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x91; SFR Page = 0x00

Bit	Name	Function
7	TF3H	**Timer 3 High Byte Overflow Flag.** Set by hardware when the Timer 3 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 3 overflows from 0xFFFF to 0x0000. When the Timer 3 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 3 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF3L	**Timer 3 Low Byte Overflow Flag.** Set by hardware when the Timer 3 low byte overflows from 0xFF to 0x00. TF3L will be set when the low byte overflows regardless of the Timer 3 mode. This bit is not automatically cleared by hardware.
5	TF3LEN	**Timer 3 Low Byte Interrupt Enable.** When set to 1, this bit enables Timer 3 Low Byte interrupts. If Timer 3 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 3 overflows.
4	TF3CEN	**Timer 3 Capture Mode Enable.** 0: Timer 3 Capture Mode is disabled. 1: Timer 3 Capture Mode is enabled.
3	T3SPLIT	**Timer 3 Split Mode Enable.** When this bit is set, Timer 3 operates as two 8-bit timers with auto-reload. 0: Timer 3 operates in 16-bit auto-reload mode. 1: Timer 3 operates as two 8-bit auto-reload timers.
2	TR3	**Timer 3 Run Control.** Timer 3 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR3H only; TMR3L is always enabled in split mode.
1	Unused	Read = 0b; Write = Don’t Care
0	T3XCLK	**Timer 3 External Clock Select.** This bit selects the external clock source for Timer 3. If Timer 3 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 0: Timer 3 clock is the system clock divided by 12. 1: Timer 3 clock is the external clock divided by 8 (synchronized with SYSCLK).