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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), CANbus, LINbus, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	40
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f584-iq

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	CAN2.0B	LIN2.1	Digital Port I/Os	External Memory Interface	Package	Ordering Part Number	Flash Memory (kB)	CAN2.0B	LIN2.1	Digital Port I/Os	External Memory Interface	Package
C8051F580-IQ	128	✓	✓	40	✓	QFP-48	C8051F585-IQ	96	—	—	40	✓	QFP-48
C8051F580-IM	128	✓	✓	40	✓	QFN-48	C8051F585-IM	96	—	—	40	✓	QFN-48
C8051F581-IQ	128	—	—	40	✓	QFP-48	C8051F586-IQ	96	✓	✓	25	—	QFP-32
C8051F581-IM	128	—	—	40	✓	QFN-48	C8051F586-IM	96	✓	✓	25	—	QFN-32
C8051F582-IQ	128	✓	✓	25	—	QFP-32	C8051F587-IQ	96	—	—	25	—	QFP-32
C8051F582-IM	128	✓	✓	25	—	QFN-32	C8051F587-IM	96	—	—	25	—	QFN-32
C8051F583-IQ	128	—	—	25	—	QFP-32	C8051F588-IM	128	✓	✓	33	✓	QFN-40
C8051F583-IM	128	—	—	25	—	QFN-32	C8051F589-IM	128	—	—	33	✓	QFN-40
C8051F584-IQ	96	✓	✓	40	✓	QFP-48	C8051F590-IM	96	✓	✓	33	✓	QFN-40
C8051F584-IM	96	✓	✓	40	✓	QFN-48	C8051F591-IM	96	—	—	33	✓	QFN-40

Note: The suffix of the part number indicates the device rating and the package. All devices are RoHS compliant.

All of these devices are also available in an automotive version. For the automotive version, the -I in the ordering part number is replaced with -A. For example, the automotive version of the C8051F580-IM is the C8051F580-AM.

The -AM and -AQ devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (IMDS) and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.silabs.com with a registered and NDA approved user account. The -AM and -AQ devices enable high volume automotive OEM applications with their enhanced testing and processing. Please contact Silicon Labs sales for more information regarding –AM and -AQ devices for your automotive project.

5. Electrical Characteristics

5.1. Absolute Maximum Specifications

Table 5.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient Temperature under Bias		–55	—	135	°C
Storage Temperature		–65	—	150	°C
Voltage on V_{REGIN} with Respect to GND		–0.3	—	5.5	V
Voltage on V_{DD} with Respect to GND		–0.3	—	2.8	V
Voltage on VDDA with Respect to GND		–0.3	—	2.8	V
Voltage on V_{IO} with Respect to GND		–0.3	—	5.5	V
Voltage on any Port I/O Pin or $\overline{RST}$ with Respect to GND		–0.3	—	V_{IO} + 0.3	V
Maximum Total Current through V_{REGIN} or GND		—	—	500	mA
Maximum Output Current Sunk by $\overline{RST}$ or any Port Pin		—	—	100	mA
Maximum Output Current Sourced by any Port Pin		—	—	100	mA

Note: Stresses outside of the range of the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5.13. Comparator 0, 1 and 2 Electrical Characteristics

VIO = 1.8 to 5.25 V, –40 to +125 °C unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Response Time: Mode 0, Vcm* = 1.5 V	CPn+ – CPn– = 100 mV	—	390	—	ns
	CPn+ – CPn– = –100 mV	—	430	—	ns
Response Time: Mode 1, Vcm* = 1.5 V	CPn+ – CPn– = 100 mV	—	620	—	ns
	CPn+ – CPn– = –100 mV	—	690	—	ns
Response Time: Mode 2, Vcm* = 1.5 V	CPn+ – CPn– = 100 mV	—	770	—	ns
	CP0+ – CP0– = –100 mV	—	860	—	ns
Response Time: Mode 3, Vcm* = 1.5 V	CPn+ – CPn– = 100 mV	—	3500	—	ns
	CPn+ – CPn– = –100 mV	—	3900	—	ns
Common-Mode Rejection Ratio		—	1.5	8.9	mV/V
Positive Hysteresis 1	CPnHYP1–0 = 00	-2	0	2	mV
Positive Hysteresis 2	CPnHYP1–0 = 01	2	6	10	mV
Positive Hysteresis 3	CPnHYP1–0 = 10	5	11	20	mV
Positive Hysteresis 4	CPnHYP1–0 = 11	13	22	40	mV
Negative Hysteresis 1	CPnHYN1–0 = 00	–2	0	2	mV
Negative Hysteresis 2	CPnHYN1–0 = 01	2	6	10	mV
Negative Hysteresis 3	CPnHYN1–0 = 10	5	11	20	mV
Negative Hysteresis 4	CPnHYN1–0 = 11	13	22	40	mV
Inverting or Non-Inverting Input Voltage Range		–0.25	—	V_{IO} + 0.25	V
Input Capacitance		—	8	—	pF
Input Offset Voltage		–10	—	+10	mV
Power Supply					
Power Supply Rejection		—	0.33	—	mV/V
Power-Up Time		—	3	—	µs
Supply Current at DC	Mode 0	—	6.1	20	µA
	Mode 1	—	3.2	10	µA
	Mode 2	—	2.5	7.5	µA
	Mode 3	—	0.5	3	µA

***Note:** Vcm is the common-mode voltage on CP0+ and CP0–.

6.2. Output Code Formatting

The registers ADC0H and ADC0L contain the high and low bytes of the output conversion code. When the repeat count is set to 1, conversion codes are represented in 12-bit unsigned integer format and the output conversion code is updated after each conversion. Inputs are measured from 0 to V_{REF} x 4095/4096. Data can be right-justified or left-justified, depending on the setting of the AD0LJST bit (ADC0CN.2). Unused bits in the ADC0H and ADC0L registers are set to 0. Example codes are shown below for both right-justified and left-justified data.

Input Voltage	Right-Justified ADC0H:ADC0L (AD0LJST = 0)	Left-Justified ADC0H:ADC0L (AD0LJST = 1)
VREF x 4095/4096	0x0FFF	0xFFF0
VREF x 2048/4096	0x0800	0x8000
VREF x 2047/4096	0x07FF	0x7FF0
0	0x0000	0x0000

When the ADC0 Repeat Count is greater than 1, the output conversion code represents the accumulated result of the conversions performed and is updated after the last conversion in the series is finished. Sets of 4, 8, or 16 consecutive samples can be accumulated and represented in unsigned integer format. The repeat count can be selected using the AD0RPT bits in the ADC0CF register. The value must be right-justified (AD0LJST = 0), and unused bits in the ADC0H and ADC0L registers are set to 0. The following example shows right-justified codes for repeat counts greater than 1. Notice that accumulating 2^n samples is equivalent to left-shifting by *n* bit positions when all samples returned from the ADC have the same value.

Input Voltage	Repeat Count = 4	Repeat Count = 8	Repeat Count = 16
V_{REF} x 4095/4096	0x3FFC	0x7FF8	0xFFF0
V_{REF} x 2048/4096	0x2000	0x4000	0x8000
V_{REF} x 2047/4096	0x1FFC	0x3FF8	0x7FF0
0	0x0000	0x0000	0x0000

6.2.1. Settling Time Requirements

A minimum tracking time is required before an accurate conversion is performed. This tracking time is determined by any series impedance, including the AMUX0 resistance, the ADC0 sampling capacitance, and the accuracy required for the conversion.

Figure 6.5 shows the equivalent ADC0 input circuit. The required ADC0 settling time for a given settling accuracy (SA) may be approximated by Equation 6.1. When measuring the Temperature Sensor output, use the tracking time specified in Table 5.11 on page 52. When measuring V_{DD} with respect to GND, R_{TOTAL} reduces to R_{MUX}. See Table 5.10 for ADC0 minimum settling time requirements as well as the mux impedance and sampling capacitor values.

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL} C_{SAMPLE}$$

Equation 6.1. ADC0 Settling Time Requirements

Where:
SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB)
t is the required settling time in seconds
R_{TOTAL} is the sum of the AMUX0 resistance and any external source resistance.
n is the ADC resolution in bits (10).

SFR Definition 6.7. ADC0CN: ADC0 Control

Bit	7	6	5	4	3	2	1	0
Name	AD0EN	BURSTEN	AD0INT	AD0BUSY	AD0WINT	AD0LJST	AD0CM[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE8; SFR Page = 0x00; Bit-Addressable

Bit	Name	Function		
7	AD0EN	**ADC0 Enable Bit.** 0: ADC0 Disabled. ADC0 is in low-power shutdown. 1: ADC0 Enabled. ADC0 is active and ready for data conversions.		
6	BURSTEN	**ADC0 Burst Mode Enable Bit.** 0: Burst Mode Disabled. 1: Burst Mode Enabled.		
5	AD0INT	**ADC0 Conversion Complete Interrupt Flag.** 0: ADC0 has not completed a data conversion since AD0INT was last cleared. 1: ADC0 has completed a data conversion.		
4	AD0BUSY	**ADC0 Busy Bit.**	**Read:** 0: ADC0 conversion is not in progress. 1: ADC0 conversion is in progress.	**Write:** 0: No Effect. 1: Initiates ADC0 Conversion if AD0CM[1:0] = 00b
3	AD0WINT	**ADC0 Window Compare Interrupt Flag.** This bit must be cleared by software 0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared. 1: ADC0 Window Comparison Data match has occurred.		
2	AD0LJST	**ADC0 Left Justify Select Bit.** 0: Data in ADC0H:ADC0L registers is right-justified 1: Data in ADC0H:ADC0L registers is left-justified. This option should not be used with a repeat count greater than 1 (when AD0RPT[1:0] is 01b, 10b, or 11b).		
1:0	AD0CM[1:0]	**ADC0 Start of Conversion Mode Select.** 00: ADC0 start-of-conversion source is write of 1 to AD0BUSY. 01: ADC0 start-of-conversion source is overflow of Timer 1. 10: ADC0 start-of-conversion source is rising edge of external CNVSTR. 11: ADC0 start-of-conversion source is overflow of Timer 2.		

SFR Definition 6.13. ADC0MX: ADC0 Channel Select

Bit	7	6	5	4	3	2	1	0
Name			ADC0MX[5:0]					
Type	R	R	R/W					
Reset	0	0	1	1	1	1	1	1

SFR Address = 0xBB; SFR Page = 0x00;

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don't Care.
5:0	AMX0P[5:0]	**AMUX0 Positive Input Selection.** 000000: P0.0 000001: P0.1 000010: P0.2 000011: P0.3 000100: P0.4 000101: P0.5 000110: P0.6 000111: P0.7 001000: P1.0 001001: P1.1 001010: P1.2 001011: P1.3 001100: P1.4 001101: P1.5 001110: P1.6 001111: P1.7 010000: P2.0 010001: P2.1 010010: P2.2 010011: P2.3 010100: P2.4 010101: P2.5 010110: P2.6 010111: P2.7 011000: P3.0 011001: P3.1 (Available on 48-pin and 40-pin package devices) 011010: P3.2 (Available on 48-pin and 40-pin package devices) 011011: P3.3 (Available on 48-pin and 40-pin package devices) 011100: P3.4 (Available on 48-pin and 40-pin package devices) 011101: P3.5 (Available on 48-pin and 40-pin package devices) 011110: P3.6 (Available on 48-pin and 40-pin package devices) 011111: P3.7 (Available on 48-pin and 40-pin package devices) 100000–101111: Reserved 110000: Temp Sensor 110001: V_{DD} 110010–111111: GND

SFR Definition 9.5. CPT2CN: Comparator2 Control

Bit	7	6	5	4	3	2	1	0
Name	CP2EN	CP2OUT	CP2RIF	CP2FIF	CP2HYP[1:0]		CP2HYN[1:0]	
Type	R/W	R	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x9A; SFR Page = 0x10

Bit	Name	Function
7	CP2EN	**Comparator2 Enable Bit.** 0: Comparator2 Disabled. 1: Comparator2 Enabled.
6	CP2OUT	**Comparator2 Output State Flag.** 0: Voltage on CP2+ < CP2–. 1: Voltage on CP2+ > CP2–.
5	CP2RIF	**Comparator2 Rising-Edge Flag. Must be cleared by software.** 0: No Comparator2 Rising Edge has occurred since this flag was last cleared. 1: Comparator2 Rising Edge has occurred.
4	CP2FIF	**Comparator2 Falling-Edge Flag. Must be cleared by software.** 0: No Comparator2 Falling-Edge has occurred since this flag was last cleared. 1: Comparator2 Falling-Edge has occurred.
3:2	CP2HYP[1:0]	**Comparator2 Positive Hysteresis Control Bits.** 00: Positive Hysteresis Disabled. 01: Positive Hysteresis = 5 mV. 10: Positive Hysteresis = 10 mV. 11: Positive Hysteresis = 20 mV.
1:0	CP2HYN[1:0]	**Comparator2 Negative Hysteresis Control Bits.** 00: Negative Hysteresis Disabled. 01: Negative Hysteresis = 5 mV. 10: Negative Hysteresis = 10 mV. 11: Negative Hysteresis = 20 mV.

SFR Definition 11.1. DPL: Data Pointer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	DPL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x82; SFR Page = All Pages

Bit	Name	Function
7:0	DPL[7:0]	**Data Pointer Low.** The DPL register is the low byte of the 16-bit DPTR. DPTR is used to access indirectly addressed Flash memory or XRAM.

SFR Definition 11.2. DPH: Data Pointer High Byte

Bit	7	6	5	4	3	2	1	0
Name	DPH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x83; SFR Page = All Pages

Bit	Name	Function
7:0	DPH[7:0]	**Data Pointer High.** The DPH register is the high byte of the 16-bit DPTR. DPTR is used to access indirectly addressed Flash memory or XRAM.

SFR Definition 13.3. SFRNEXT: SFR Next

Bit	7	6	5	4	3	2	1	0
Name	SFRNEXT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x85; SFR Page = All Pages

Bit	Name	Function
7:0	SFRNEXT[7:0]	**SFR Page Bits.** This is the value that will go to the SFR Page register upon a return from interrupt. Write: Sets the SFR Page contained in the second byte of the SFR Stack. This will cause the SFRPAGE SFR to have this SFR page value upon a return from interrupt. Read: Returns the value of the SFR page contained in the second byte of the SFR stack. SFR page context is retained upon interrupts/return from interrupts in a 3 byte SFR Page Stack: SFRPAGE is the first entry, SFRNEXT is the second, and SFRLAST is the third entry. The SFR stack bytes may be used alter the context in the SFR Page Stack, and will not cause the stack to “push” or “pop”. Only interrupts and return from interrupts cause pushes and pops of the SFR Page Stack.

17.1. Power-On Reset

During power-up, the device is held in a reset state and the $\overline{\text{RST}}$ pin is driven low until V_{DD} settles above V_{RST}. A delay occurs before the device is released from reset; the delay decreases as the V_{DD} ramp time increases (V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST}). Figure 17.2. plots the power-on and V_{DD} monitor reset timing. The maximum V_{DD} ramp time is 1 ms; slower ramp times may cause the device to be released from reset before V_{DD} reaches the V_{RST} level. For ramp times less than 1 ms, the power-on reset delay ($T_{PORDelay}$) is typically less than 0.3 ms.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000) software can read the PORSF flag to determine if a power-up was the cause of reset. The content of internal data memory should be assumed to be undefined after a power-on reset. The V_{DD} monitor is enabled following a power-on reset.

Note: For devices with a date code before year 2011, work week 24 (1124), if the /RST pin is held low for more than 1 second while power is applied to the device, and then /RST is released, a percentage of devices may lock up and fail to execute code. Toggling the /RST pin does not clear the condition. The condition is cleared by cycling power. Most devices that are affected will show the lock up behavior only within a narrow range of temperatures (a 5 to 10 °C window). Parts with a date code of year 2011, work week 24 (1124) or later do not have any restrictions on /RST low time. The date code is included in the bottom-most line of the package top side marking. The date code is a four-digit number with the format YYWW, where YY is the two-digit calendar year and WW is the two digit work week.

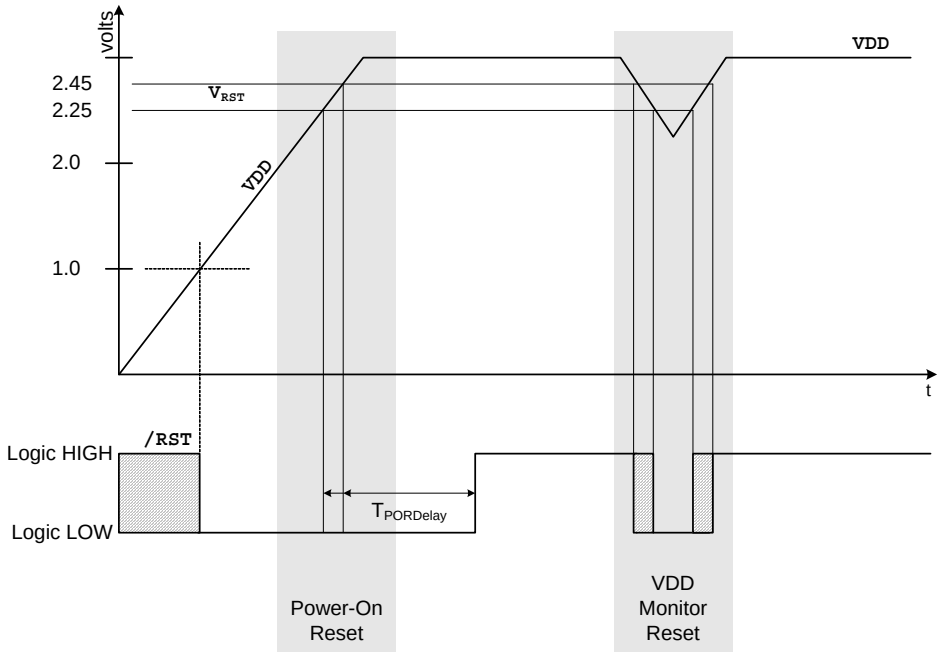

Figure 17.2. Power-On and V_{DD} Monitor Reset Timing

18.6.1. Non-Multiplexed Mode

18.6.1.1. 16-bit MOVX: EMI0CF[4:2] = 101, 110, or 111

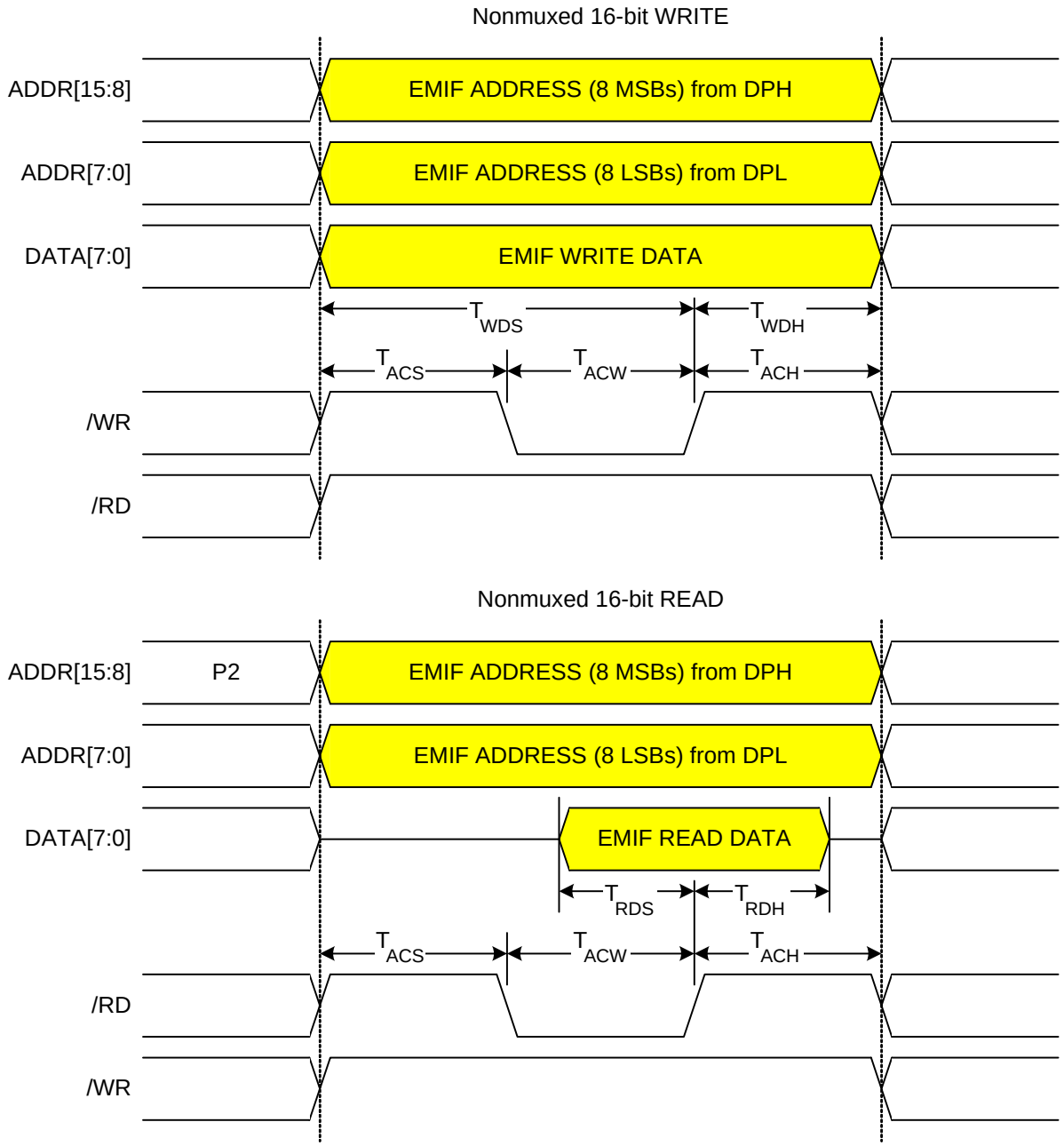

Figure 18.4. Non-multiplexed 16-bit MOVX Timing

SFR Definition 20.2. XBR1: Port I/O Crossbar Register 1

Bit	7	6	5	4	3	2	1	0
Name	T1E	T0E	ECIE	PCA0ME[2:0]			SYSCKE	Reserved
Type	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE2; SFR Page = 0x0F

Bit	Name	Function
7	T1E	**T1 Enable.** 0: T1 unavailable at Port pin. 1: T1 routed to Port pin.
6	T0E	**T0 Enable.** 0: T0 unavailable at Port pin. 1: T0 routed to Port pin.
5	ECIE	**PCA0 External Counter Input Enable.** 0: ECI unavailable at Port pin. 1: ECI routed to Port pin.
4:2	PCA0ME[2:0]	**PCA0 Module I/O Enable Bits.** 000: All PCA0 I/O unavailable at Port pins. 001: CEX0 routed to Port pin. 010: CEX0, CEX1 routed to Port pins. 011: CEX0, CEX1, CEX2 routed to Port pins. 100: CEX0, CEX1, CEX2, CEX3 routed to Port pins. 101: CEX0, CEX1, CEX2, CEX3, CEX4 routed to Port pins. 110: CEX0, CEX1, CEX2, CEX3, CEX4, CEX5 routed to Port pins. 111: RESERVED
1	SYSCKE	**$\overline{\text{SYSCLK}}$ Output Enable.** 0: $\overline{\text{SYSCLK}}$ unavailable at Port pin. 1: $\overline{\text{SYSCLK}}$ output routed to Port pin.
0	Reserved	Always Write to 0.

SFR Definition 20.18. P1MDIN: Port 1 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xF2; SFR Page = 0x0F

Bit	Name	Function
7:0	P1MDIN[7:0]	**Analog Configuration Bits for P1.7–P1.0 (respectively).** Port pins configured for analog mode have their weak pull-up and digital receiver disabled. For analog mode, the pin also needs to be configured for open-drain mode in the P1MDOUT register. 0: Corresponding P1.n pin is configured for analog mode. 1: Corresponding P1.n pin is not configured for analog mode.

SFR Definition 20.19. P1MDOUT: Port 1 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDOUT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA5; SFR Page = 0x0F

Bit	Name	Function
7:0	P1MDOUT[7:0]	**Output Configuration Bits for P1.7–P1.0 (respectively).** These bits are ignored if the corresponding bit in register P1MDIN is logic 0. 0: Corresponding P1.n Output is open-drain. 1: Corresponding P1.n Output is push-pull.

23.1. Supporting Documents

It is assumed the reader is familiar with or has access to the following supporting documents:

1. The I^2C-Bus and How to Use It (including specifications), Philips Semiconductor.
2. The I^2C-Bus Specification—Version 2.0, Philips Semiconductor.
3. System Management Bus Specification—Version 1.1, SBS Implementers Forum.

23.2. SMBus Configuration

Figure 23.2 shows a typical SMBus configuration. The SMBus specification allows any recessive voltage between 3.0 V and 5.0 V; different devices on the bus may operate at different voltage levels. The bi-directional SCL (serial clock) and SDA (serial data) lines must be connected to a positive power supply voltage through a pullup resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the SCL and SDA lines, so that both are pulled high (recessive state) when the bus is free. The maximum number of devices on the bus is limited only by the requirement that the rise and fall times on the bus not exceed 300 ns and 1000 ns, respectively.

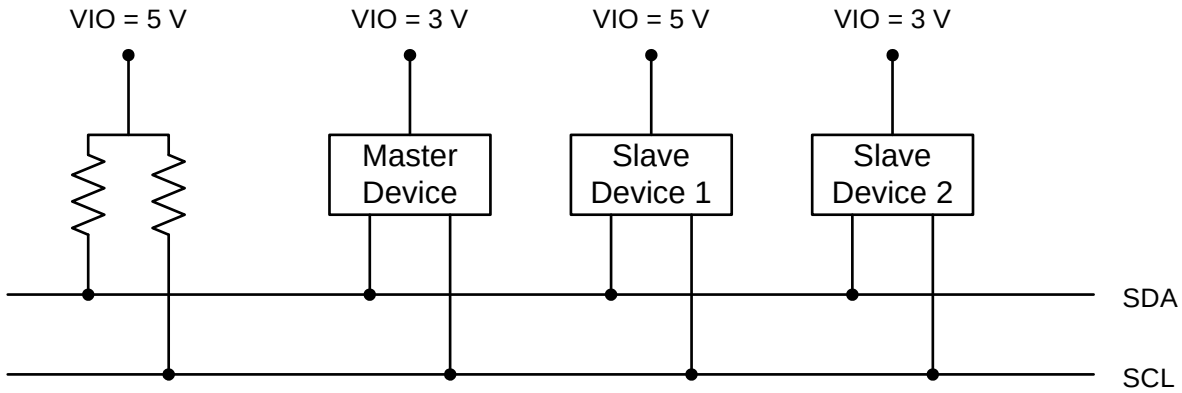

Figure 23.2. Typical SMBus Configuration

23.3. SMBus Operation

Two types of data transfers are possible: data transfers from a master transmitter to an addressed slave receiver (WRITE), and data transfers from an addressed slave transmitter to a master receiver (READ). The master device initiates both types of data transfers and provides the serial clock pulses on SCL. The SMBus interface may operate as a master or a slave, and multiple master devices on the same bus are supported. If two or more masters attempt to initiate a data transfer simultaneously, an arbitration scheme is employed with a single master always winning the arbitration. It is not necessary to specify one device as the Master in a system; any device who transmits a START and a slave address becomes the master for the duration of that transfer.

A typical SMBus transaction consists of a START condition followed by an address byte (Bits7–1: 7-bit slave address; Bit0: R/W direction bit), one or more bytes of data, and a STOP condition. Bytes that are received (by a master or slave) are acknowledged (ACK) with a low SDA during a high SCL (see Figure 23.3). If the receiving device does not ACK, the transmitting device will read a NACK (not acknowledge), which is a high SDA during a high SCL.

The direction bit (R/W) occupies the least-significant bit position of the address byte. The direction bit is set to logic 1 to indicate a "READ" operation and cleared to logic 0 to indicate a "WRITE" operation.

23.5.3. Write Sequence (Slave)

During a write sequence, an SMBus master writes data to a slave device. The slave in this transfer will be a receiver during the address byte, and a receiver during all data bytes. When slave events are enabled (INH = 0), the interface enters Slave Receiver Mode when a START followed by a slave address and direction bit (WRITE in this case) is received. Upon entering Slave Receiver Mode, an interrupt is generated and the ACKRQ bit is set. The software must respond to the received slave address with an ACK, or ignore the received slave address with a NACK.

If the received slave address is ignored, slave interrupts will be inhibited until the next START is detected. If the received slave address is acknowledged, zero or more data bytes are received. Software must write the ACK bit at that time to ACK or NACK the received byte.

The interface exits Slave Receiver Mode after receiving a STOP. Note that the interface will switch to Slave Transmitter Mode if SMB0DAT is written while an active Slave Receiver. Figure 23.7 shows a typical slave write sequence. Two received data bytes are shown, though any number of bytes may be received. Notice that the 'data byte transferred' interrupts occur **before** the ACK in this mode.

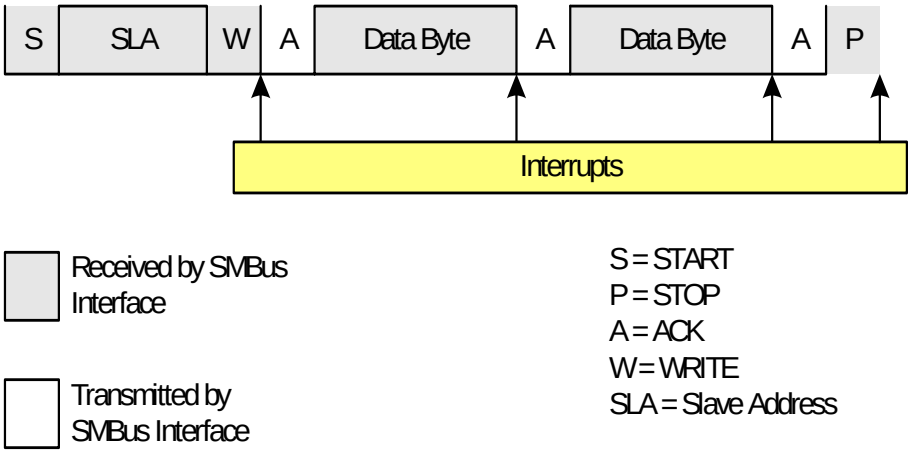

Figure 23.7. Typical Slave Write Sequence

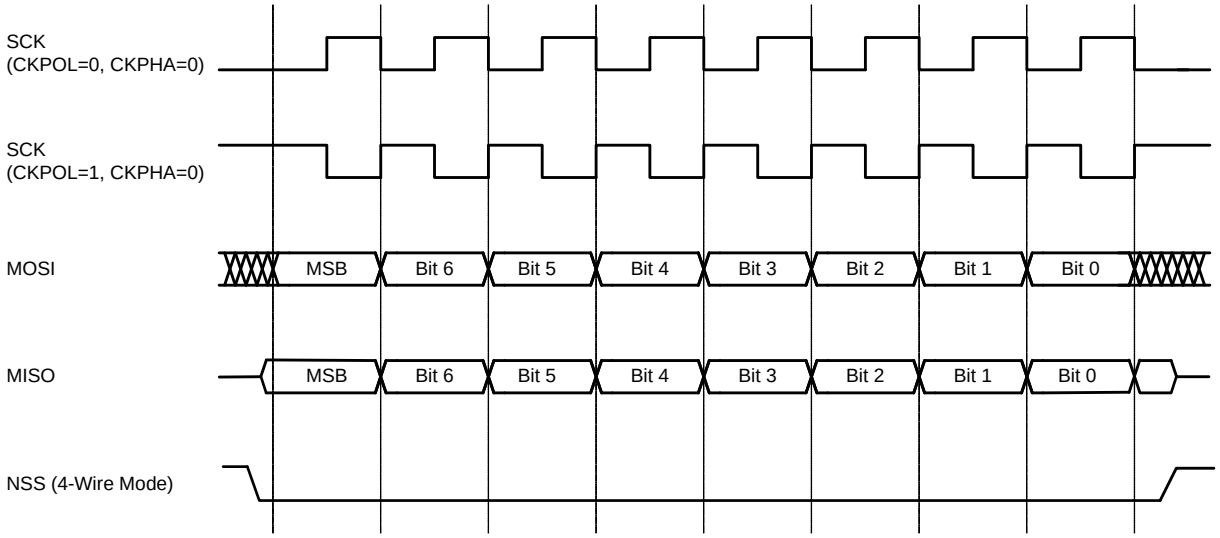

Figure 26.6. Slave Mode Data/Clock Timing (CKPHA = 0)

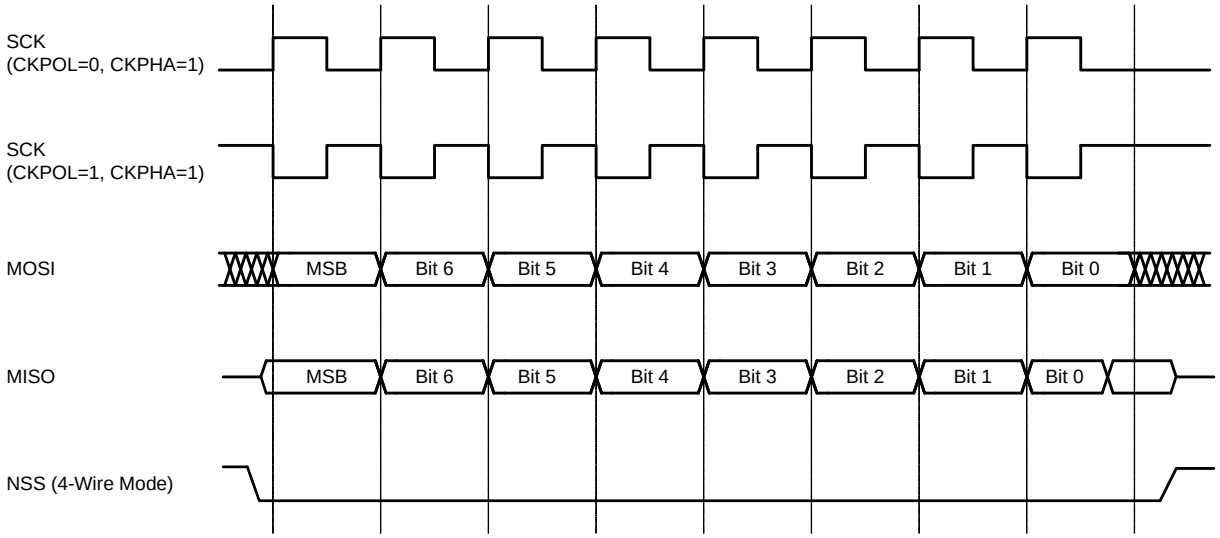

Figure 26.7. Slave Mode Data/Clock Timing (CKPHA = 1)

26.6. SPI Special Function Registers

SPI0 is accessed and controlled through four special function registers in the system controller: SPI0CN Control Register, SPI0DAT Data Register, SPI0CFG Configuration Register, and SPI0CKR Clock Rate Register. The four special function registers related to the operation of the SPI0 Bus are described in the following figures.

27.1. Timer 0 and Timer 1

Each timer is implemented as a 16-bit register accessed as two separate bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The Counter/Timer Control register (TCON) is used to enable Timer 0 and Timer 1 as well as indicate status. Timer 0 interrupts can be enabled by setting the ET0 bit in the IE register (Section “14.2. Interrupt Register Descriptions” on page 129); Timer 1 interrupts can be enabled by setting the ET1 bit in the IE register (Section “14.2. Interrupt Register Descriptions” on page 129). Both counter/timers operate in one of four primary modes selected by setting the Mode Select bits T1M1–T0M0 in the Counter/Timer Mode register (TMOD). Each timer can be configured independently. Each operating mode is described below.

27.1.1. Mode 0: 13-bit Counter/Timer

Timer 0 and Timer 1 operate as 13-bit counter/timers in Mode 0. The following describes the configuration and operation of Timer 0. However, both timers operate identically, and Timer 1 is configured in the same manner as described for Timer 0.

The TH0 register holds the eight MSBs of the 13-bit counter/timer. TL0 holds the five LSBs in bit positions TL0.4–TL0.0. The three upper bits of TL0 (TL0.7–TL0.5) are indeterminate and should be masked out or ignored when reading. As the 13-bit timer register increments and overflows from 0x1FFF (all ones) to 0x0000, the timer overflow flag TF0 (TCON.5) is set and an interrupt will occur if Timer 0 interrupts are enabled.

The C/T0 bit (TMOD.2) selects the counter/timer's clock source. When C/T0 is set to logic 1, high-to-low transitions at the selected Timer 0 input pin (T0) increment the timer register (Refer to Section “20.3. Priority Crossbar Decoder” on page 192 for information on selecting and configuring external I/O pins). Clearing C/T selects the clock defined by the T0M bit (CKCON.3). When T0M is set, Timer 0 is clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 27.1).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or the input signal $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 14.7). Setting GATE0 to 1 allows the timer to be controlled by the external input signal $\overline{\text{INT0}}$ (see Section “14.2. Interrupt Register Descriptions” on page 129), facilitating pulse width measurements.

TR0	GATE0	$\overline{\text{INT0}}$	Counter/Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0	Disabled
1	1	1	Enabled
Note: X = Don't Care			

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal $\overline{\text{INT1}}$ is used with Timer 1; the $\overline{\text{INT1}}$ polarity is defined by bit IN1PL in register IT01CF (see SFR Definition 14.7).

The TF3H bit is set when TMR3H overflows from 0xFF to 0x00; the TF3L bit is set when TMR3L overflows from 0xFF to 0x00. When Timer 3 interrupts are enabled, an interrupt is generated each time TMR3H overflows. If Timer 3 interrupts are enabled and TF3LEN (TMR3CN.5) is set, an interrupt is generated each time either TMR3L or TMR3H overflows. When TF3LEN is enabled, software must check the TF3H and TF3L flags to determine the source of the Timer 3 interrupt. The TF3H and TF3L interrupt flags are not cleared by hardware and must be manually cleared by software.

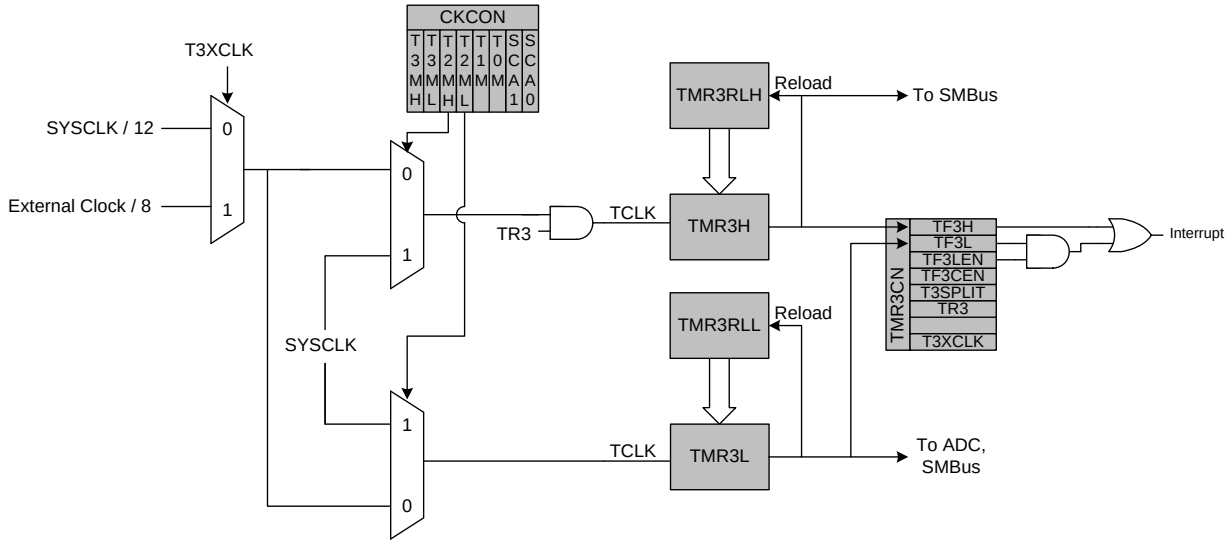

Figure 27.8. Timer 3 8-Bit Mode Block Diagram

27.3.3. External Oscillator Capture Mode

Capture Mode allows the external oscillator to be measured against the system clock. Timer 3 can be clocked from the system clock, or the system clock divided by 12, depending on the T3ML (CKCON.6), and T3XCLK bits. When a capture event is generated, the contents of Timer 3 (TMR3H:TMR3L) are loaded into the Timer 3 reload registers (TMR3RLH:TMR3RLL) and the TF3H flag is set. A capture event is generated by the falling edge of the clock source being measured, which is the external oscillator/8. By recording the difference between two successive timer capture values, the external oscillator frequency can be determined with respect to the Timer 3 clock. The Timer 3 clock should be much faster than the capture clock to achieve an accurate reading. Timer 3 should be in 16-bit auto-reload mode when using Capture Mode.

If the SYSCLK is 24 MHz and the difference between two successive captures is 5861, then the external clock frequency is as follows:

24 MHz/(5861/8) = 0.032754 MHz or 32.754 kHz

This mode allows software to determine the external oscillator frequency when an RC network or capacitor is used to generate the clock source.

SFR Definition 27.20. TMRnCAPL: Timer 4 and 5 Capture Register Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMRnRLL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

TMR4CAPL SFR Address = 0xCA; TMR5CAPL SFR Address = 0x92; SFR Page = 0x10

Bit	Name	Function
7:0	TMRnCAPL[7:0]	**Timer n Reload Register Low Byte.** TMRnCAPL captures the low byte of Timer 4 and 5 when Timer 4 and 5 are configured in capture mode. When Timer 4 and 5 are configured in auto-reload mode, it holds the low byte of the reload value.

SFR Definition 27.21. TMRnCAPH: Timer 4 and 5 Capture Register High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMRnRLH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

TMR4CAPH SFR Address = 0xCB; TMR5CAPH SFR Address = 0x93; SFR Page = 0x10

Bit	Name	Function
7:0	TMRnCAPH[7:0]	**Timer n Reload Register High Byte.** TMRnCAPH captures the high byte of Timer 4 and 5 when Timer 4 and 5 are configured in capture mode. When Timer 4 and 5 are configured in auto-reload mode, it holds the high byte of the reload value.

- Added Port 2 Event and Port 3 Events to wake-up sources in “19.2.1. Internal Oscillator Suspend Mode” .
- Updated SFR Definition 20.3 with correct names for bits CP2AE and CP2E.
- Updated “21. Local Interconnect Network (LIN0)” with a voltage range specification for the internal oscillator.
- Updated LIN Register Definitions 21.9 and 21.10 with correct reset values.
- Updated “22. Controller Area Network (CAN0)” with a voltage range specification for the internal oscillator.
- Updated C2 Register Definitions 30.2 and 30.3 with correct C2 and SFR addresses.

Revision 1.2 to Revision 1.3

- Updated the note in “Power-Fail Reset/VDD Monitor” on page 154 to use a larger font.
- Added the note regarding the voltage regulator and VDD monitor in the high setting from “Power-Fail Reset/VDD Monitor” on page 154 to “Voltage Regulator (REG0)” on page 89 and “V_{DD} Maintenance and the V_{DD} monitor” on page 143. Also adjusted the language regarding the solution with the highest system reliability.
- Updated the steps in “V_{DD} Maintenance and the V_{DD} monitor” on page 143 to mention using the VDD monitor in the high setting during flash write/erase operations.
- Updated the SUSPEND bit description in OSCICN (SFR Definition 19.2) to mention that firmware must set the ZTCEN bit in REF0CN (SFR Definition 8.1) before entering suspend.
- Added a note to the IFRDY flag in the OSCICN register (SFR Definition 19.2) that the flag may not accurately reflect the state of the oscillator.
- Added VDD Ramp Time for Power On spec to Table 5.4, “Reset Electrical Characteristics,” on page 48.
- Added a note regarding programming at cold temperatures on –I devices to “Programming The Flash Memory” on page 138 and added Temperature during Programming Operations specification to Table 5.5, “Flash Electrical Characteristics,” on page 48.
- Added a note regarding P0.0/VREF when VDD is used as the reference to Table 20.1, “Port I/O Assignment for Analog Functions,” on page 191 and to the description of the REFSL bit in REF0CN (SFR Definition 8.1).
- Added a note regarding a potential unknown state on GPIO during power up if VIO ramps significantly before VDD to “Port Input/Output” on page 188 and “Reset Sources” on page 152.
- Added steps to set the FLEWT bit in the flash write/erase procedures in “Flash Erase Procedure” on page 139, “Flash Write Procedure” on page 139, and “Flash Write Optimization” on page 140.
- Added the “Reprogramming the VDD Monitor High Threshold” on page 138 section.
- Added a note regarding fast changes on VDD causing the V_{DD} Monitor to trigger to “Power-Fail Reset/VDD Monitor” on page 154.
- Added notes regarding UART TX and RX behavior in “Data Transmission” on page 259 and “Data Reception” on page 259.
- Added a note regarding an issue with /RST low time on some older devices to “Power-On Reset” on page 153.
- Added Table 5.8, “Crystal Oscillator Electrical Characteristics,” on page 50.
- Added a paragraph in “External Crystal Example” on page 185 regarding surface mount crystals and drive current.
- Removed recommendations to introduce a delay after enabling the VDD Monitor before enabling it as a reset source in “Power-Fail Reset/VDD Monitor” on page 154.