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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	40
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f585-iqr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Figure 4.8. QFP-32 Package Drawing

 Table 4.8. QFP-32 Landing Diagram Dimensions

Dimension	Min	Max	Dimension	Min	Мах
C1	8.40	8.50	X1	0.40	0.50
C2	8.40	8.50	Y1	1.25	1.35
E	0.80 BSC				

Notes:

General

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60μm minimum, all the way around the pad.

Stencil Design

- **4.** A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 5. The stencil thickness should be 0.125mm (5 mils).
- 6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

Card Assembly

- 7. A No-Clean, Type-3 solder paste is recommended.
- 8. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



Table 5.3. Port I/O DC Electrical Characteristics

 V_{DD} = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified.

Parameters	Conditions	Min	Тур	Max	Units
Output High Voltage	I _{OH} = –3 mA, Port I/O push-pull	V _{IO} – 0.4		_	V
	I _{OH} = −10 μA, Port I/O push-pull	V _{IO} – 0.02	—	—	
	I _{OH} = –10 mA, Port I/O push-pull	—	V _{IO} – 0.7	—	
Output Low Voltage	V _{IO} = 1.8 V:				
	Ι _{ΟL} = 70 μΑ	—	—	50	
	I _{OL} = 8.5 mA	—	—	750	
	V _{IO} = 2.7 V:				
	I _{OL} = 70 μA	—	—	45	mV
	I _{OL} = 8.5 mA	—	—	550	
	V _{IO} = 5.25 V:				
	I _{OL} = 70 μA	—	—	40	
	I _{OL} = 8.5 mA	—	—	400	
Input High Voltage	V _{REGIN} = 5.25 V	0.7 x VIO	—	—	V
Input Low Voltage	V _{REGIN} = 2.7 V	_	_	0.3 x VIO	V
	Weak Pullup Off	—	—	2	
	Weak Pullup On, V _{IO} = 2.1 V,				
	$V_{IN} = 0 V, V_{DD} = 1.8 V$	_	6	9	
Input Leakage	Weak Pullup On, V _{IO} = 2.6 V,				μA
Current	$V_{IN} = 0 V, V_{DD} = 2.6 V$	_	16	22	
	Weak Pullup On, V _{IO} = 5.0 V,				
	$V_{IN} = 0 V, V_{DD} = 2.6 V$		45	115	



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Figure 6.3. 12-Bit ADC Tracking Mode Example

6.1.4. Burst Mode

Burst Mode is a power saving feature that allows ADC0 to remain in a very low power state between conversions. When Burst Mode is enabled, ADC0 wakes from a very low power state, accumulates 1, 4, 8, or 16 samples using an internal Burst Mode clock (approximately 25 MHz), then re-enters a very low power state. Since the Burst Mode clock is independent of the system clock, ADC0 can perform multiple conversions then enter a very low power state within a single system clock cycle, even if the system clock is slow (e.g., 32.768 kHz), or suspended.

Burst Mode is enabled by setting BURSTEN to logic 1. When in Burst Mode, AD0EN controls the ADC0 idle power state (i.e. the state ADC0 enters when not tracking or performing conversions). If AD0EN is set to logic 0, ADC0 is powered down after each burst. If AD0EN is set to logic 1, ADC0 remains enabled after each burst. On each convert start signal, ADC0 is awakened from its Idle Power State. If ADC0 is powered down, it will automatically power up and wait the programmable Power-Up Time controlled by the AD0PWR bits. Otherwise, ADC0 will start tracking and converting immediately. Figure 6.4 shows an example of Burst Mode Operation with a slow system clock and a repeat count of 4.

Important Note: When Burst Mode is enabled, only Post-Tracking and Dual-Tracking modes can be used.

When Burst Mode is enabled, a single convert start will initiate a number of conversions equal to the repeat count. When Burst Mode is disabled, a convert start is required to initiate each conversion. In both modes, the ADC0 End of Conversion Interrupt Flag (AD0INT) will be set after "repeat count" conversions have



6.3.2. Setting the Gain Value

The three programmable gain registers are accessed indirectly using the ADC0H and ADC0L registers when the GAINEN bit (ADC0CF.0) bit is set. ADC0H acts as the address register, and ADC0L is the data register. The programmable gain registers can only be written to and cannot be read. See Gain Register Definition 6.1, Gain Register Definition 6.2, and Gain Register Definition 6.3 for more information.

The gain is programmed using the following steps:

- 1. Set the GAINEN bit (ADC0CF.0)
- 2. Load the ADC0H with the ADC0GNH, ADC0GNL, or ADC0GNA address.
- 3. Load ADC0L with the desired value for the selected gain register.
- 4. Reset the GAINEN bit (ADC0CF.0)

Notes:

- 1. An ADC conversion should not be performed while the GAINEN bit is set.
- 2. Even with gain enabled, the maximum input voltage must be less than V_{REGIN} and the maximum voltage of the signal after gain must be less than or equal to V_{REF}.

In code, changing the value to 0.44 gain from the previous example looks like:

// in 'C':

ADC0CF = 0x01;	// GAINEN = 1
ADC0H = 0x04;	// Load the ADC0GNH address
ADC0L = 0x6C;	// Load the upper byte of 0x6CA to ADC0GNH
ADC0H = 0x07;	// Load the ADC0GNL address
ADC0L = 0xA0;	// Load the lower nibble of 0x6CA to ADC0GNL
ADC0H = 0x08;	// Load the ADC0GNA address
ADC0L = 0x01;	// Set the GAINADD bit
ADC0CF &= ~0x01;	// GAINEN = 0
; in assembly	
ORL ADC0CF,#01H	; GAINEN = 1

	, 0, (11) = 1
MOV ADC0H,#04H	; Load the ADC0GNH address
MOV ADC0L,#06CH	; Load the upper byte of 0x6CA to ADC0GNH
MOV ADC0H,#07H	; Load the ADC0GNL address
MOV ADC0L,#0A0H	; Load the lower nibble of 0x6CA to ADC0GNL
MOV ADC0H,#08H	; Load the ADC0GNA address
MOV ADC0L,#01H	; Set the GAINADD bit
ANL ADC0CF,#0FEH	; GAINEN = 0



SFR Definition 6.5. ADC0H: ADC0 Data Word MSB

Bit	7	6	5	4	3	2	1	0
Name	ADC0H[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xBE; SFR Page = 0x00

Bit	Name	Function
7:0	ADC0H[7:0]	ADC0 Data Word High-Order Bits.
		For AD0LJST = 0 and AD0RPT as follows:
		00: Bits 3–0 are the upper 4 bits of the 12-bit result. Bits 7–4 are 0000b.
		01: Bits 4–0 are the upper 5 bits of the 14-bit result. Bits 7–5 are 000b.
		10: Bits 5–0 are the upper 6 bits of the 15-bit result. Bits 7–6 are 00b.
		11: Bits 7–0 are the upper 8 bits of the 16-bit result.
		For AD0LJST = 1 (AD0RPT must be 00): Bits 7–0 are the most-significant bits of the
		ADC0 12-bit result.

SFR Definition 6.6. ADC0L: ADC0 Data Word LSB

Bit	7	6	5	4	3	2	1	0
Name	ADC0L[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xBD; SFR Page = 0x00

Bit	Name	Function
7:0	ADC0L[7:0]	ADC0 Data Word Low-Order Bits.
		For AD0LJST = 0: Bits 7–0 are the lower 8 bits of the ADC0 Accumulated Result. For AD0LJST = 1 (AD0RPT must be '00'): Bits 7–4 are the lower 4 bits of the 12-bit result. Bits 3–0 are 0000b.



8. Voltage Reference

The Voltage reference multiplexer on the C8051F58x/F59x devices is configurable to use an externally connected voltage reference, the on-chip reference voltage generator routed to the VREF pin, or the V_{DD} power supply voltage (see Figure 8.1). The REFSL bit in the Reference Control register (REF0CN, SFR Definition 8.1) selects the reference source for the ADC. For an external source or the on-chip reference, REFSL should be set to 0 to select the VREF pin. To use V_{DD} as the reference source, REFSL should be set to 1.

The BIASE bit enables the internal voltage bias generator, which is used by the ADC, Temperature Sensor, and internal oscillator. This bias is automatically enabled when any peripheral which requires it is enabled, and it does not need to be enabled manually. The bias generator may be enabled manually by writing a 1 to the BIASE bit in register REFOCN. The electrical specifications for the voltage reference circuit are given in Table 5.12.

The on-chip voltage reference circuit consists of a temperature stable bandgap voltage reference generator and a gain-of-two output buffer amplifier. The output voltage is selectable between 1.5 V and 2.25 V. The on-chip voltage reference can be driven on the VREF pin by setting the REFBE bit in register REFOCN to a 1. The maximum load seen by the VREF pin must be less than 200 μ A to GND. Bypass capacitors of 0.1 μ F and 4.7 μ F are recommended from the VREF pin to GND. If the on-chip reference is not used, the REFBE bit should be cleared to 0. Electrical specifications for the on-chip voltage reference are given in Table 5.12.

Important Note about the VREF Pin: When using either an external voltage reference or the on-chip reference circuitry, the VREF pin should be configured as an analog pin and skipped by the Digital Crossbar. Refer to Section "20. Port Input/Output" on page 188 for the location of the VREF pin, as well as details of how to configure the pin in analog mode and to be skipped by the crossbar.



Figure 8.1. Voltage Reference Functional Block Diagram



Note that false rising edges and falling edges can be detected when the comparator is first powered on or if changes are made to the hysteresis or response time control bits. Therefore, it is recommended that the rising-edge and falling-edge flags be explicitly cleared to logic 0 a short time after the comparator is enabled or its mode bits have been changed.

SFR Definition 9.1. CPT0CN: Comparator0 Control

Bit	7	6	5	4	3	2	1	0
Name	CP0EN	CP0OUT	CP0RIF	CP0FIF	CP0H	YP[1:0]	CP0H	/N[1:0]
Туре	R/W	R	R/W	R/W	R/	W	R/	W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x9A; SFR Page = 0x00

Bit	Name	Function
7	CP0EN	Comparator0 Enable Bit.
		0: Comparator0 Disabled.
		1: Comparator0 Enabled.
6	CP0OUT	Comparator0 Output State Flag.
		0: Voltage on CP0+ < CP0–.
		1: Voltage on CP0+ > CP0
5	CP0RIF	Comparator0 Rising-Edge Flag. Must be cleared by software.
		0: No Comparator0 Rising Edge has occurred since this flag was last cleared.
		1: Comparator0 Rising Edge has occurred.
4	CP0FIF	Comparator0 Falling-Edge Flag. Must be cleared by software.
		0: No Comparator0 Falling-Edge has occurred since this flag was last cleared.
		1: Comparator0 Falling-Edge has occurred.
3:2	CP0HYP[1:0]	Comparator0 Positive Hysteresis Control Bits.
		00: Positive Hysteresis Disabled.
		01: Positive Hysteresis = 5 mV.
		10: Positive Hysteresis = 10 mV.
		11: Positive Hysteresis = 20 mV.
1:0	CP0HYN[1:0]	Comparator0 Negative Hysteresis Control Bits.
		00: Negative Hysteresis Disabled.
		01: Negative Hysteresis = 5 mV.
		10: Negative Hysteresis = 10 mV.
		11: Negative Hysteresis = 20 mV.



SFR Definition 13.2. SFRPAGE: SFR Page

Bit	7	6	5	4	3	2	1	0			
Name		SFRPAGE[7:0]									
Туре		R/W									
Reset	0	0	0	0	0	0	0	0			

SFR Address = 0xA7; SFR Page = All Pages

Bit	Name	Function
7:0	SFRPAGE[7:0]	SFR Page Bits.
		Represents the SFR Page the C8051 core uses when reading or modifying SFRs.
		Write: Sets the SFR Page.
		Read: Byte is the SFR page the C8051 core is using.
		When enabled in the SFR Page Control Register (SFR0CN), the C8051 core will automatically switch to the SFR Page that contains the SFRs of the correspond- ing peripheral/function that caused the interrupt, and return to the previous SFR page upon return from interrupt (unless SFR Stack was altered before a return- ing from the interrupt). SFRPAGE is the top byte of the SFR Page Stack, and push/pop events of this stack are caused by interrupts (and not by reading/writ- ing to the SFRPAGE register)



Bit	7	6	5	4	3	2	1	0	
Nam	e Reserved	Reserved	CHPFEN	Reserved	Reserved	Reserved	Reserved	CHBLKW	
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Rese	et 0	0	1	0	0	0	0	0	
SFR A	ddress = 0xE	3; SFR Page	e = 0x0F						
Bit	Name		Function						
7:6	Reserved	Must Write 0	0b						
5	CHPFEN	Cache Prefe 0: Prefetch e 1: Prefetch e	ect Enable E Engine is disa Engine is ena	Bit. abled. abled.					
4:1	Reserved	Must Write 0	000b.						
0	CHBLKW	Block Write This bit allow 0: Each byte	Enable Bit. /s block write of a softwar	es to Flash n e Flash write	nemory from e is written ir f two	firmware. ndividually.			

SFR Definition 15.5. ONESHOT: Flash Oneshot Period

Bit	7	6	5	4	3	2	1	0
Name					PERIOD[3:0]			
Туре	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	1

SFR Address = 0xBE; SFR Page = 0x0F

ы	Name	Function
7:4	Unused	Read = 0000b. Write = don't care.
3:0 F	PERIOD[3:0]	Oneshot Period Control Bits. These bits limit the internal Flash read strobe width as follows. When the Flash read strobe is de-asserted, the Flash memory enters a low-power state for the remainder of the system clock cycle. These bits have no effect when the system clocks is greater than 12.5 MHz and FLRT = 0.



SFR Definition 17.2. RSTSRC: Reset Source

Bit	7	6	5	4	3	2	1	0
Name		FERROR	C0RSEF	SWRSF	WDTRSF	MCDRSF	PORSF	PINRSF
Туре	R	R	R/W	R/W	R	R/W	R/W	R
Reset	0	Varies						

SFR Address = 0xEF; SFR Page = 0x00

Bit	Name	Description	Write	Read
7	Unused	Unused.	Don't care.	0
6	FERROR	Flash Error Reset Flag.	N/A	Set to 1 if Flash read/write/erase error caused the last reset.
5	CORSEF	Comparator0 Reset Enable and Flag.	Writing a 1 enables Com- parator0 as a reset source (active-low).	Set to 1 if Comparator0 caused the last reset.
4	SWRSF	Software Reset Force and Flag.	Writing a 1 forces a sys- tem reset.	Set to 1 if last reset was caused by a write to SWRSF.
3	WDTRSF	Watchdog Timer Reset Flag.	N/A	Set to 1 if Watchdog Timer overflow caused the last reset.
2	MCDRSF	Missing Clock Detector Enable and Flag.	Writing a 1 enables the Missing Clock Detector. The MCD triggers a reset if a missing clock condition is detected.	Set to 1 if Missing Clock Detector timeout caused the last reset.
1	PORSF	Power-On/V _{DD} Monitor Reset Flag, and V _{DD} monitor Reset Enable.	Writing a 1 enables the V_{DD} monitor as a reset source. Writing 1 to this bit before the V_{DD} monitor is enabled and stabilized may cause a system reset.	Set to 1 anytime a power- on or V _{DD} monitor reset occurs. When set to 1 all other RSTSRC flags are inde- terminate.
0	PINRSF	HW Pin Reset Flag.	N/A	Set to 1 if \overline{RST} pin caused the last reset.
Note:	Do not use	read-modify-write operations on this	s register	



20.6. Special Function Registers for Accessing and Configuring Port I/O

All Port I/O are accessed through corresponding special function registers (SFRs) that are both byte addressable and bit addressable, except for P4 which is only byte addressable. When writing to a Port, the value written to the SFR is latched to maintain the output data value at each pin. When reading, the logic levels of the Port's input pins are returned regardless of the XBRn settings (i.e., even when the pin is assigned to another signal by the Crossbar, the Port register can always read its corresponding Port I/O pin). The exception to this is the execution of the read-modify-write instructions that target a Port Latch register as the destination. The read-modify-write instructions when operating on a Port SFR are the following: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ and MOV, CLR or SETB, when the destination is an individual bit in a Port SFR. For these instructions, the value of the latch register (not the pin) is read, modified, and written back to the SFR.

Ports 0–3 have a corresponding PnSKIP register which allows its individual Port pins to be assigned to digital functions or skipped by the Crossbar. All Port pins used for analog functions, GPIO, or dedicated digital functions such as the EMIF should have their PnSKIP bit set to 1.

The Port input mode of the I/O pins is defined using the Port Input Mode registers (PnMDIN). Each Port cell can be configured for analog or digital I/O. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic. The only exception to this is P4, which can only be used for digital I/O.

The output driver characteristics of the I/O pins are defined using the Port Output Mode registers (PnMD-OUT). Each Port Output driver can be configured as either open drain or push-pull. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic. The only exception to this is the SMBus (SDA, SCL) pins, which are configured as open-drain regardless of the PnMDOUT settings.

SFR Definition 20.13. P0: Port 0

Bit	7	6	5	4	3	2	1	0			
Name		P0[7:0]									
Туре		R/W									
Reset	1	1 1 1 1 1 1 1 1									

SFR Address = 0x80; SFR Page = All Pages; Bit-Addressable

Bit	Name	Description	Write	Read
7:0	P0[7:0]	Port 0 Data. Sets the Port latch logic value or reads the Port pin logic state in Port cells con- figured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P0.n Port pin is logic LOW. 1: P0.n Port pin is logic HIGH.



SFR Definition 20.16. P0SKIP: Port 0 Skip

Bit	7	6	5	4	3	2	1	0			
Name	P0SKIP[7:0]										
Туре	R/W										
Reset	0	0 0 0 0 0 0 0 0									

SFR Address = 0xD4; SFR Page = 0x0F

Bit	Name	Function
7:0	P0SKIP[7:0]	Port 0 Crossbar Skip Enable Bits.
		 These bits select Port 0 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar. 0: Corresponding P0.n pin is not skipped by the Crossbar. 1: Corresponding P0.n pin is skipped by the Crossbar.

SFR Definition 20.17. P1: Port 1

Bit	7	6	5	4	3	2	1	0			
Name		P1[7:0]									
Туре		R/W									
Reset	1	1 1 1 1 1 1 1 1									

SFR Address = 0x90; SFR Page = All Pages; Bit-Addressable

Bit	Name	Description	Write	Read
7:0	P1[7:0]	Port 1 Data. Sets the Port latch logic value or reads the Port pin logic state in Port cells con- figured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P1.n Port pin is logic LOW. 1: P1.n Port pin is logic HIGH.



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23.4.2. SMB0CN Control Register

SMB0CN is used to control the interface and to provide status information (see SFR Definition 23.2). The higher four bits of SMB0CN (MASTER, TXMODE, STA, and STO) form a status vector that can be used to jump to service routines. MASTER indicates whether a device is the master or slave during the current transfer. TXMODE indicates whether the device is transmitting or receiving data for the current byte.

STA and STO indicate that a START and/or STOP has been detected or generated since the last SMBus interrupt. STA and STO are also used to generate START and STOP conditions when operating as a master. Writing a 1 to STA will cause the SMBus interface to enter Master Mode and generate a START when the bus becomes free (STA is not cleared by hardware after the START is generated). Writing a 1 to STO while in Master Mode will cause the interface to generate a STOP and end the current transfer after the next ACK cycle. If STO and STA are both set (while in Master Mode), a STOP followed by a START will be generated.

As a receiver, writing the ACK bit defines the outgoing ACK value; as a transmitter, reading the ACK bit indicates the value received during the last ACK cycle. ACKRQ is set each time a byte is received, indicating that an outgoing ACK value is needed. When ACKRQ is set, software should write the desired outgoing value to the ACK bit before clearing SI. A NACK will be generated if software does not write the ACK bit before clearing SI. SDA will reflect the defined ACK value immediately following a write to the ACK bit; however SCL will remain low until SI is cleared. If a received slave address is not acknowledged, further slave events will be ignored until the next START is detected.

The ARBLOST bit indicates that the interface has lost an arbitration. This may occur anytime the interface is transmitting (master or slave). A lost arbitration while operating as a slave indicates a bus error condition. ARBLOST is cleared by hardware each time SI is cleared.

The SI bit (SMBus Interrupt Flag) is set at the beginning and end of each transfer, after each byte frame, or when an arbitration is lost; see Table 23.3 for more details.

Important Note About the SI Bit: The SMBus interface is stalled while SI is set; thus SCL is held low, and the bus is stalled until software clears SI.



27. Timers

Each MCU includes six counter/timers: two are 16-bit counter/timers compatible with those found in the standard 8051, and the other four are 16-bit auto-reload timers for use with the ADC, SMBus, or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. Timer 2 and Timer 3 offer 16-bit and split 8-bit timer functionality with auto-reload. Timer 4 and Timer 5 have 16-bit auto reload and capture and can also produce a 50% duty-cycle square wave (toggle output) at an general purpose port pin.

Timer 0 and Timer 1 Modes	Timer 2 and 3 Modes	Timer 4 and 5 Modes
13-bit counter/timer	16-bit timer with auto-reload	16-bit timer with auto-reload
16-bit counter/timer		
8-bit counter/timer with auto-reload	Two 8-bit timers with auto-reload	16-bit counter/timer with capture
Two 8-bit counter/timers (Timer 0 only)		Toggle Output

Timers 0 and 1 may be clocked by one of five sources, determined by the Timer Mode Select bits (T1M– T0M) and the Clock Scale bits (SCA1–SCA0). The Clock Scale bits define a pre-scaled clock from which Timer 0 and/or Timer 1 may be clocked (See SFR Definition 27.1 for pre-scaled clock selection).Timer 0/1 may then be configured to use this pre-scaled clock signal or the system clock.

Timer 2 and Timer 3 may be clocked by the system clock, the system clock divided by 12, or the external oscillator clock source divided by 8.

Timer 4 and Timer 5 may be clocked by the system clock, system clock divided by 2 or 12, or the external oscillator clock source divided by 8.

Timers 0, 1, 4, and 5 may also be operated as counters. When functioning as a counter, a counter/timer register is incremented on each high-to-low transition at the selected input pin. Events with a frequency of up to one-fourth the system clock frequency can be counted. The input signal need not be periodic, but it should be held at a given level for at least two full system clock cycles to ensure the level is properly sampled.



27.2. Timer 2

Timer 2 is a 16-bit timer formed by two 8-bit SFRs: TMR2L (low byte) and TMR2H (high byte). Timer 2 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T2SPLIT bit (TMR2CN.3) defines the Timer 2 operation mode.

Timer 2 may be clocked by the system clock, the system clock divided by 12, or the external oscillator source divided by 8. The external clock mode is ideal for real-time clock (RTC) functionality, where the internal oscillator drives the system clock while Timer 2 (and/or the PCA) is clocked by an external precision oscillator. Note that the external oscillator source divided by 8 is synchronized with the system clock.

27.2.1. 16-bit Timer with Auto-Reload

When T2SPLIT (TMR2CN.3) is zero, Timer 2 operates as a 16-bit timer with auto-reload. Timer 2 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 2 reload registers (TMR2RLH and TMR2RLL) is loaded into the Timer 2 register as shown in Figure 27.4, and the Timer 2 High Byte Overflow Flag (TMR2CN.7) is set. If Timer 2 interrupts are enabled (if IE.5 is set), an interrupt will be generated on each Timer 2 overflow. Additionally, if Timer 2 interrupts are enabled and the TF2LEN bit is set (TMR2CN.5), an interrupt will be generated each time the lower 8 bits (TMR2L) overflow from 0xFF to 0x00.



Figure 27.4. Timer 2 16-Bit Mode Block Diagram

27.2.2. 8-bit Timers with Auto-Reload

When T2SPLIT is set, Timer 2 operates as two 8-bit timers (TMR2H and TMR2L). Both 8-bit timers operate in auto-reload mode as shown in Figure 27.5. TMR2RLL holds the reload value for TMR2L; TMR2RLH holds the reload value for TMR2H. The TR2 bit in TMR2CN handles the run control for TMR2H. TMR2L is always running when configured for 8-bit Mode.

Each 8-bit timer may be configured to use SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. The Timer 2 Clock Select bits (T2MH and T2ML in CKCON) select either SYSCLK or the clock defined by the Timer 2 External Clock Select bit (T2XCLK in TMR2CN), as follows:

T2MH	T2XCLK	TMR2H Clock Source
0	0	SYSCLK/12
0	1	External Clock/8
1	Х	SYSCLK

T2ML	T2XCLK	TMR2L Clock Source
0	0	SYSCLK/12
0	1	External Clock/8
1	Х	SYSCLK





Figure 27.11. Timer 4 and 5 Auto Reload and Toggle Mode Block Diagram

27.4.4. Toggle Output Mode

Timers 4 and 5 have the capability to toggle the state of their respective output port pins (T4 or T5) to produce a 50% duty cycle waveform output. The port pin state will change upon the overflow or underflow of the respective timer (depending on whether the timer is counting *up* or *down*). The toggle frequency is determined by the clock source of the timer and the values loaded into TMRnCAPH and TMRnCAPL. When counting down, the auto-reload value for the timer is 0xFFFF, and underflow will occur when the value in the timer matches the value stored in TMRnCAPH:TMRCAPL. When counting up, the auto-reload value for the timer is TMRnCAPH:TMRCAPL, and overflow will occur when the value in the timer transitions from 0xFFFF to the reload value.

To output a square wave, the timer is placed in reload mode (the Capture/Reload Select Bit in TMRnCN and the Timer/Counter Select Bit in TMRnCN are cleared to 0). The timer output is enabled by setting the Timer Output Enable Bit in TMRnCF to 1. The timer should be configured via the timer clock source and reload/underflow values such that the timer overflow/underflows at 1/2 the desired output frequency. The port pin assigned by the crossbar as the timer's output pin should be configured as a digital output (see **Section "20. Port Input/Output" on page 188**). Setting the timer's Run Bit (TRn) to 1 will start the toggle of the pin. A Read/Write of the Timer's Toggle Output State Bit (TMRnCF.2) is used to read the state of the toggle output, or to force a value of the output. This is useful when it is desired to start the toggle of a pin in a known state, or to force the pin into a desired state when the toggle mode is halted.

$$F_{sq} = \frac{F_{TCLK}}{2 \times (65536 - TMRnCAP)}$$

Equation 27.1. Square Wave Frequency



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Figure 29.8. PCA1 8-Bit PWM Mode Diagram



SFR Definition 29.7. PCA1CPLn: PCA1 Capture Module Low Byte

Bit	7	6	5	4	3	2	1	0
Name				PCA1C	Pn[7:0]			
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: PCA1CPL6 = 0xFB, PCA1CPL7 = 0xE9, PCA1CPL8 = 0xEB, PCA1CPL9 = 0xED, PCA1CPL10 = 0xFD, PCA1CPL11 = 0xCE; SFR Page (all registers) = 0x10

Bit	Name	Function				
7:0	PCA1CPn[7:0]	PCA1 Capture Module Low Byte.				
		The PCA1CPLn register holds the low byte (LSB) of the 16-bit capture module n. This register address also allows access to the low byte of the corresponding PCA1 channel's auto-reload value for 9, 10, or 11-bit PWM mode. The ARSEL1 bit in register PCA1PWM controls which register is accessed.				
Note:	te: A write to this register will clear the module's ECOM1n bit to a 0.					

SFR Definition 29.8. PCA1CPHn: PCA1 Capture Module High Byte

Bit	7	6	5	4	3	2	1	0
Name				PCA1C	Pn[15:8]			
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: PCA1CPH6 = 0xFC, PCA1CPH7 = 0xEA, PCA1CPH8 = 0xEC, PCA1CPH9 = 0xEE, PCA1CPH10 = 0xFE, PCA1CPH11 = 0xCF; SFR Page (all registers) = 0x10

Bit	Name	Function				
7:0	PCA1CPn[15:8]	PCA1 Capture Module High Byte.				
		The PCA1CPHn register holds the high byte (MSB) of the 16-bit capture module n. This register address also allows access to the high byte of the corresponding PCA1 channel's auto-reload value for 9, 10, or 11-bit PWM mode. The ARSEL1 bit in register PCA1PWM controls which register is accessed.				
Note	ote: A write to this register will set the module's ECOM1n bit to a 1.					



DOCUMENT CHANGE LIST

Revision 0.1 to Revision 1.0

Updated all specification TBDs

Clarified and corrected text throughout the document.

Revision 1.0 to Revision 1.1

- Updated "Ordering Information" on page 22 to include -A (Automotive) devices and automotive qualification information.
- Updated supply current related specifications throughout "5. Electrical Characteristics".
- Updated SFR Definition 8.1 to change VREF high setting to 2.20 V from 2.25 V.
- Updated Table 5.13 on page 53 and Figure 9.1 on Page 77 to indicate that Comparators are powered from V_{IO} and not V_{DDA}.
- Updated the Gain Table in "Calculating the Gain Value" on page 60 to fix the ADC0GNH Value in the last row.
- Updated Table 11.1 on page 94 with correct timing for all branch instructions, MOVC, and CPL A.
- Updated "Programming The Flash Memory" on page 138 to clarify behavior of 8-bit MOVX instructions and when writing/erasing Flash.
- Updated SFR Definition 15.3 (FLSCL) to include FLEWT bit definition. This bit must be set before writing or erasing Flash. Also updated Table 5.5 on page 48 to reflect new Flash Write and Erase timing.
- Updated "17.7. Flash Error Reset" with an additional cause of a Flash Error reset.
- Updated "20.1. Port I/O Modes of Operation" to remove note regarding interfacing to voltages above VIO.
- Updated "23. SMBus" to remove all hardware ACK features, including SMB0ADM and SMB0ADR SFRs.
- Updated "24.3.2. Data Reception" to clarify UART receive FIFO behavior.
- Updated SFR Definition 24.1 (SCON0) to correct SFR Page to 0x00 from All Pages.
- Various formatting changes and corrections throughout the document.

Note: All items from the C8051F58x/59x Errata dated July 1, 2009 are incorporated into this data sheet.

Revision 1.1 to Revision 1.2

- Updated "1. System Overview" with a voltage range specification for the internal oscillator.
- Updated Table 5.6, "Internal High-Frequency Oscillator Electrical Characteristics," on page 49 with new conditions for the internal oscillator accuracy. The internal oscillator accuracy is dependent on the operating voltage range.
- Updated "5. Electrical Characteristics" to remove the internal oscillator curve across temperature diagram.
- Updated Figure 6.4 with new timing diagram when using CNVSTR pin.
- Updated SFR Definition 8.1 (REF0CN) with oscillator suspend requirement for ZTCEN.
- Fixed incorrect cross references in "9. Comparators" .
- Updated SFR Definition 10.1 (REG0CN) with a new definition for Bit 6. The bit 6 reset value is 1b and must be written to 1b.
- Updated SFR Definition 12.1 (PSBANK) with correct reset value.
- Updated "16.3. Suspend Mode" with note regarding ZTCEN.

