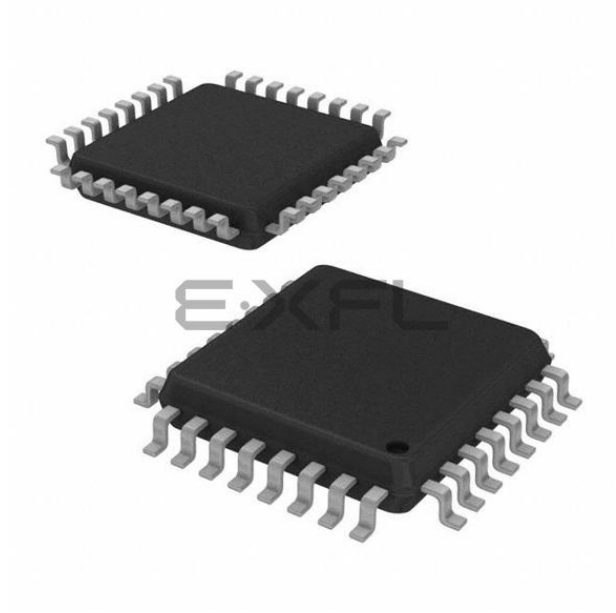

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Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 25x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f587-iq

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been accumulated. Similarly, the Window Comparator will not compare the result to the greater-than and less-than registers until “repeat count” conversions have been accumulated.

Note: When using Burst Mode, care must be taken to issue a convert start signal no faster than once every four SYSCLK periods. This includes external convert start signals.

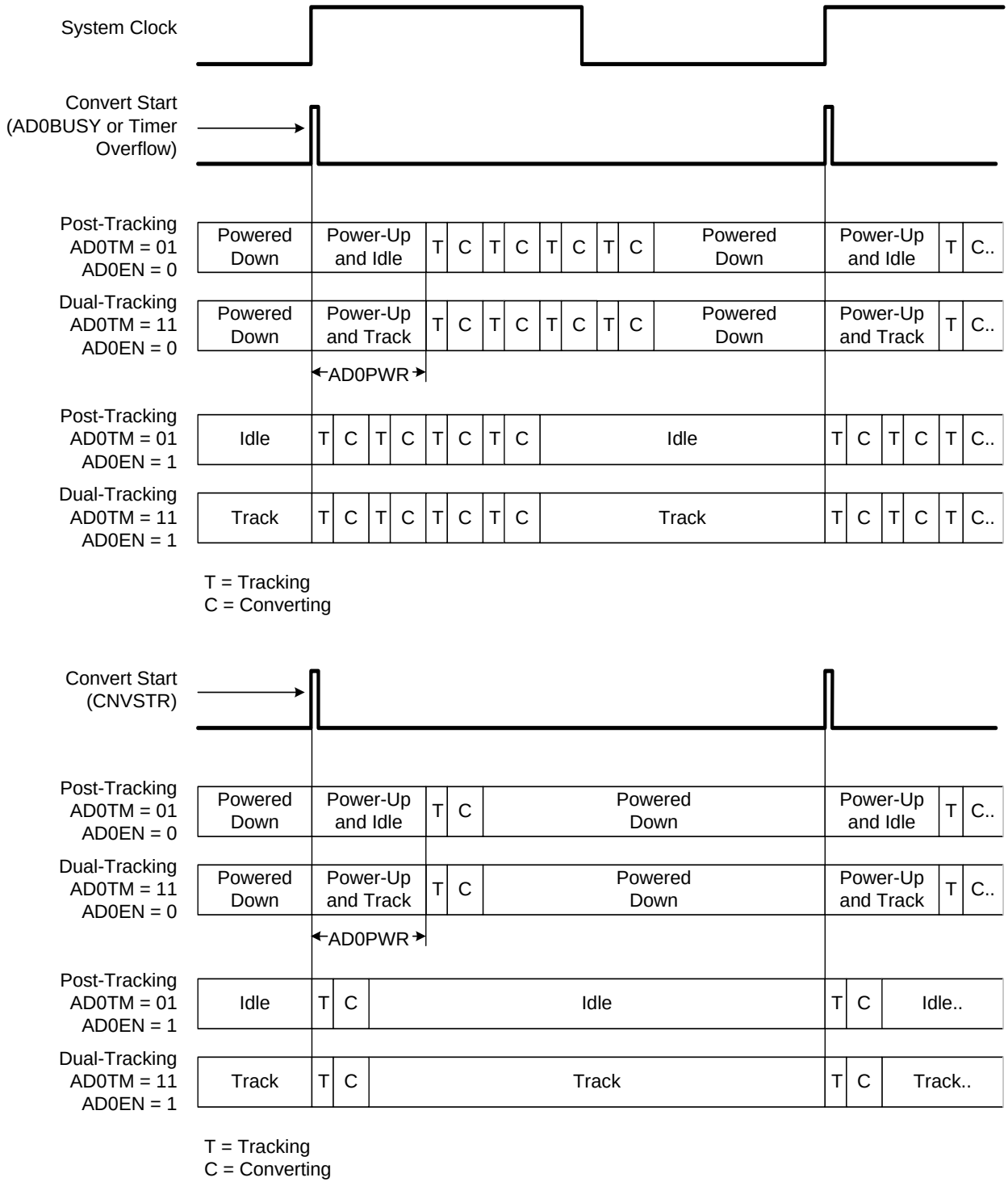


Figure 6.4. 12-Bit ADC Burst Mode Example With Repeat Count Set to 4

8. Voltage Reference

The Voltage reference multiplexer on the C8051F58x/F59x devices is configurable to use an externally connected voltage reference, the on-chip reference voltage generator routed to the VREF pin, or the V_{DD} power supply voltage (see Figure 8.1). The REFSL bit in the Reference Control register (REF0CN, SFR Definition 8.1) selects the reference source for the ADC. For an external source or the on-chip reference, REFSL should be set to 0 to select the VREF pin. To use V_{DD} as the reference source, REFSL should be set to 1.

The BIASE bit enables the internal voltage bias generator, which is used by the ADC, Temperature Sensor, and internal oscillator. This bias is automatically enabled when any peripheral which requires it is enabled, and it does not need to be enabled manually. The bias generator may be enabled manually by writing a 1 to the BIASE bit in register REF0CN. The electrical specifications for the voltage reference circuit are given in Table 5.12.

The on-chip voltage reference circuit consists of a temperature stable bandgap voltage reference generator and a gain-of-two output buffer amplifier. The output voltage is selectable between 1.5 V and 2.25 V. The on-chip voltage reference can be driven on the VREF pin by setting the REFBE bit in register REF0CN to a 1. The maximum load seen by the VREF pin must be less than 200 µA to GND. Bypass capacitors of 0.1 µF and 4.7 µF are recommended from the VREF pin to GND. If the on-chip reference is not used, the REFBE bit should be cleared to 0. Electrical specifications for the on-chip voltage reference are given in Table 5.12.

Important Note about the VREF Pin: When using either an external voltage reference or the on-chip reference circuitry, the VREF pin should be configured as an analog pin and skipped by the Digital Crossbar. Refer to Section “20. Port Input/Output” on page 188 for the location of the VREF pin, as well as details of how to configure the pin in analog mode and to be skipped by the crossbar.

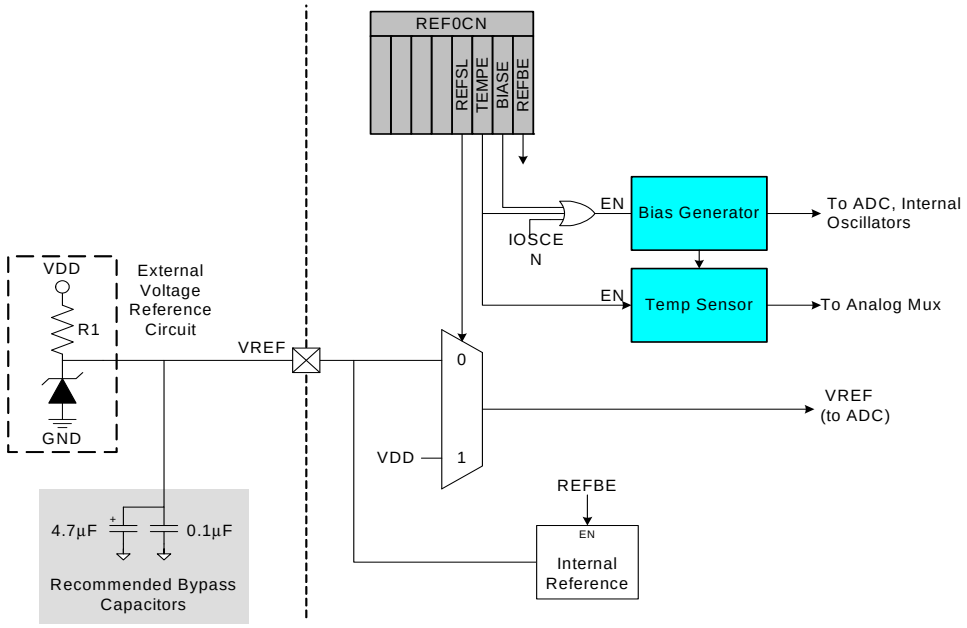


Figure 8.1. Voltage Reference Functional Block Diagram

SFR Definition 9.7. CPT0MX: Comparator0 MUX Selection

Bit	7	6	5	4	3	2	1	0
Name	CMX0N[3:0]				CMX0P[3:0]			
Type	R/W				R/W			
Reset	0	1	1	1	0	1	1	1

SFR Address = 0x9C; SFR Page = 0x00

Bit	Name	Function
7:4	CMX0N[3:0]	**Comparator0 Negative Input MUX Selection.**
		0000: P0.1
		0001: P0.3
		0010: P0.5
		0011: P0.7
		0100: P1.1
		0101: P1.3
		0110: P1.5
		0111: P1.7
		1000: P2.1
		1001: P2.3
		1010: P2.5
		1011: P2.7
		1100–1111: None
3:0	CMX0P[3:0]	**Comparator0 Positive Input MUX Selection.**
		0000: P0.0
		0001: P0.2
		0010: P0.4
		0011: P0.6
		0100: P1.0
		0101: P1.2
		0110: P1.4
		0111: P1.6
		1000: P2.0
		1001: P2.2
		1010: P2.4
		1011: P2.6
		1100–1111: None

SFR Definition 11.1. DPL: Data Pointer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	DPL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x82; SFR Page = All Pages

Bit	Name	Function
7:0	DPL[7:0]	**Data Pointer Low.** The DPL register is the low byte of the 16-bit DPTR. DPTR is used to access indirectly addressed Flash memory or XRAM.

SFR Definition 11.2. DPH: Data Pointer High Byte

Bit	7	6	5	4	3	2	1	0
Name	DPH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x83; SFR Page = All Pages

Bit	Name	Function
7:0	DPH[7:0]	**Data Pointer High.** The DPH register is the high byte of the 16-bit DPTR. DPTR is used to access indirectly addressed Flash memory or XRAM.

SFR Definition 14.2. IP: Interrupt Priority

Bit	7	6	5	4	3	2	1	0
Name		PSPI0	PT2	PS0	PT1	PX1	PT0	PX0
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

SFR Address = 0xB8; Bit-Addressable; SFR Page = All Pages

Bit	Name	Function
7	Unused	Read = 1b, Write = Don't Care.
6	PSPI0	**Serial Peripheral Interface (SPI0) Interrupt Priority Control.** This bit sets the priority of the SPI0 interrupt. 0: SPI0 interrupt set to low priority level. 1: SPI0 interrupt set to high priority level.
5	PT2	**Timer 2 Interrupt Priority Control.** This bit sets the priority of the Timer 2 interrupt. 0: Timer 2 interrupt set to low priority level. 1: Timer 2 interrupt set to high priority level.
4	PS0	**UART0 Interrupt Priority Control.** This bit sets the priority of the UART0 interrupt. 0: UART0 interrupt set to low priority level. 1: UART0 interrupt set to high priority level.
3	PT1	**Timer 1 Interrupt Priority Control.** This bit sets the priority of the Timer 1 interrupt. 0: Timer 1 interrupt set to low priority level. 1: Timer 1 interrupt set to high priority level.
2	PX1	**External Interrupt 1 Priority Control.** This bit sets the priority of the External Interrupt 1 interrupt. 0: External Interrupt 1 set to low priority level. 1: External Interrupt 1 set to high priority level.
1	PT0	**Timer 0 Interrupt Priority Control.** This bit sets the priority of the Timer 0 interrupt. 0: Timer 0 interrupt set to low priority level. 1: Timer 0 interrupt set to high priority level.
0	PX0	**External Interrupt 0 Priority Control.** This bit sets the priority of the External Interrupt 0 interrupt. 0: External Interrupt 0 set to low priority level. 1: External Interrupt 0 set to high priority level.

SFR Definition 14.3. EIE1: Extended Interrupt Enable 1

Bit	7	6	5	4	3	2	1	0
Name	ELIN0	ET3	ECP1	ECP0	EPCA0	EADC0	EWADC0	ESMB0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE6; SFR Page = All Pages

Bit	Name	Function
7	ELIN0	**Enable LIN0 Interrupt.** This bit sets the masking of the LIN0 interrupt. 0: Disable LIN0 interrupts. 1: Enable interrupt requests generated by the LIN0INT flag.
6	ET3	**Enable Timer 3 Interrupt.** This bit sets the masking of the Timer 3 interrupt. 0: Disable Timer 3 interrupts. 1: Enable interrupt requests generated by the TF3L or TF3H flags.
5	ECP1	**Enable Comparator1 (CP1) Interrupt.** This bit sets the masking of the CP1 interrupt. 0: Disable CP1 interrupts. 1: Enable interrupt requests generated by the CP1RIF or CP1FIF flags.
4	ECP0	**Enable Comparator0 (CP0) Interrupt.** This bit sets the masking of the CP0 interrupt. 0: Disable CP0 interrupts. 1: Enable interrupt requests generated by the CP0RIF or CP0FIF flags.
3	EPCA0	**Enable Programmable Counter Array (PCA0) Interrupt.** This bit sets the masking of the PCA0 interrupts. 0: Disable all PCA0 interrupts. 1: Enable interrupt requests generated by PCA0.
2	EADC0	**Enable ADC0 Conversion Complete Interrupt.** This bit sets the masking of the ADC0 Conversion Complete interrupt. 0: Disable ADC0 Conversion Complete interrupt. 1: Enable interrupt requests generated by the AD0INT flag.
1	EWADC0	**Enable Window Comparison ADC0 Interrupt.** This bit sets the masking of ADC0 Window Comparison interrupt. 0: Disable ADC0 Window Comparison interrupt. 1: Enable interrupt requests generated by ADC0 Window Compare flag (AD0WINT).
0	ESMB0	**Enable SMBus (SMB0) Interrupt.** This bit sets the masking of the SMB0 interrupt. 0: Disable all SMB0 interrupts. 1: Enable interrupt requests generated by SMB0.

SFR Definition 15.2. FLKEY: Flash Lock and Key

Bit	7	6	5	4	3	2	1	0
Name	FLKEY[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB7; SFR Page = All Pages

Bit	Name	Function
7:0	FLKEY[7:0]	**Flash Lock and Key Register.** Write: This register provides a lock and key function for Flash erasures and writes. Flash writes and erases are enabled by writing 0xA5 followed by 0xF1 to the FLKEY register. Flash writes and erases are automatically disabled after the next write or erase is complete. If any writes to FLKEY are performed incorrectly, or if a Flash write or erase operation is attempted while these operations are disabled, the Flash will be permanently locked from writes or erasures until the next device reset. If an application never writes to Flash, it can intentionally lock the Flash by writing a non-0xA5 value to FLKEY from software. Read: When read, bits 1–0 indicate the current Flash lock state. 00: Flash is write/erase locked. 01: The first key code has been written (0xA5). 10: Flash is unlocked (writes/erases allowed). 11: Flash writes/erases disabled until the next reset.

SFR Definition 15.4. CCH0CN: Cache Control

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	CHPFEN	Reserved	Reserved	Reserved	Reserved	CHBLKW
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

SFR Address = 0xE3; SFR Page = 0x0F

Bit	Name	Function
7:6	Reserved	Must Write 00b
5	CHPFEN	**Cache Prefect Enable Bit.** 0: Prefetch engine is disabled. 1: Prefetch engine is enabled.
4:1	Reserved	Must Write 0000b.
0	CHBLKW	**Block Write Enable Bit.** This bit allows block writes to Flash memory from firmware. 0: Each byte of a software Flash write is written individually. 1: Flash bytes are written in groups of two.

SFR Definition 15.5. ONESHOT: Flash Oneshot Period

Bit	7	6	5	4	3	2	1	0
Name					PERIOD[3:0]			
Type	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	1

SFR Address = 0xBE; SFR Page = 0x0F

Bit	Name	Function
7:4	Unused	Read = 0000b. Write = don't care.
3:0	PERIOD[3:0]	**Oneshot Period Control Bits.** These bits limit the internal Flash read strobe width as follows. When the Flash read strobe is de-asserted, the Flash memory enters a low-power state for the remainder of the system clock cycle. These bits have no effect when the system clocks is greater than 12.5 MHz and FLRT = 0. $FLASH_{RDMAX} = 5ns + (PERIOD \times 5ns)$

18.6.1.2. 8-bit MOVX without Bank Select: EMI0CF[4:2] = 101 or 111

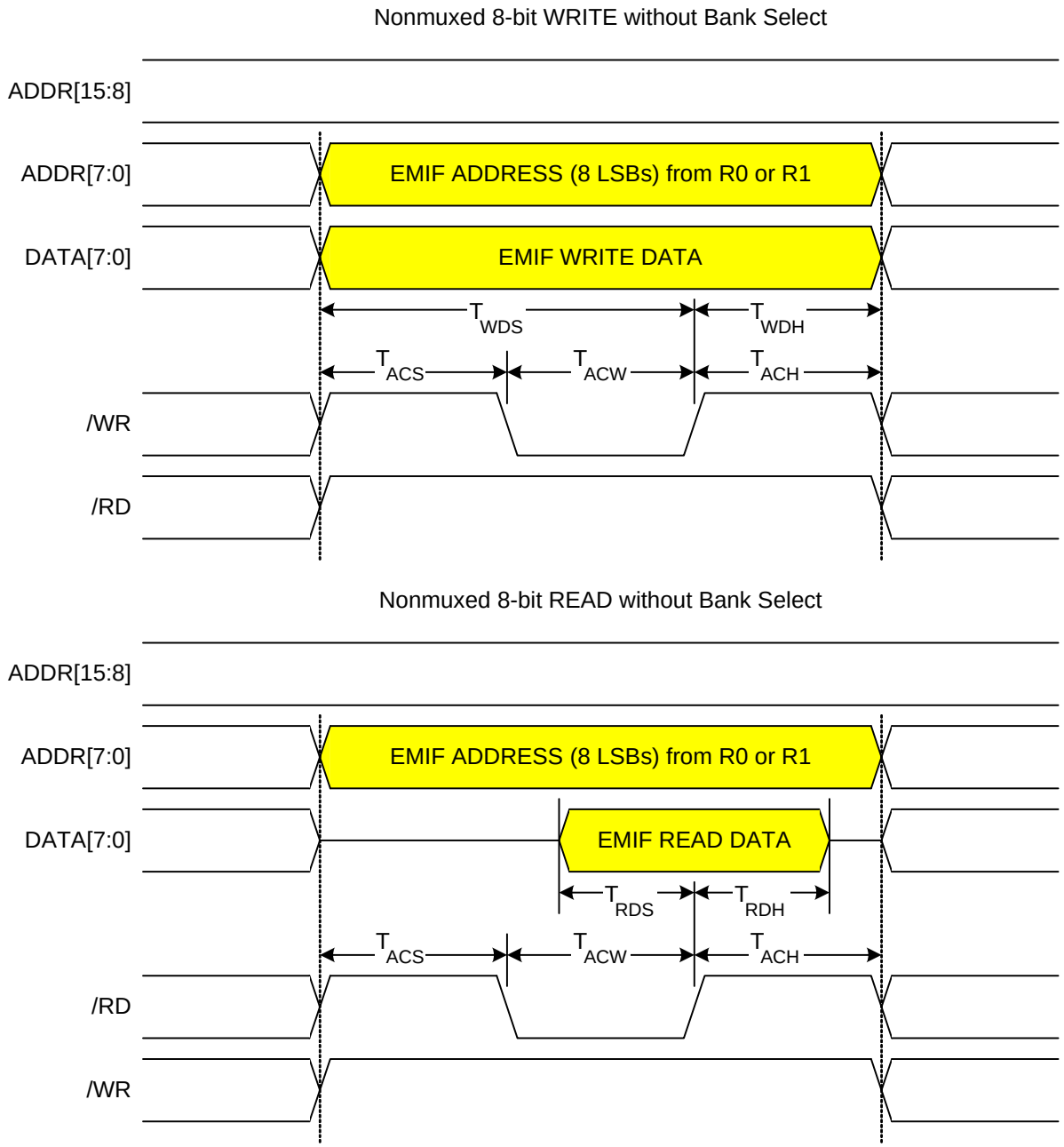


Figure 18.5. Non-multiplexed 8-bit MOVX without Bank Select Timing

LIN Register Definition 21.4. LIN0DTn: LIN0 Data Byte n

Bit	7	6	5	4	3	2	1	0
Name	DATAn[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

Indirect Address: LIN0DT1 = 0x00, LIN0DT2 = 0x01, LIN0DT3 = 0x02, LIN0DT4 = 0x03, LIN0DT5 = 0x04, LIN0DT6 = 0x05, LIN0DT7 = 0x06, LIN0DT8 = 0x07

Bit	Name	Function
7:0	DATAn[7:0]	**LIN Data Byte n.** Serial Data Byte that is received or transmitted across the LIN interface.

LIN Register Definition 21.6. LIN0ST: LIN0 Status Register

Bit	7	6	5	4	3	2	1	0
Name	ACTIVE	IDLTOUT	ABORT	DTREQ	LININT	ERROR	WAKEUP	DONE
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Indirect Address = 0x09

Bit	Name	Function
7	ACTIVE	**LIN Active Indicator Bit.** 0: No transmission activity detected on the LIN bus. 1: Transmission activity detected on the LIN bus.
6	IDLT	**Bus Idle Timeout Bit. (slave mode only)** 0: The bus has not been idle for four seconds. 1: No bus activity has been detected for four seconds, but the bus is not yet in Sleep mode.
5	ABORT	**Aborted Transmission Bit. (slave mode only)** 0: The current transmission has not been interrupted or stopped. This bit is reset to 0 after receiving a SYNCH BREAK that does not interrupt a pending transmission. 1: New SYNCH BREAK detected before the end of the last transmission or the STOP bit (LIN0CTRL.7) has been set.
4	DTREQ	**Data Request Bit. (slave mode only)** 0: Data identifier has not been received. 1: Data identifier has been received.
3	LININT	**Interrupt Request Bit.** 0: An interrupt is not pending. This bit is cleared by setting RSTINT (LIN0CTRL.3) 1: There is a pending LIN0 interrupt.
2	ERROR	**Communication Error Bit.** 0: No error has been detected. This bit is cleared by setting RSTERR (LIN0CTRL.2) 1: An error has been detected.
1	WAKEUP	**Wakeup Bit.** 0: A wakeup signal is not being transmitted and has not been received. 1: A wakeup signal is being transmitted or has been received
0	DONE	**Transmission Complete Bit.** 0: A transmission is not in progress or has not been started. This bit is cleared at the start of a transmission. 1: The current transmission is complete.

26.5. Serial Clock Phase and Polarity

Four combinations of serial clock phase and polarity can be selected using the clock control bits in the SPI0 Configuration Register (SPI0CFG). The CKPHA bit (SPI0CFG.5) selects one of two clock phases (edge used to latch the data). The CKPOL bit (SPI0CFG.4) selects between an active-high or active-low clock. Both master and slave devices must be configured to use the same clock phase and polarity. SPI0 should be disabled (by clearing the SPIEN bit, SPI0CN.0) when changing the clock phase or polarity. The clock and data line relationships for master mode are shown in Figure 26.5. For slave mode, the clock and data relationships are shown in Figure 26.6 and Figure 26.7. CKPHA must be set to 0 on both the master and slave SPI when communicating between two of the following devices: C8051F04x, C8051F06x, C8051F12x, C8051F31x, C8051F32x, and C8051F33x.

The SPI0 Clock Rate Register (SPI0CKR) as shown in SFR Definition 26.3 controls the master mode serial clock frequency. This register is ignored when operating in slave mode. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency or 12.5 MHz, whichever is slower. When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS (in 4-wire slave mode), and the serial input data synchronously with the slave's system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the slave's system clock.

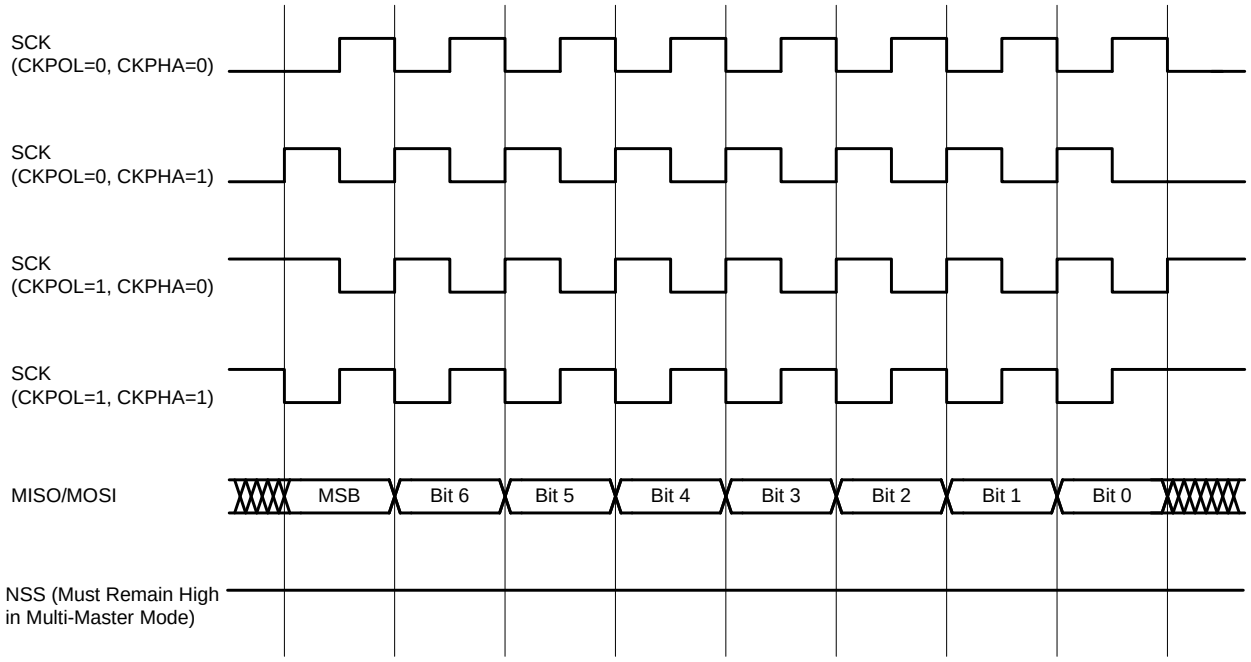


Figure 26.5. Master Mode Data/Clock Timing

SFR Definition 27.4. TL0: Timer 0 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8A; SFR Page = All Pages

Bit	Name	Function
7:0	TL0[7:0]	**Timer 0 Low Byte.** The TL0 register is the low byte of the 16-bit Timer 0.

SFR Definition 27.5. TL1: Timer 1 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8B; SFR Page = All Pages

Bit	Name	Function
7:0	TL1[7:0]	**Timer 1 Low Byte.** The TL1 register is the low byte of the 16-bit Timer 1.

SFR Definition 27.8. TMR2CN: Timer 2 Control

Bit	7	6	5	4	3	2	1	0
Name	TF2H	TF2L	TF2LEN	TF2CEN	T2SPLIT	TR2		T2XCLK
Type	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC8; Bit-Addressable; SFR Page = 0x00

Bit	Name	Function
7	TF2H	**Timer 2 High Byte Overflow Flag.** Set by hardware when the Timer 2 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 2 overflows from 0xFFFF to 0x0000. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF2L	**Timer 2 Low Byte Overflow Flag.** Set by hardware when the Timer 2 low byte overflows from 0xFF to 0x00. TF2L will be set when the low byte overflows regardless of the Timer 2 mode. This bit is not automatically cleared by hardware.
5	TF2LEN	**Timer 2 Low Byte Interrupt Enable.** When set to 1, this bit enables Timer 2 Low Byte interrupts. If Timer 2 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 2 overflows.
4	TF2CEN	**Timer 2 Capture Mode Enable.** 0: Timer 2 Capture Mode is disabled. 1: Timer 2 Capture Mode is enabled.
3	T2SPLIT	**Timer 2 Split Mode Enable.** When this bit is set, Timer 2 operates as two 8-bit timers with auto-reload. 0: Timer 2 operates in 16-bit auto-reload mode. 1: Timer 2 operates as two 8-bit auto-reload timers.
2	TR2	**Timer 2 Run Control.** Timer 2 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR2H only; TMR2L is always enabled in split mode.
1	Unused	Read = 0b; Write = Don't Care
0	T2XCLK	**Timer 2 External Clock Select.** This bit selects the external clock source for Timer 2. If Timer 2 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 2 Clock Select bits (T2MH and T2ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 0: Timer 2 clock is the system clock divided by 12. 1: Timer 2 clock is the external clock divided by 8 (synchronized with SYSCLK).

29. Programmable Counter Array 1 (PCA1)

The Programmable Counter Array (PCA1) provides enhanced timer functionality while requiring less CPU intervention than the standard 8051 counter/timers. PCA1 consists of a dedicated 16-bit counter/timer and six 16-bit capture/compare modules. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the Crossbar to Port I/O when enabled. The counter/timer is driven by a programmable timebase that can select between eight sources: system clock, system clock divided by four, system clock divided by twelve, the external oscillator clock source divided by 8, Timer 0, 4, or 5 overflows, or an external clock signal on the ECI input pin. Each capture/compare module may be configured to operate independently in one of six modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, 8 to 11-Bit PWM, or 16-Bit PWM (each mode is described in Section “29.3. Capture/Compare Modules” on page 336). The external oscillator clock option is ideal for real-time clock (RTC) functionality, allowing PCA1 to be clocked by a precision external oscillator while the internal oscillator drives the system clock. PCA1 is configured and controlled through the system controller's Special Function Registers. The PCA1 block diagram is shown in Figure 29.1

Note: PCA0 and PCA1 are fully independent peripherals. PCA0 offers channels CEX0 - CEX5, and PCA1 offers channels CEX6-CEX11. PCA0 and PCA1 are identical, except that PCA0 Module 5 may be used as a watchdog timer.

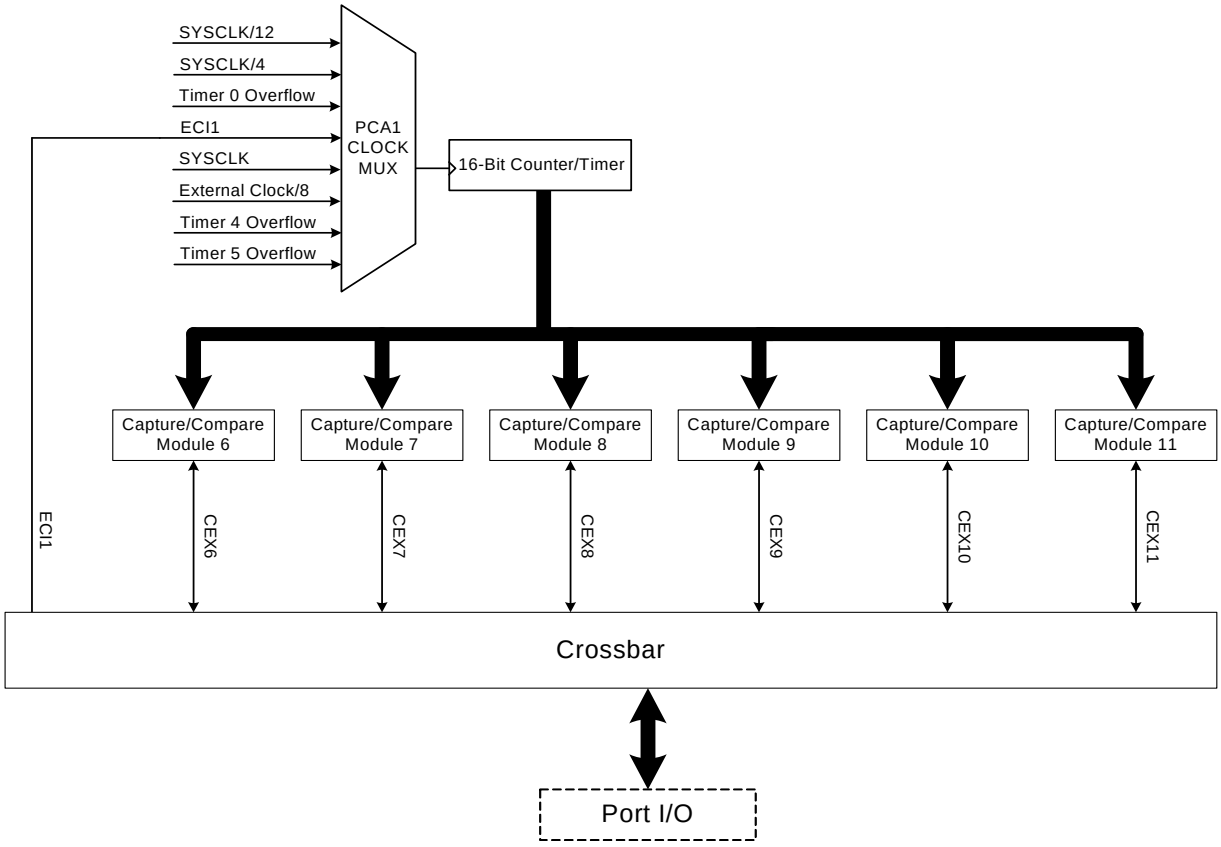


Figure 29.1. PCA1 Block Diagram

29.1. PCA1 Counter/Timer

The 16-bit PCA1 counter/timer consists of two 8-bit SFRs: PCA1L and PCA1H. PCA1H is the high byte (MSB) of the 16-bit counter/timer and PCA1L is the low byte (LSB). Reading PCA1L automatically latches the value of PCA1H into a “snapshot” register; the following PCA1H read accesses this “snapshot” register. **Reading the PCA1L Register first guarantees an accurate reading of the entire 16-bit PCA1 counter.** Reading PCA1H or PCA1L does not disturb the counter operation. The CPS12–CPS10 bits in the PCA1MD register select the timebase for the counter/timer as shown in Table 29.1.

When the counter/timer overflows from 0xFFFF to 0x0000, the Counter Overflow Flag (CF1) in PCA1MD is set to logic 1 and an interrupt request is generated if CF1 interrupts are enabled. Setting the ECF1 bit in PCA1MD to logic 1 enables the CF1 flag to generate an interrupt request. The CF1 bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Clearing the CIDL1 bit in the PCA1MD register allows the PCA1 to continue normal operation while the CPU is in Idle mode.

Table 29.1. PCA1 Timebase Input Options

CPS12	CPS11	CPS10	Timebase
0	0	0	System clock divided by 12.
0	0	1	System clock divided by 4.
0	1	0	Timer 0 overflow.
0	1	1	High-to-low transitions on ECI1 (max rate = system clock divided by 4).
1	0	0	System clock.
1	0	1	External oscillator source divided by 8.*
1	1	0	Timer 4 Overflow.
1	1	1	Timer 5 Overflow.
***Note:** External oscillator source divided by 8 is synchronized with the system clock.			

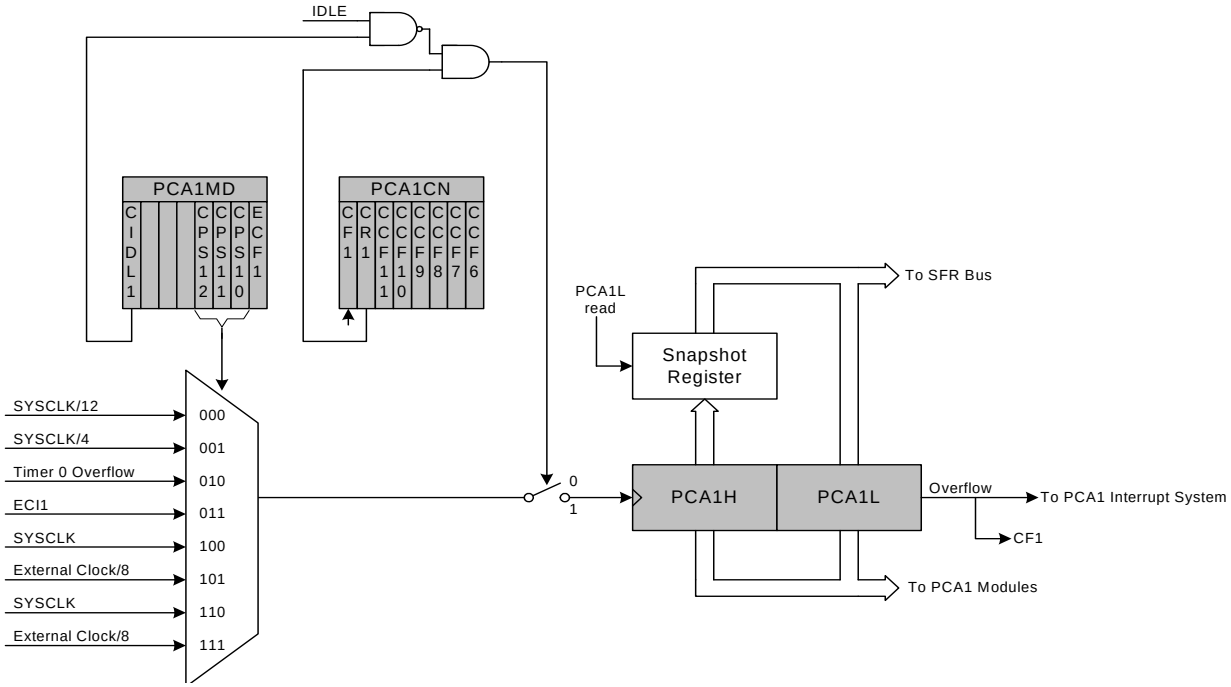


Figure 29.2. PCA1 Counter/Timer Block Diagram

30.2. C2 Pin Sharing

The C2 protocol allows the C2 pins to be shared with user functions so that in-system debugging and Flash programming may be performed. This is possible because C2 communication is typically performed when the device is in the halt state, where all on-chip peripherals and user software are stalled. In this halted state, the C2 interface can safely ‘borrow’ the C2CK (RST) and C2D pins. In most applications, external resistors are required to isolate C2 interface traffic from the user application. A typical isolation configuration is shown in Figure 30.1.

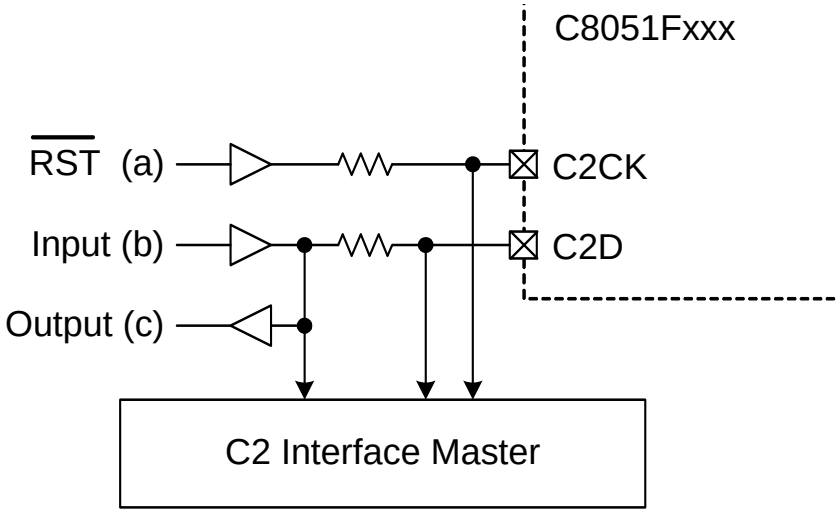


Figure 30.1. Typical C2 Pin Sharing

The configuration in Figure 30.1 assumes the following:

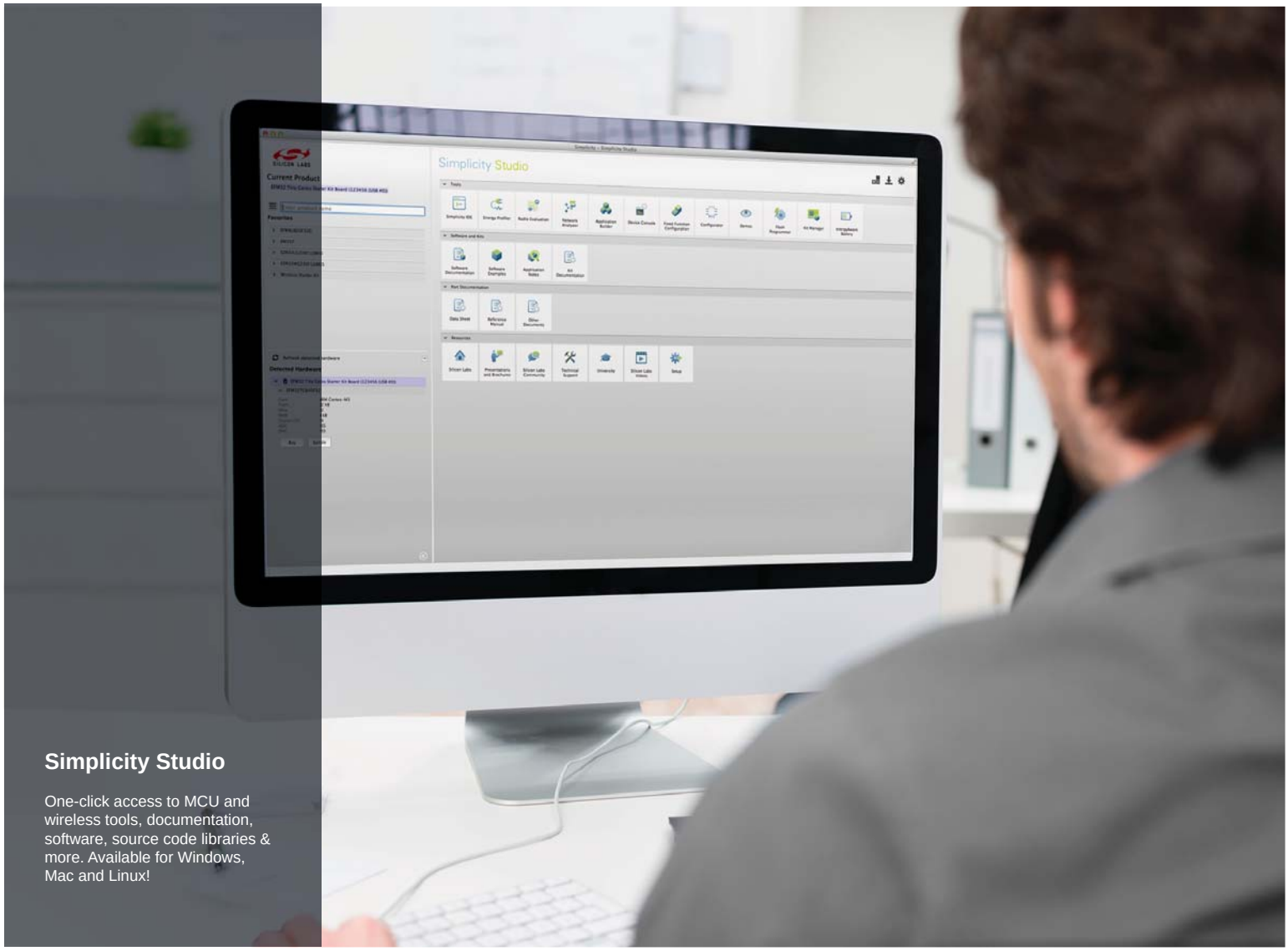
1. The user input (b) cannot change state while the target device is halted.
2. The RST pin on the target device is used as an input only.

Additional resistors may be necessary depending on the specific application.

- Added Port 2 Event and Port 3 Events to wake-up sources in “19.2.1. Internal Oscillator Suspend Mode” .
- Updated SFR Definition 20.3 with correct names for bits CP2AE and CP2E.
- Updated “21. Local Interconnect Network (LIN0)” with a voltage range specification for the internal oscillator.
- Updated LIN Register Definitions 21.9 and 21.10 with correct reset values.
- Updated “22. Controller Area Network (CAN0)” with a voltage range specification for the internal oscillator.
- Updated C2 Register Definitions 30.2 and 30.3 with correct C2 and SFR addresses.

Revision 1.2 to Revision 1.3

- Updated the note in “Power-Fail Reset/VDD Monitor” on page 154 to use a larger font.
- Added the note regarding the voltage regulator and VDD monitor in the high setting from “Power-Fail Reset/VDD Monitor” on page 154 to “Voltage Regulator (REG0)” on page 89 and “V_{DD} Maintenance and the V_{DD} monitor” on page 143. Also adjusted the language regarding the solution with the highest system reliability.
- Updated the steps in “V_{DD} Maintenance and the V_{DD} monitor” on page 143 to mention using the VDD monitor in the high setting during flash write/erase operations.
- Updated the SUSPEND bit description in OSCICN (SFR Definition 19.2) to mention that firmware must set the ZTCEN bit in REF0CN (SFR Definition 8.1) before entering suspend.
- Added a note to the IFRDY flag in the OSCICN register (SFR Definition 19.2) that the flag may not accurately reflect the state of the oscillator.
- Added VDD Ramp Time for Power On spec to Table 5.4, “Reset Electrical Characteristics,” on page 48.
- Added a note regarding programming at cold temperatures on –I devices to “Programming The Flash Memory” on page 138 and added Temperature during Programming Operations specification to Table 5.5, “Flash Electrical Characteristics,” on page 48.
- Added a note regarding P0.0/VREF when VDD is used as the reference to Table 20.1, “Port I/O Assignment for Analog Functions,” on page 191 and to the description of the REFSL bit in REF0CN (SFR Definition 8.1).
- Added a note regarding a potential unknown state on GPIO during power up if VIO ramps significantly before VDD to “Port Input/Output” on page 188 and “Reset Sources” on page 152.
- Added steps to set the FLEWT bit in the flash write/erase procedures in “Flash Erase Procedure” on page 139, “Flash Write Procedure” on page 139, and “Flash Write Optimization” on page 140.
- Added the “Reprogramming the VDD Monitor High Threshold” on page 138 section.
- Added a note regarding fast changes on VDD causing the V_{DD} Monitor to trigger to “Power-Fail Reset/VDD Monitor” on page 154.
- Added notes regarding UART TX and RX behavior in “Data Transmission” on page 259 and “Data Reception” on page 259.
- Added a note regarding an issue with /RST low time on some older devices to “Power-On Reset” on page 153.
- Added Table 5.8, “Crystal Oscillator Electrical Characteristics,” on page 50.
- Added a paragraph in “External Crystal Example” on page 185 regarding surface mount crystals and drive current.
- Removed recommendations to introduce a delay after enabling the VDD Monitor before enabling it as a reset source in “Power-Fail Reset/VDD Monitor” on page 154.



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