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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I ² C), CANbus, LINbus, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	33
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f590-im

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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C8051F581-IM	128	—	—	40	\checkmark	QFN-48	C8051F586-IM	96	\checkmark	\checkmark	25	—	QFN-32
C8051F582-IQ	128	\checkmark	~	25	—	QFP-32	C8051F587-IQ	96	—	—	25	—	QFP-32
C8051F582-IM	128	\checkmark	\checkmark	25	—	QFN-32	C8051F587-IM	96	—	—	25	—	QFN-32
C8051F583-IQ	128			25		QFP-32	C8051F588-IM	128	\checkmark	\checkmark	33	\checkmark	QFN-40
C8051F583-IM	128	—	—	25	—	QFN-32	C8051F589-IM	128	—	—	33	\checkmark	QFN-40
C8051F584-IQ	96	\checkmark	\checkmark	40	\checkmark	QFP-48	C8051F590-IM	96	\checkmark	\checkmark	33	\checkmark	QFN-40
C8051F584-IM	96	\checkmark	~	40	~	QFN-48	C8051F591-IM	96	—		33	\checkmark	QFN-40

Table 2.1. Product Selection Guide

Note: The suffix of the part number indicates the device rating and the package. All devices are RoHS compliant.

All of these devices are also available in an automotive version. For the automotive version, the -I in the ordering part number is replaced with -A. For example, the automotive version of the C8051F580-IM is the C8051F580-AM.

The -AM and -AQ devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (IMDS) and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.silabs.com with a registered and NDA approved user account. The -AM and -AQ devices enable high volume automotive OEM applications with their enhanced testing and processing. Please contact Silicon Labs sales for more information regarding –AM and -AQ devices for your automotive project.



12.2.1. Internal RAM

There are 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFR) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 12.1 illustrates the data memory organization of the C8051F58x/F59x.

12.2.1.1. General Purpose Registers

The lower 32 bytes of data memory, locations 0x00 through 0x1F, may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in SFR Definition 11.6). This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

12.2.1.2. Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (bit source or destination operands as opposed to a byte source or destination).

The MCS-51[™] assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte. For example, the instruction:

MOV C, 22.3h

moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

12.2.1.3. Stack

A programmer's stack can be located anywhere in the 256-byte data memory. The stack area is designated using the Stack Pointer (SP) SFR. The SP will point to the last location used. The next value pushed on the stack is placed at SP+1 and then SP is incremented. A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08, which is also the first register (R0) of register bank 1. Thus, if more than one register bank is to be used, the SP should be initialized to a location in the data memory not being used for data storage. The stack depth can extend up to 256 bytes.



14.1.1. Interrupt Priorities

Each interrupt source can be individually programmed to one of two priority levels: low or high. A low priority interrupt service routine can be preempted by a high priority interrupt. A high priority interrupt cannot be preempted. Each interrupt has an associated interrupt priority bit in an SFR (IE, EIP1, or EIP2) used to configure its priority level. Low priority is the default. If two interrupts are recognized simultaneously, the interrupt with the higher priority is serviced first. If both interrupts have the same priority level, a fixed priority order is used to arbitrate, given in Table 14.1.

14.1.2. Interrupt Latency

Interrupt response time depends on the state of the CPU when the interrupt occurs. Pending interrupts are sampled and priority decoded each system clock cycle. Therefore, the fastest possible response time is 5 system clock cycles: 1 clock cycle to detect the interrupt and 4 clock cycles to complete the LCALL to the ISR. If an interrupt is pending when a RETI is executed, a single instruction is executed before an LCALL is made to service the pending interrupt. Therefore, the maximum response time for an interrupt (when no other interrupt is currently being serviced or the new interrupt is of greater priority) occurs when the CPU is performing an RETI instruction followed by a DIV as the next instruction. In this case, the response time is 18 system clock cycles: 1 clock cycle to detect the interrupt, 5 clock cycles to execute the RETI, 8 clock cycles to complete the DIV instruction and 4 clock cycles to execute the LCALL to the ISR. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction.



SFR Definition 16.1. PCON: Power Control

Bit	7	6	5	4	3	2	1	0
Name			STOP	IDLE				
Туре				R/W	R/W			
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x87; SFR Page = All Pages

Bit	Name	Function
7:2	GF[5:0]	General Purpose Flags 5–0.
		These are general purpose flags for use under software control.
1	STOP	Stop Mode Select. Setting this bit will place the CIP-51 in Stop mode. This bit will always be read as 0. 1: CPU goes into Stop mode (internal oscillator stopped).
0	IDLE	IDLE: Idle Mode Select. Setting this bit will place the CIP-51 in Idle mode. This bit will always be read as 0. 1: CPU goes into Idle mode. (Shuts off clock to CPU, but clock to Timers, Interrupts, Serial Ports, and Analog Peripherals are still active.)



17. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- CIP-51 halts program execution
- Special Function Registers (SFRs) are initialized to their defined reset values
- External Port pins are forced to a known state
- Interrupts and timers are disabled.

All SFRs are reset to the predefined values noted in the SFR detailed descriptions. The contents of internal data memory are unaffected during a reset; any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost, even though the data on the stack is not altered.

The Port I/O latches are reset to 0xFF (all logic ones) in open-drain mode. Weak pullups are enabled during and after the reset. For V_{DD} Monitor and power-on resets, the \overrightarrow{RST} pin is driven low until the device exits the reset state.

Note: When VIO rises faster than VDD, which can happen when VREGIN and VIO are tied together, a delay created between GPIO power (VIO) and the logic controlling GPIO (VDD) results in a temporary unknown state at the GPIO pins. Cross coupling VIO and VDD with a 4.7 μF capacitor mitigates the root cause of the problem by allowing VIO and VDD to rise at the same rate.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal oscillator. The Watchdog Timer is enabled with the system clock divided by 12 as its clock source. Program execution begins at location 0x0000.



Figure 17.1. Reset Sources



17.1. Power-On Reset

During power-up, the device is held in a reset state and the \overline{RST} pin is driven low until V_{DD} settles above V_{RST}. A delay occurs before the device is released from reset; the delay decreases as the V_{DD} ramp time increases (V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST}). Figure 17.2. plots the power-on and V_{DD} monitor reset timing. The maximum V_{DD} ramp time is 1 ms; slower ramp times may cause the device to be released from reset before V_{DD} reaches the V_{RST} level. For ramp times less than 1 ms, the power-on reset delay (T_{PORDelay}) is typically less than 0.3 ms.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000) software can read the PORSF flag to determine if a power-up was the cause of reset. The content of internal data memory should be assumed to be undefined after a power-on reset. The V_{DD} monitor is enabled following a power-on reset.

Note: For devices with a date code before year 2011, work week 24 (1124), if the /RST pin is held low for more than 1 second while power is applied to the device, and then /RST is released, a percentage of devices may lock up and fail to execute code. Toggling the /RST pin does not clear the condition. The condition is cleared by cycling power. Most devices that are affected will show the lock up behavior only within a narrow range of temperatures (a 5 to 10 °C window). Parts with a date code of year 2011, work week 24 (1124) or later do not have any restrictions on /RST low time. The date code is included in the bottom-most line of the package top side marking. The date code is a four-digit number with the format YYWW, where YY is the two-digit calendar year and WW is the two digit work week.



Figure 17.2. Power-On and V_{DD} Monitor Reset Timing



SFR Definition 20.14. P0MDIN: Port 0 Input Mode

Bit	7	6	5	4	3	2	1	0						
Name	POMDIN[7:0]													
Туре	R/W													
Reset	1	1	1	1	1	1	1	1						

SFR Address = 0xF1; SFR Page = 0x0F

Bit	Name	Function
7:0	P0MDIN[7:0]	Analog Configuration Bits for P0.7–P0.0 (respectively).
		 Port pins configured for analog mode have their weak pull-up and digital receiver disabled. For analog mode, the pin also needs to be configured for open-drain mode in the P0MDOUT register. 0: Corresponding P0.n pin is configured for analog mode. 1: Corresponding P0.n pin is not configured for analog mode.

SFR Definition 20.15. P0MDOUT: Port 0 Output Mode

Bit	7	6	5	4	3	2	1	0						
Name	P0MDOUT[7:0]													
Туре	R/W													
Reset	0 0		0	0	0	0	0	0						

SFR Address = 0xA4; SFR Page = 0x0F

Bit	Name	Function
7:0	P0MDOUT[7:0]	Output Configuration Bits for P0.7–P0.0 (respectively).
		These bits are ignored if the corresponding bit in register P0MDIN is logic 0. 0: Corresponding P0.n Output is open-drain. 1: Corresponding P0.n Output is push-pull.



		Baud (bits/sec)													
		20 ł	<	19.2 K			9.6 K			4.8 K			1 K		
SYSCLK (MHz)	Mult.	Pres.	Div.	Mult.	Pres.	Div.	Mult.	Pres.	Div.	Mult.	Pres.	Div.	Mult.	Pres.	Div.
25	0	1	312	0	1	325	1	1	325	3	1	325	19	1	312
24.5	0	1	306	0	1	319	1	1	319	3	1	319	19	1	306
24	0	1	300	0	1	312	1	1	312	3	1	312	19	1	300
22.1184	0	1	276	0	1	288	1	1	288	3	1	288	19	1	276
16	0	1	200	0	1	208	1	1	208	3	1	208	19	1	200
12.25	0	0	306	0	0	319	1	0	319	3	0	319	19	0	306
12	0	0	300	0	0	312	1	0	312	3	0	312	19	0	300
11.0592	0	0	276	0	0	288	1	0	288	3	0	288	19	0	276
8	0	0	200	0	0	208	1	0	208	3	0	208	19	0	200

Table 21.2. Manual Baud Rate Parameters Examples

21.2.4. Baud Rate Calculations—Automatic Mode

If the LIN controller is configured for slave mode, only the prescaler and divider need to be calculated:

prescaler =
$$\ln \left[\frac{\text{SYSCLK}}{4000000} \right] \times \frac{1}{\ln 2} - 1$$

divider = $\frac{\text{SYSCLK}}{2^{(\text{prescaler} + 1)} \times 20000}$

The following example calculates the values of these variables for a 24 MHz system clock:

prescaler =
$$ln \left[\frac{24000000}{4000000} \right] \times \frac{1}{ln2} - 1 = 1.585 \cong 1$$

divider =
$$\frac{24000000}{2^{(1+1)} \times 20000}$$
 = 300

Table 21.3 presents some typical values of system clock and baud rate along with their factors.



SFR Definition 21.3. LIN0CF: LIN0 Control Mode Register

Bit	7	6	5	4	3	2	1	0
Name	LINEN	MODE	ABAUD					
Туре	R/W	R/W	R/W	R	R	R	R	R
Reset	0	1	1	0	0	0	0	0

SFR Address = 0xC9; SFR Page = 0x0F

Bit	Name	Function
7	LINEN	LIN Interface Enable Bit.
		0: LIN0 is disabled.
		1: LINU IS ENADIED.
6	MODE	LIN Mode Selection Bit.
		0: LIN0 operates in slave mode.
		1: LIN0 operates in master mode.
5	ABAUD	LIN Mode Automatic Baud Rate Selection.
		This bit only has an effect when the MODE bit is configured for slave mode.
		0: Manual baud rate selection is enabled.
		1: Automatic baud rate selection is enabled.
4:0	Unused	Read = 00000b; Write = Don't Care



24.3. Configuration and Operation

UART0 provides standard asynchronous, full duplex communication. It can operate in a point-to-point serial communications application, or as a node on a multi-processor serial interface. To operate in a point-to-point application, where there are only two devices on the serial bus, the MCE0 bit in SMOD0 should be cleared to 0. For operation as part of a multi-processor communications bus, the MCE0 and XBE0 bits should both be set to 1. In both types of applications, data is transmitted from the microcontroller on the TX0 pin, and received on the RX0 pin. The TX0 and RX0 pins are configured using the crossbar and the Port I/O registers, as detailed in Section "20. Port Input/Output" on page 188.

In typical UART communications, The transmit (TX) output of one device is connected to the receive (RX) input of the other device, either directly or through a bus transceiver, as shown in Figure 24.5.



Figure 24.5. Typical UART Interconnect Diagram

24.3.1. Data Transmission

Data transmission begins when software writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) will be set at the end of any transmission (the beginning of the stop-bit time). If enabled, an interrupt will occur when TI0 is set.

Note: THRE0 can have a momentary glitch high when the UART Transmit Holding Register is not empty. The glitch will occur some time after SBUF0 was written with the previous byte and does not occur if THRE0 is checked in the instruction(s) immediately following the write to SBUF0. When firmware writes SBUF0 and SBUF0 is not empty, TX0 will be stuck low until the next device reset. Firmware should use or poll on TI0 rather than THRE0 for asynchronous UART writes that may have a random delay in between transactions.

If the extra bit function is enabled (XBE0 = 1) and the parity function is disabled (PE0 = 0), the value of the TBX0 (SCON0.3) bit will be sent in the extra bit position. When the parity function is enabled (PE0 = 1), hardware will generate the parity bit according to the selected parity type (selected with S0PT[1:0]), and append it to the data field. Note: when parity is enabled, the extra bit function is not available.

24.3.2. Data Reception

Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be stored in the receive FIFO if the following conditions are met: the receive FIFO (3 bytes deep) must not be full, and the stop bit(s) must be logic 1. In the event that the receive FIFO is full, the incoming byte will be lost, and a Receive FIFO Overrun Error will be generated (OVR0 in register SCON0 will be set to logic 1). If the stop bit(s) were logic 0, the incoming data will not be stored in the receive FIFO. If the reception conditions are met, the data is stored in the receive FIFO, and the RI0 flag will be set. Note: when MCE0 = 1, RI0 will only be set if the extra bit was equal to 1. Data can be read from the receive FIFO by reading the SBUF0 register. The SBUF0 register represents the oldest byte in the FIFO. After SBUF0 is read, the next byte in the FIFO is immediately loaded into SBUF0, and space is made available in the FIFO for another incoming byte. If enabled, an interrupt will occur when RI0



Data transmission begins when an instruction writes a data byte to the SBUF1 register. The TI1 Transmit Interrupt Flag (SCON1.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN1 Receive Enable bit (SCON1.4) is set to 1. After the stop bit is received, the data byte will be loaded into the SBUF1 receive register if the following conditions are met: (1) RI1 must be logic 0, and (2) if MCE1 is logic 1, the 9th bit must be logic 1 (when MCE1 is logic 0, the state of the ninth data bit is unimportant). If these conditions are met, the eight bits of data are stored in SBUF1, the ninth bit is stored in RB81, and the RI1 flag is set to 1. A UART1 interrupt will occur if enabled when either TI1 or RI1 is set to '1'.



25.3. Multiprocessor Communications

9-Bit UART mode supports multiprocessor communication between a master processor and one or more slave processors by special use of the ninth data bit. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its ninth bit is logic 1; in a data byte, the ninth bit is always set to logic 0.

Setting the MCE1 bit (SCON1.5) of a slave processor configures its UART such that when a stop bit is received, the UART will generate an interrupt only if the ninth bit is logic 1 (RB81 = 1) signifying an address byte has been received. In the UART interrupt handler, software will compare the received address with the slave's own assigned 8-bit address. If the addresses match, the slave will clear its MCE1 bit to enable interrupts on the reception of the following data byte(s). Slaves that weren't addressed leave their MCE1 bits set and do not generate interrupts on the reception of the following data byte(s) addressed slave resets its MCE1 bit to ignore all transmissions until it receives the next address byte.

Multiple addresses can be assigned to a single slave and/or a single address can be assigned to multiple slaves, thereby enabling "broadcast" transmissions to more than one slave simultaneously. The master processor can be configured to receive all transmissions or a protocol can be implemented such that the master/slave role is temporarily reversed to enable half-duplex transmission between the original master and slave(s).



Figure 25.6. UART Multi-Processor Mode Interconnect Diagram



26.5. Serial Clock Phase and Polarity

Four combinations of serial clock phase and polarity can be selected using the clock control bits in the SPI0 Configuration Register (SPI0CFG). The CKPHA bit (SPI0CFG.5) selects one of two clock phases (edge used to latch the data). The CKPOL bit (SPI0CFG.4) selects between an active-high or active-low clock. Both master and slave devices must be configured to use the same clock phase and polarity. SPI0 should be disabled (by clearing the SPIEN bit, SPI0CN.0) when changing the clock phase or polarity. The clock and data line relationships for master mode are shown in Figure 26.5. For slave mode, the clock and data relationships are shown in Figure 26.6 and Figure 26.7. CKPHA must be set to 0 on both the master and slave SPI when communicating between two of the following devices: C8051F04x, C8051F06x, C8051F12x, C8051F31x, C8051F32x, and C8051F33x.

The SPI0 Clock Rate Register (SPI0CKR) as shown in SFR Definition 26.3 controls the master mode serial clock frequency. This register is ignored when operating in slave mode. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency or 12.5 MHz, whichever is slower. When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS (in 4-wire slave mode), and the serial input data synchronously with the slave's system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the slave's system clock frequency.



Figure 26.5. Master Mode Data/Clock Timing



SFR Definition 27.1. CKCON: Clock Control

Bit	7	6	5	4	3	2	1	0
Name	T3MH	T3ML	T2MH	T2ML	T1M	ТОМ	SCA[1:0]	
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8E; SFR Page = All Pages

Bit	Name	Function
7	ТЗМН	Timer 3 High Byte Clock Select.
		Selects the clock supplied to the Timer 3 high byte (split 8-bit timer mode only). 0: Timer 3 high byte uses the clock defined by the T3XCLK bit in TMR3CN. 1: Timer 3 high byte uses the system clock.
6	T3ML	Timer 3 Low Byte Clock Select.
		Selects the clock supplied to Timer 3. Selects the clock supplied to the lower 8-bit timer in split 8-bit timer mode.0: Timer 3 low byte uses the clock defined by the T3XCLK bit in TMR3CN.1: Timer 3 low byte uses the system clock.
5	T2MH	Timer 2 High Byte Clock Select.
		Selects the clock supplied to the Timer 2 high byte (split 8-bit timer mode only). 0: Timer 2 high byte uses the clock defined by the T2XCLK bit in TMR2CN. 1: Timer 2 high byte uses the system clock.
4	T2ML	Timer 2 Low Byte Clock Select.
		 Selects the clock supplied to Timer 2. If Timer 2 is configured in split 8-bit timer mode, this bit selects the clock supplied to the lower 8-bit timer. 0: Timer 2 low byte uses the clock defined by the T2XCLK bit in TMR2CN. 1: Timer 2 low byte uses the system clock.
3	T1	Timer 1 Clock Select.
		Selects the clock source supplied to Timer 1. Ignored when C/T1 is set to 1. 0: Timer 1 uses the clock defined by the prescale bits SCA[1:0]. 1: Timer 1 uses the system clock.
2	Т0	Timer 0 Clock Select.
		Selects the clock source supplied to Timer 0. Ignored when C/T0 is set to 1.
		0: Counter/Timer 0 uses the clock defined by the prescale bits SCA[1:0]. 1: Counter/Timer 0 uses the system clock.
1:0	SCA[1:0]	Timer 0/1 Prescale Bits.
		These bits control the Timer 0/1 Clock Prescaler:
		UU: System clock divided by 12
		10: System clock divided by 48
		11: External clock divided by 8 (synchronized with the system clock)





Figure 27.6. Timer 2 External Oscillator Capture Mode Block Diagram



SFR Definition 27.19. TMRnCF: Timer 4 and 5 Configuration

Bit	7	6 5 4 3 2 1				0		
Nam	e			Tn№	[1:0]	TOGn	TnOE	DCENn
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Rese	t O	0	0	0	0	0	0	0
TMR4CF SFR Address = 0xC9; TMR5CF SFR Address = 0x96; SFR Page = 0x10;								
Bit	Bit Name Function							
7:5	Reserved	Must Write	000b.					
4:3	TnM[1:0]	Timer 4 and 00: Timer cl 01: Timer cl 10: Timer cl 11: Timer cl	Timer 4 and 5 Clock Mode Select Bits. 00: Timer clock is SYSCLK / 12. 01: Timer clock is SYSCLK. 10: Timer clock is External Clock / 8 (synchronized to system clock). 11: Timer clock is SYSCLK / 2.					
2	TOGn	Timer 4 and 5 Toggle Output State.When Timer 4 or 5 are used to toggle a port pin, this bit can be used to read the stateof the output or can be written to force the state of the output.						
1	TnOE	 Timer 4 and 5 Output Enable. This bit enables the timer to output a 50% duty cycle output to the timer's assigned external port pin. The Timer is configured for Square Wave Output as follows: CPRLn = 0. CTn = 0. TnOE = 1. Load TMRnCAPH:TMRnCAPL. 0: Output of toggle mode not available at Timer's assigned port pin. 1: Output of toggle mode available at Timer's assigned port pin. 						
0	DCENn	 Decrement Enable. This bit enables the timer to count up or down as determined by the state of TnEX. 0: Timer will count up, regardless of the state of TnEX. 1: Timer will count up or down, depending on the state of TnEX as follows: If TnEx = 0, the timer counts down. If TnEx = 1, the timer counts up. 					e of TnEX. s:	



SFR Definition 28.2. PCA0MD: PCA0 Mode

Bit	7	6	5	4	3	2	1	0
Nam	CIDL	WDTE	WDLCK		CPS2	CPS1	CPS0	ECF
Туре	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Rese	t 0	1	0	0	0	0	0	0
SFR Address = 0xD9; SFR Page = 0x00								
Bit	Name		Function					
7	CIDL	PCA0 Counter Specifies PCA 0: PCA0 conti 1: PCA0 opera	 PCA0 Counter/Timer Idle Control. Specifies PCA0 behavior when CPU is in Idle Mode. 0: PCA0 continues to function normally while the system controller is in Idle Mode. 1: PCA0 operation is suspended while the system controller is in Idle Mode. 					
6	WDTE	Watchdog Tir If this bit is set 0: Watchdog T 1: PCA0 Modu	Watchdog Timer Enable If this bit is set, PCA0 Module 5 is used as the watchdog timer. 0: Watchdog Timer disabled. 1: PCA0 Module 5 enabled as Watchdog Timer.					
5	WDLCK	 Watchdog Timer Lock This bit locks/unlocks the Watchdog Timer Enable. When WDLCK is set, the Watchdog Timer may not be disabled until the next system reset. 0: Watchdog Timer Enable unlocked. 1: Watchdog Timer Enable locked. 						
4	Unused	Read = 0b, Write = Don't care.						
3:1	CPS[2:0]	PCA0 Counter/Timer Pulse Select. These bits select the timebase source for the PCA0 counter 000: System clock divided by 12 001: System clock divided by 4 010: Timer 0 overflow 011: High-to-low transitions on ECI (max rate = system clock divided by 4) 100: System clock 101: External clock divided by 8 (synchronized with the system clock) 110: Timer 4 overflow 111: Timer 5 overflow						
0	ECF	PCA0 Counter/Timer Overflow Interrupt Enable.						
		 This bit sets the masking of the PCA0 Counter/Timer Overflow (CF) interrupt. 0: Disable the CF interrupt. 1: Enable a PCA0 Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set. 					ot. 0CN.7) is	
Note:	ote: When the WDTE bit is set to 1, the other bits in the PCA0MD register cannot be modified. To change the contents of the PCA0MD register, the Watchdog Timer must first be disabled.							



29.3.3. High-Speed Output Mode

In High-Speed Output mode, a module's associated CEXn pin is toggled each time a match occurs between the PCA1 Counter and the module's 16-bit capture/compare register (PCA1CPHn and PCA1CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA1CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the TOG1n, MAT1n, and ECOM1n bits in the PCA1CPMn register enables the High-Speed Output mode. If ECOM1n is cleared, the associated pin will retain its state, and not toggle on the next match event.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA1 Capture/Compare registers, the low byte should always be written first. Writing to PCA1CPLn clears the ECOM1n bit to 0; writing to PCA1CPHn sets ECOM1n to 1.



Figure 29.6. PCA1 High-Speed Output Mode Diagram

