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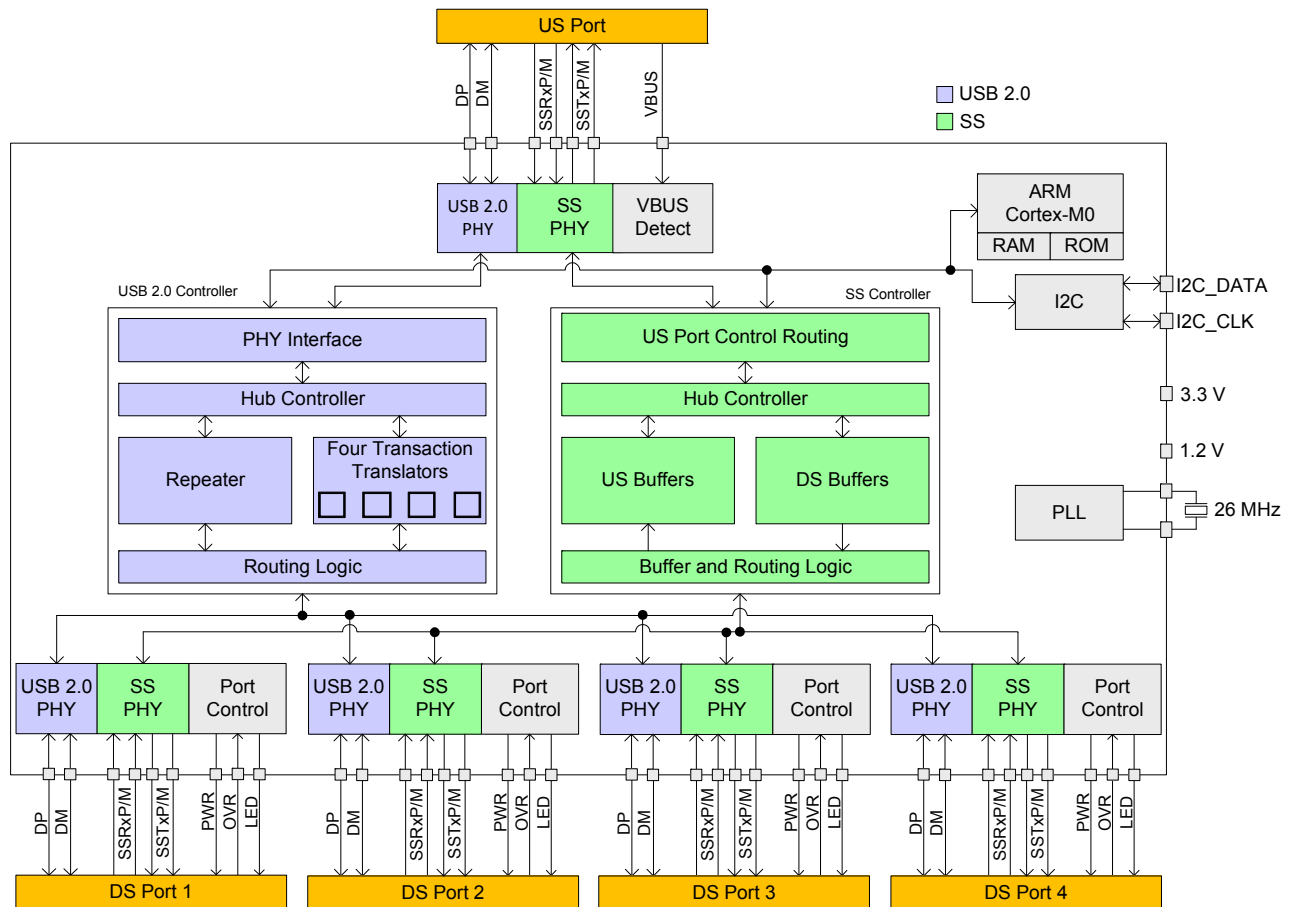
What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details

Product Status	Active
Applications	USB 2.0 Hub Controller
Core Processor	ARM® Cortex®-M0
Program Memory Type	ROM (32kB)
Controller Series	CYUSB
RAM Size	16K x 8
Interface	I ² C
Number of I/O	10
Voltage - Supply	1.14V ~ 1.26V, 2.5V ~ 2.7V, 3V ~ 3.6V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb2304-68ltxit

Block Diagram



HX3 Product Options

Table 1. HX3 Product Options

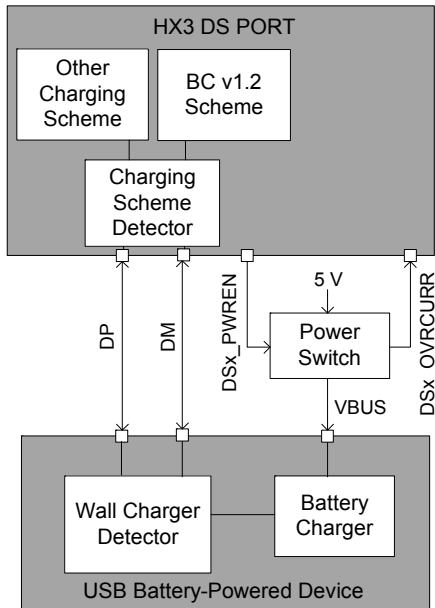
Features	CYUSB3302	CYUSB3304	CYUSB3312	CYUSB3314	CYUSB3324	CYUSB3326	CYUSB3328	CYUSB2302-68LTXI	CYUSB2304-68LTXI
Number of DS ports	2 (USB 3.0)	4 (USB 3.0)	2 (USB 3.0)	4 (USB 3.0)	4 (USB 3.0)	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	8 (4 SS, 4 USB 2.0)	2 (USB 2.0)	4 (USB 2.0)
Number of Shared Link ports	0	0	0	0	0	2 ^[1]	4	0	0
BC v1.2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACA-Dock	No	No	No	No	Yes	No	Yes	No	No
External Power Switch Control	Ganged	Ganged	Individual and Ganged	Individual and Ganged	Individual and Ganged	Individual	Individual	Ganged	Ganged
Pin-Strap support	No	No	Yes	Yes	Yes	Yes	Yes	No	No
I ² C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Vendor command	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Port indicators	No	No	Yes	Yes	Yes	No	No	No	No
Packages ^[2]	68-QFN, 100-ball BGA	68-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	68-QFN, 100-ball BGA	68-QFN, 100-ball BGA
Temperature range	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial (88-QFN only) and Commercial	Industrial and Commercial	Industrial and Commercial

Notes

- DS1 and DS2 are Shared link Ports.
- BGA Industrial Grade packages are limited to 1 W of active power. For power calculations refer to [Table 10](#) on page 33.

When the US port is disconnected from the host, HX3 detects if any of the DS ports are connected to a device requesting charging. It determines the charging method and then switches to the appropriate signaling based on the detected charging specification as shown in Figure 4. The hub either emulates a USB-compliant dedicated charging port by connecting DP and DM (see the BC v1.2 specification) or other supported proprietary charging schemes.

Figure 4. Ghost Charge Implementation in HX3



Ghost Charge is enabled by default and can be disabled through configuration. Refer to [Configuration Options on page 24](#).

Vendor-Command Support

HX3 supports vendor-specific requests and can also enumerate as a vendor-specific device. The vendor-specific request can be used to (a) bridge USB and I²C and (b) configure HX3. This feature can be used for the following applications:

- Firmware upgrade of an external ASSP connected to HX3 through USB
- In-System programming (ISP) of an EEPROM connected to HX3 through USB

Note

3. 124 kΩ is the recommended RID_A value as per BC v1.2 specification, but some portable devices use custom RID_A values.

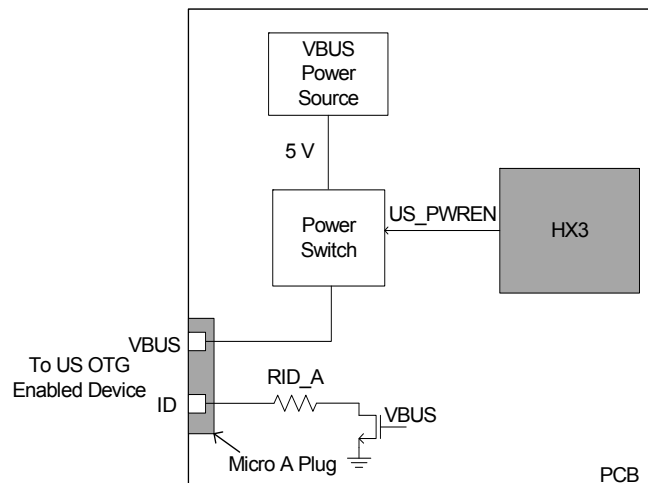
ACA-Dock Support

In traditional USB topologies, the host provides VBUS to enable and charge the connected devices. For OTG hosts, however, an ACA-Dock provides VBUS and a method to charge the host. HX3 supports the ACA-Dock standard (see BC v1.2 specification) by integrating the functions of the adapter controller.

Figure 5 shows the ACA-Dock system. If the ACA-Dock feature is enabled, HX3 turns on the external power switch to drive VBUS on the US port. To inform the OTG host that it is connected to an ACA-Dock, the ID pin is tied to ground using a resistor RID_A³ as shown in Figure 5. The ACA-Dock feature can be disabled using the [Configuration Options on page 24](#).

For example, a BC v1.2 compliant phone such as a Sony Xperia (neo V) can be docked to a HX3-based ACA-Dock system. The phone acts as an OTG host and the ACA-Dock charges the phone connected to the US port while also powering the four DS ports.

Figure 5. ACA-Dock Support



Pin Information

Figure 6. HX3 68-Pin QFN 2-Port Pinout

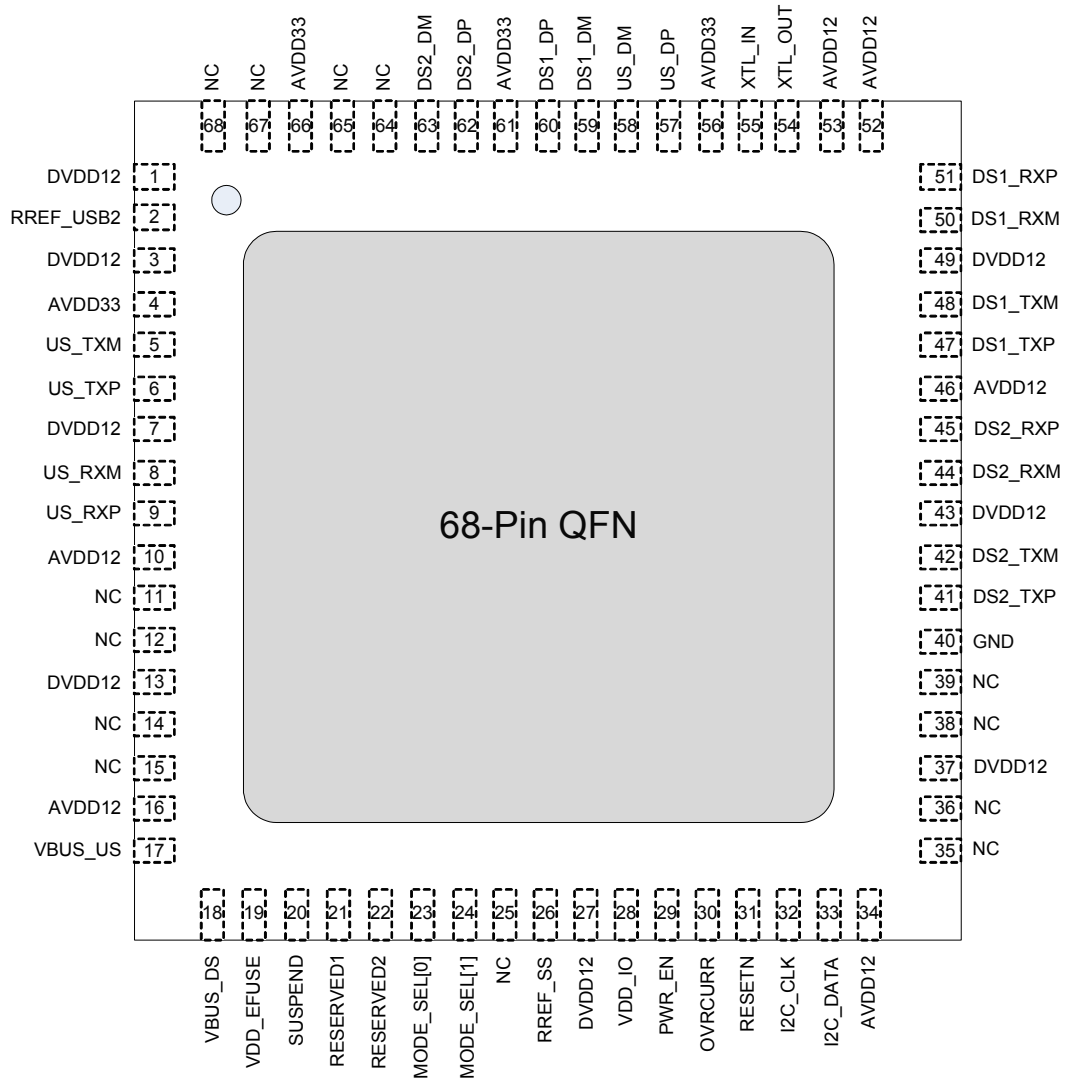


Figure 9. HX3 100-Ball BGA Pinout for CYUSB3304

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
NC	DS4_DM	DS4_DP	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
NC	NC	NC	VDD_IO	VSS	AVDD33	NC	NC	NC	DVDD12
C1	C2	C3	C4	C5	C6	C7	C8	C9	10
US_TXM	NC	NC	DS3_DP	DS3_DM	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
US_TXP	NC	NC	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
DVDD12	RREF_US B2	NC	NC	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
US_RXM	VSS	AVDD33	MODE_SE L[1]	DVDD12	OVRCUR R	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
US_RXP	VBUS_DS	SUSPEND	RESERVE D1	MODE_SE L[0]	VDD_IO	PWR_EN	I2C_DATA	VSS	DS2_RXM
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
AVDD12	VBUS_US	VDD_EFUS SE	RESERVE D2	RREF_SS	VSS	DS2_TXM	DS2_TXP	NC	AVDD12
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
VSS	AVDD12	VSS	GPIO	NC	I2C_CLK	NC	NC	VSS	DS3_RXM
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
DS4_TXP	DS4_TXM	DVDD12	DS4_RXP	DS4_RXM	NC	DS3_TXP	DS3_TXM	DVDD12	DS3_RXP

Table 2. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB3302 and CYUSB3304 (continued)

Pin Name		Type	68-QFN Pin#	100-BGA Ball #	Description
CYUSB3302	CYUSB3304				
RESERVED1		I/O	21	G4	This pin must be pulled HIGH using a 10 k Ω to VDD_IO.
RESERVED2		I	22	H4	This pin must be pulled HIGH using a 10 k Ω to VDD_IO.
Mode Select, Clock, and Reset					
MODE_SEL[0]		I	23	G5	Device operation mode select bit 0; refer to Table 5 on page 24
MODE_SEL[1]		I	24	F4	Device operation mode select bit 1; refer to Table 5 on page 24
XTL_OUT		A	54	E6	Crystal out
XTL_IN		A	55	E5	Crystal in
RESETN		I	31	F7	Active LOW reset input
I2C_CLK		I/O	32	J6	I ² C clock
I2C_DATA		I/O	33	G8	I ² C data
SUSPEND		I/O	20	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and Ground					
VDD_EFUSE		PWR	19	H3	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V.
AVDD12		PWR	10, 16, 34, 46, 52, 53	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND		PWR	40	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12		PWR	1, 3, 7, 13, 27, 37, 43, 49,	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS_US		PWR	17	H2	This pin must be connected to VBUS from US port
VBUS_DS		PWR	18	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	4, 56, 61, 66	A4, A7, B6, F3	3.3 V analog supply
VDD_IO		PWR	28	B4, E7, G6	3.3 V I/O supply
USB Precision Resistors					
RREF_USB2		A	2	E2	Connect pin to a precision resistor (6.04 k Ω $\pm$ 1%) to generate a current reference for USB 2.0 PHY.
RREF_SS		A	26	H5	Connect pin to a precision resistor (200 Ω $\pm$ 1%) for SS PHY termination impedance calibration.

Note

4. These pins are Do Not Use (DNU); they must be left floating.

Figure 11. HX3 88-Pin QFN 4-Port Pinout

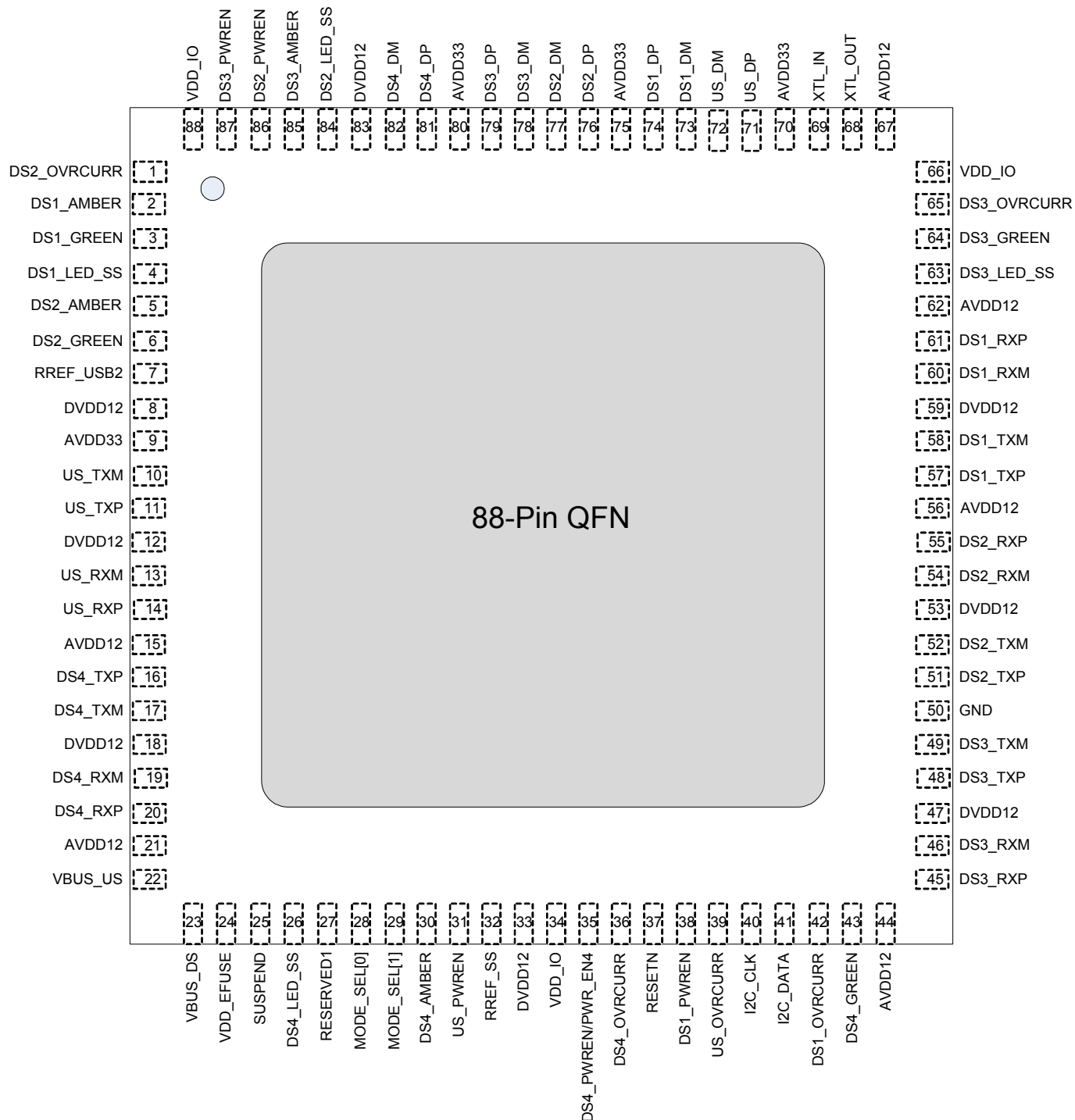


Figure 12. HX3 100-Ball BGA Pinout for CYUSB3312

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
DS3_PWR EN	NC	NC	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
DS2_OVR CURR	DS2_PWR EN	DS3_AMBE R	VDD_IO	VSS	AVDD33	DS3_OVR CURR	DS3_GREE N	DS3_LED_ SS	DVDD12
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
US_TXM	DS1_AMBE R	DS2_LED_ SS	NC	NC	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
US_TXP	DS1_LED_ SS	DS1_GREE N	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
DVDD12	RREF_USB 2	DS2_GREE N	DS2_AMBE R	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
US_RXM	VSS	AVDD33	MODE_SE L[1]	DVDD12	DS4_OVR CURR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
US_RXP	VBUS_DS	SUSPEND	RESERVE D1	MODE_SE L[0]	VDD_IO	DS4_PWR EN	I2C_DATA	VSS	DS2_RXM
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
AVDD12	VBUS_US	VDD_EFUS E	DS4_LED_ SS	RREF_SS	VSS	DS2_TXM	DS2_TXP	DS4_GREE N	AVDD12
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
VSS	AVDD12	VSS	DS4_AMBE R	US_PWRE N	I2C_CLK	DS1_PWR EN	DS1_OVR CURR	VSS	NC
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
NC	NC	DVDD12	NC	NC	US_OVRC URR	NC	NC	DVDD12	NC

Figure 13. HX3 100-Ball BGA Pinout for CYUSB3314, CYUSB332x

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
DS3_PWR EN	DS4_DM	DS4_DP	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
DS2_OVR CURR	DS2_PWR EN	DS3_AMB ER	VDD_IO	VSS	AVDD33	DS3_OVR CURR	DS3_GRE EN	DS3_LED _SS	DVDD12
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
US_TXM	DS1_AMB ER	DS2_LED _SS	DS3_DP	DS3_DM	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
US_TXP	DS1_LED _SS	DS1_GRE EN	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
DVDD12	RREF_US B2	DS2_GRE EN	DS2_AMB ER	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
US_RXM	VSS	AVDD33	MODE_SE L[1]	DVDD12	DS4_OVR CURR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
US_RXP	VBUS_DS	SUSPEND	RESERVE D1	MODE_SE L[0]	VDD_IO	DS4_PWR EN	I2C_DATA	VSS	DS2_RXM
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
AVDD12	VBUS_US	VDD_EFU SE	DS4_LED _SS	RREF_SS	VSS	DS2_TXM	DS2_TXP	DS4_GRE EN	AVDD12
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
VSS	AVDD12	VSS	DS4_AMB ER	US_PWR EN	I2C_CLK	DS1_PWR EN	DS1_OVR CURR	VSS	DS3_RXM
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
DS4_TXP	DS4_TXM	DVDD12	DS4_RXP	DS4_RXM	US_OVRC URR	DS3_TXP	DS3_TXM	DVDD12	DS3_RXP

Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X (continued)

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314				
	CYUSB3324				
	CYUSB3326				
	CYUSB3328				
DS2 Port					
DS2_RXP		I	55	F10	SuperSpeed receive plus
DS2_RXM		I	54	G10	SuperSpeed receive minus
DS2_TXP		O	51	H8	SuperSpeed transmit plus
DS2_TXM		O	52	H7	SuperSpeed transmit minus
DS2_DP		I/O	76	A6	USB 2.0 data plus
DS2_DM		I/O	77	A5	USB 2.0 data minus
DS2_OVRCURR		I	1	B1	Overcurrent detect input for DS2 port
DS2_PWREN ^[7]		I/O	86	B2	VBUS power enable output for DS2 port. When the port is disabled, this pin is in tristate.
DS2_CDP_EN ^[8]					This pin is called DS2_CDP_EN in the pin-strap configuration mode.
DS2_AMBER ^[7]		I/O	5	E4	LED_AMBER output for DS2 port
NON_REMOVABLE[0] ^[8]					This pin is called NON_REMOVABLE[0] in the pin-strap configuration mode.
DS2_GREEN ^[7]		I/O	6	E3	CYUSB3312/3314/3324: LED_GREEN output for DS2 port
DS2_VBUSEN_SL ^[7]					CYUSB3326/3328: VBUS power enable output for SS port 2
NON_REMOVABLE[1] ^[8]					This pin is called NON_REMOVABLE[1] in the pin-strap configuration mode.
DS2_LED_SS ^[7]		I/O	84	C3	LED_SS output for DS2 port
PWR_EN_SEL ^[8]					This pin is called PWR_EN_SEL in the pin-strap configuration mode.
DS3 Port					
NC	DS3_RXP	I	45	K10	SuperSpeed receive plus
NC	DS3_RXM	I	46	J10	SuperSpeed receive minus
NC	DS3_TXP	O	48	K7	SuperSpeed transmit plus
NC	DS3_TXM	O	49	K8	SuperSpeed transmit minus
NC	DS3_DP	I/O	79	C4	USB 2.0 data plus
NC	DS3_DM	I/O	78	C5	USB 2.0 data minus
DS3_OVRCURR		I	65	B7	CYUSB3314/3324/3326/3328: Overcurrent detect input for DS3 port CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
DS3_PWREN ^[7]		I/O	87	A1	VBUS power enable output for DS3 port. When the port is disabled, this pin is in tristate.
DS3_CDP_EN ^[8]					This pin is called DS3_CDP_EN in the pin-strap configuration mode.
DS3_AMBER ^[7]		I/O	85	B3	LED_AMBER output for DS3 port
VID_SEL[2] ^[8]					This pin is called VID_SEL[2] in the pin-strap configuration mode.

Notes

7. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
8. For pin-strap configuration details, refer to [Table 6](#) on page 25.

I²C Configuration

When enabled for I²C configuration through the MODE_SEL pins (See Table 5 on page 24), HX3 can be configured as an I²C master or as an I²C slave. HX3's configuration data is a maximum of 197 bytes and HX3's firmware is 10 KB. Note that HX3's firmware also includes configuration settings.

HX3 as I²C Master

HX3 reads configurations from an external I²C EEPROM with sizes ranging from 16 to 64 KB. An example of a supported EEPROM is 24LC128. Based on the contents of the bSignature and bImageType fields in Table 7 on page 26, HX3 performs one of the following actions:

- Loads custom configuration settings from the EEPROM when bSignature is "CY" and bImageType is 0xD4.
- Loads the Cypress-provided firmware from the EEPROM when bSignature is "CY" and bImageType is 0xB0. This firmware also includes configuration settings.
- If bSignature ≠ "CY", HX3 enumerates in the vendor-specific mode.

The contents of the EEPROM can be updated with the easy-to-use [Cypress Blaster Plus](#) tool. Blaster Plus is a

GUI-based tool to configure HX3. This tool allows to do the following:

- Download the Cypress-provided firmware from a PC via HX3's US port and store it on an EEPROM connected to HX3's I²C port.
- Read the configuration settings from the EEPROM. These settings are displayed in the Blaster Plus GUI. Modify settings as required.
- Write back the updated settings on to the EEPROM. In addition, an image file can be created for external use.

The Blaster Plus tool, user guide, and the Cypress-provided firmware are available at www.cypress.com/hx3.

HX3 as I²C Slave

An external I²C master can program the configuration settings into HX3 according to the EEPROM map in Table 7 on page 26. Alternatively, the HX3 firmware (<10 KB), which includes configuration settings, can also be programmed. It is recommended to use the Blaster Plus tool to create the HX3 firmware or configuration image file. HX3's I²C slave address needs to be provided while creating the image file. Refer to Table 6 for HX3's I²C slave address.

Table 7. EEPROM Map

I ² C Offset	Bits	Name	Default	Description
0	7:0	bSignature LSB ("C")	0x43	The first byte of the 2-byte signature initialized with "CY" ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device.
1	7:0	bSignature MSB ("Y")	0x59	The second byte of the 2-byte signature initialized with "CY" ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device.
2	7:6	bImageCTL	b'00	Reserved
	5:4	I ² C Speed	b'11	b'01: 400 kHz b'11: 100 kHz
	3:1	bImageCTL	b'000	Reserved
	0	bImageCTL	0	0: Execution binary file 1: Data file
3	7:0	bImageType	0xD4	0xD4: Load only configuration 0xB0: Load firmware boot image All other bImageType will return an error code.
4	7:0	bD4Length	40	bD4Length is defined in bytes as the length from offset 5. I ² C offset bytes 0–4 are the header bytes. bD4Length = 6: Only update VID, PID, and DID bD4Length = 18: Configuration options (no PHY trim) bD4Length = 40: Configuration options with PHY trim options bD4Length > 40: User must provide valid string descriptors bD4Length > 192: Error
5	7:0	VID [7:0]	0xB4	Custom Vendor ID - LSB
6	7:0	VID [15:8]	0x04	Custom Vendor ID - MSB
7	7:0	PID [7:0]	0x04	Custom Product ID (PID)
8	7:0	PID [15:8]	0x65	Default: 0x6504 If separate PID is used for USB 2.0, the USB 2.0 PID will be read from offset 35 and 36. Else, USB 2.0 PID = PID+2; Default: 0x6506

Table 7. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
9	7:0	DID [7:0]	00 - 88-pin QFN, 10 - 68-pin QFN	Custom Device ID - revision - LSB
10	7:0	DID [15:8]	50	Custom Device ID - revision - MSB
11	7:0	Reserved	0	Reserved
12	7:4	SHARED_LINK_EN	b'0000	Enable Shared Link on DS port bit[7:4]=DS4, DS3, DS2, DS1 0: Shared Link not enabled 1: Shared Link enabled
	3:0	SHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a SuperSpeed port is active. bit[3:0] = DS4, DS3, DS2, DS1 0: Not active 1: Active
13	7:0	POWER_ON_TIME	0x32	Time (in 2-ms intervals) from the time the power-on sequence begins on a port until power is good on that port (bPwron2PwrGood)
14	7:4	REMOVABLE_PORTS [3:0]	b'1111	Indicates if the port is removable. bit[7:4]=DS4, DS3, DS2, DS1 0: Non-removable 1: Removable
	3:0	UHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a USB 2.0 port is active. bit[3:0]=DS4, DS3, DS2, DS1 0: Not active 1: Active
15	7	SS_LED_PIN_CONTROL	0	Port 1–4: SS LED disable 0: DS[1:4]_LED_SS are LEDs. The LED glows when the SS port is active and not in disabled state. 1: DS[1:4]_LED_SS are not LEDs
	6	GREEN_LED_PIN_CONTROL	0	Port 1–4: USB 2.0 Green LED disable 0: DS[1:4]_GREEN are LEDs 1: DS[1:4]_GREEN are not LEDs
	5	AMBER_LED_PIN_CONTROL	0	Port 1–4: USB 2.0 Amber LED disable 0: DS[1:4]_AMBER are LEDs 1: DS[1:4]_AMBER are not LEDs
	4	PORT_INDICATORS	1	Port indicators supported 0: Port indicators are not supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request has no effect. 1: Port indicators are supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request controls the indicators.
	3	COMPOUND_HUB	0	Identifies a compound device. 0: Hub is not part of a compound device. 1: Hub is part of a compound device.
	2:1	Reserved	0	Reserved
	0	GANG	0	1: Ganged power switch enable for all DS ports 0: Individual port power switch enable for each DS port

Table 7. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
23	7:6	HS_AMPLITUDE_DS4	b'00	HS driver amplitude control; HS driver current: +0% to +7.5% b'00: Default b'01: +2.5% b'10: +5% b'11: +7.5%
	5:4	HS_AMPLITUDE_DS3	b'00	
	3:2	HS_AMPLITUDE_DS2	b'00	
	1:0	HS_AMPLITUDE_DS2	b'00	
24	7:6	HS_AMPLITUDE_US	b'00	HS driver slope control for all ports b'0000: +15% b'0001: +5% b'0100: Default b'0101: -5% b'1111: -7.5%
	5:2	HS_SLOPE	b'0100	
	1:0	HS_TX_VREF	b'10	
25	7:3	HS_PREEMP_EN[4:0]	b'00000	HS driver pre-emphasis enable – for ports DS4, DS3, DS2, DS1, and US 0: pre-emphasis is disabled 1: pre-emphasis is enabled HS driver pre-emphasis depth 0: +10% 1: +20%
	2	HS_PREEMP_DEPTH_DS4 ^[17]	0	
	1	HS_PREEMP_DEPTH_DS3 ^[17]	0	
	0	HS_PREEMP_DEPTH_DS2 ^[17]	0	
	7	HS_PREEMP_DEPTH_DS1 ^[17]	0	
26	6	HS_PREEMP_DEPTH_US ^[17]	0	Reserved
	5	Reserved	1	
	4:1	PCS_TX_DEEMPH_DS4	0x6	
	0	Reserved	0	
	7:4	PCS_TX_DEEMPH_DS3	0x6	
27	3:0	PCS_TX_DEEMPH_DS2	0x6	USB 3.0 Tx driver de-emphasis value 0x3: -2.75 dB 0x6: -3.4 dB (Default) 0x9: -4.0 dB
	7:4	PCS_TX_DEEMPH_DS1	0x6	
28	3:0	PCS_TX_DEEMPH_US	0x6	Reserved
	7	Reserved	0	
29	6	Reserved	1	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
	5:0	PCS_TX_SWING_FULL_DS4	0x29	
30	7:6	Reserved	0	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
	5:0	PCS_TX_SWING_FULL_DS3	0x29	

Note

17. HS_PREEMP_DEPTH is valid only when corresponding HS_PREEMP_EN is set for that port.

Ordering Information

Table 11 lists HX3's ordering information. The table contains only the part numbers that are currently available for order. Additional part numbers for industrial temperature range can be made available on request. For more information, visit the Cypress [website](#) or contact the local sales representative.

Table 11. Ordering Information

Serial No.	Ordering Part Number	Number of DS Ports	Number of Shared Link Ports	Ghost Charge	ACA-Dock	Temperature	Package
1.	CYUSB3302-68LTXC	2 (USB 3.0)	0	Yes	No	0-70 °C	68-QFN
2.	CYUSB3302-68LTXI	2 (USB 3.0)	0	Yes	No	-40-85 °C	68-QFN
3.	CYUSB3304-68LTXC	4 (USB 3.0)	0	Yes	No	0-70 °C	68-QFN
4.	CYUSB3304-68LTXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	68-QFN
5.	CYUSB3312-88LTXC	2 (USB 3.0)	0	Yes	No	0-70 °C	88-QFN
6.	CYUSB3312-88LTXI	2 (USB 3.0)	0	Yes	No	-40-85 °C	88-QFN
7.	CYUSB3314-88LTXC	4 (USB 3.0)	0	Yes	No	0-70 °C	88-QFN
8.	CYUSB3314-88LTXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	88-QFN
9.	CYUSB3324-88LTXC	4 (USB 3.0)	0	Yes	Yes	0-70 °C	88-QFN
10.	CYUSB3324-88LTXI	4 (USB 3.0)	0	Yes	Yes	-40-85 °C	88-QFN
11.	CYUSB3326-88LTXC	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	0-70 °C	88-QFN
12.	CYUSB3326-88LTXI	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	-40-85 °C	88-QFN
13.	CYUSB3328-88LTXC	8 (4 SS, 4 USB 2.0)	4	Yes	Yes	0-70 °C	88-QFN
14.	CYUSB3328-88LTXI	8 (4 SS, 4 USB 2.0)	4	Yes	Yes	-40-85 °C	88-QFN
15.	CYUSB3302-BVXC	2 (USB 3.0)	0	Yes	No	0-70 °C	100-BGA
16.	CYUSB3302-BVXI	2 (USB 3.0)	0	Yes	No	-40-85 °C	100-BGA
17.	CYUSB3304-BVXC	4 (USB 3.0)	0	Yes	No	0-70 °C	100-BGA
18.	CYUSB3304-BVXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	100-BGA
19.	CYUSB3312-BVXC	2 (USB 3.0)	0	Yes	No	0-70 °C	100-BGA
20.	CYUSB3312-BVXI	2 (USB 3.0)	0	Yes	No	-40-85 °C	100-BGA
21.	CYUSB3314-BVXC	4 (USB 3.0)	0	Yes	No	0-70 °C	100-BGA
22.	CYUSB3314-BVXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	100-BGA
23.	CYUSB3324-BVXC	4 (USB 3.0)	0	Yes	Yes	0-70 °C	100-BGA
24.	CYUSB3324-BVXI	4 (USB 3.0)	0	Yes	Yes	-40-85 °C	100-BGA
25.	CYUSB3326-BVXC	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	0-70 °C	100-BGA
26.	CYUSB3326-BVXI	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	-40-85 °C	100-BGA
27.	CYUSB3328-BVXC	8 (4 SS, 4 USB 2.0)	4	Yes	Yes	0-70 °C	100-BGA
28.	CYUSB2302-68LTXI	2 (USB 2.0)	0	Yes	No	-40-85 °C	68-QFN
29.	CYUSB2304-68LTXI	4 (USB 2.0)	0	Yes	No	-40-85 °C	68-QFN

Packaging

Table 12. Package Characteristics

Parameter	Description	Min	Typ	Max	Units
T _A	Operating ambient temperature	−40	–	85	°C
T _J	Operating junction temperature	−40	–	125	°C
T _{JA}	Package J _A (68-pin QFN)	–	16.2	–	°C/W
T _{JA}	Package J _A (88-pin QFN)	–	15.7	–	°C/W
T _{JA}	Package J _A (100-ball BGA)	–	35	–	°C/W
T _{JC}	Package J _C (68-pin QFN)	–	23.8	–	°C/W
T _{JC}	Package J _C (88-pin QFN)	–	18.9	–	°C/W
T _{JC}	Package J _C (100-ball BGA)	–	12	–	°C/W

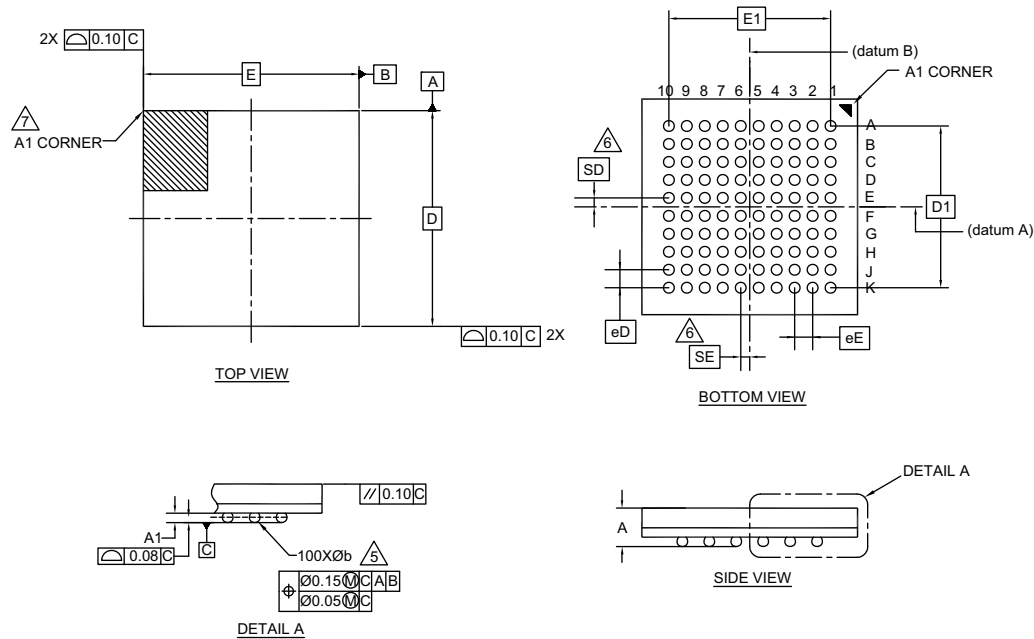
Table 13. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
68-pin QFN	260 °C	30 seconds
88-pin QFN	260 °C	30 seconds
100-ball BGA	260 °C	30 seconds

Table 14. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
68-pin QFN	MSL 3
88-pin QFN	MSL 3
100-ball BGA	MSL 3

Figure 20. 100-Ball BGA (6.0 × 6.0 × 1.0 mm) BZ100 Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	6.00 BSC		
E	6.00 BSC		
D1	4.50 BSC		
E1	4.50 BSC		
MD	10		
ME	10		
N	100		
Ø b	0.25	0.30	0.35
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.25 BSC		
SE	0.25 BSC		

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
- JEDEC SPECIFICATION NO. REF. : MO-195C.

51-85209 *F

Acronyms

Table 15. Acronyms Used in this Document

Acronym	Description
ACA	Accessory Charging Adapter
ASSP	Application-Specific Standard Product
BC	Battery Charging
CDP	Charging Downstream Port
DS	DownStream
DCP	Dedicated Charging Port
DNU	Do Not Use
DWG	Device Working Group
EEPROM	Electrically Erasable Programmable Read-Only Memory
FS	Full-Speed
FW	FirmWare
GND	GrouND
GPIO	General-Purpose Input/Output
HS	Hi-Speed
ISP	In-System Programming
I/O	Input/Output
LS	Low-Speed
NC	No Connect
OTG	On-The-Go
PID	Product ID
POR	Power-On Reset
ROM	Read-Only Memory
SCL	Serial CLock
SDA	Serial DAta
SS	SuperSpeed
TT	Transaction Translator
US	UpStream
VID	Vendor ID

Reference Documents

[USB 2.0 Specification](#)

[USB 3.0 Specification](#)

[Battery Charging Specification](#)

Document Conventions

Units of Measure

Table 16. Units of Measure

Symbol	Unit of Measure
°C	degree celsius
Ω	ohm
Gbps	gigabit per second
KB	kilobyte
kHz	kilohertz
kΩ	kiloohm
Mbps	megabit per second
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
ppm	parts per million
V	volt

Silicon Revision History

This datasheet is applicable for the USB-IF certified (TID# 330000060) HX3 Rev. *D and Rev. *C Silicon.

Rev. *D: This Silicon revision improves the yield of HX3, and is drop-in compatible for all the part numbers. There is no need to change the board design or layout to use the HX3 Rev. *D Silicon. Products are completely compatible with the HX3 Rev. *C Silicon.

Rev. *C: This Silicon revision fixes the errata applicable to the Rev. *A Silicon.

The following table defines the changes between Rev. *A, Rev. *C, and Rev. *D Silicon.

No.	Items	Part Numbers	Rev. *A	Rev. *C	Rev. *D
1	USB-IF Compliance	All	Requires firmware on external EEPROM	No external EEPROM required	No external EEPROM required
2	FS-only hub or host connected to HX3 Upstream Port	All	Not supported	Supported	Supported
3	Suspend Power	All	90 mW	37.8 mW	37.8 mW

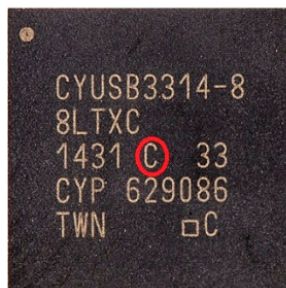
Method of Identification

Markings on row 3 of the HX3 package differentiate Rev. *D Silicon from Rev. *C Silicon and Rev. *A Silicon as indicated in the example below. Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

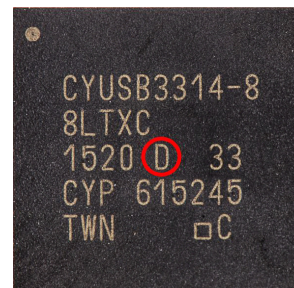
HX3 REV *A SILICON



HX3 REV *C SILICON



HX3 REV *D SILICON



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