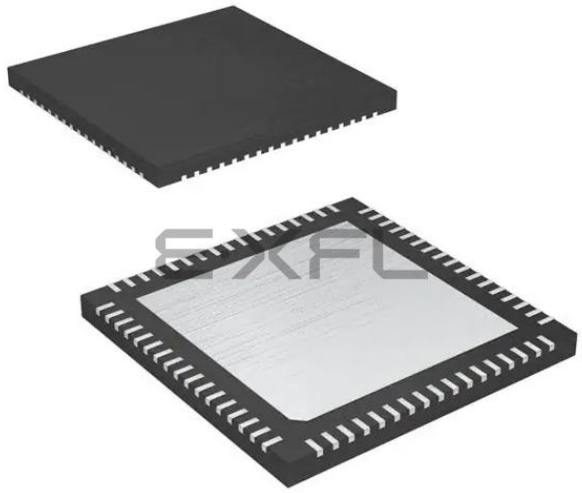

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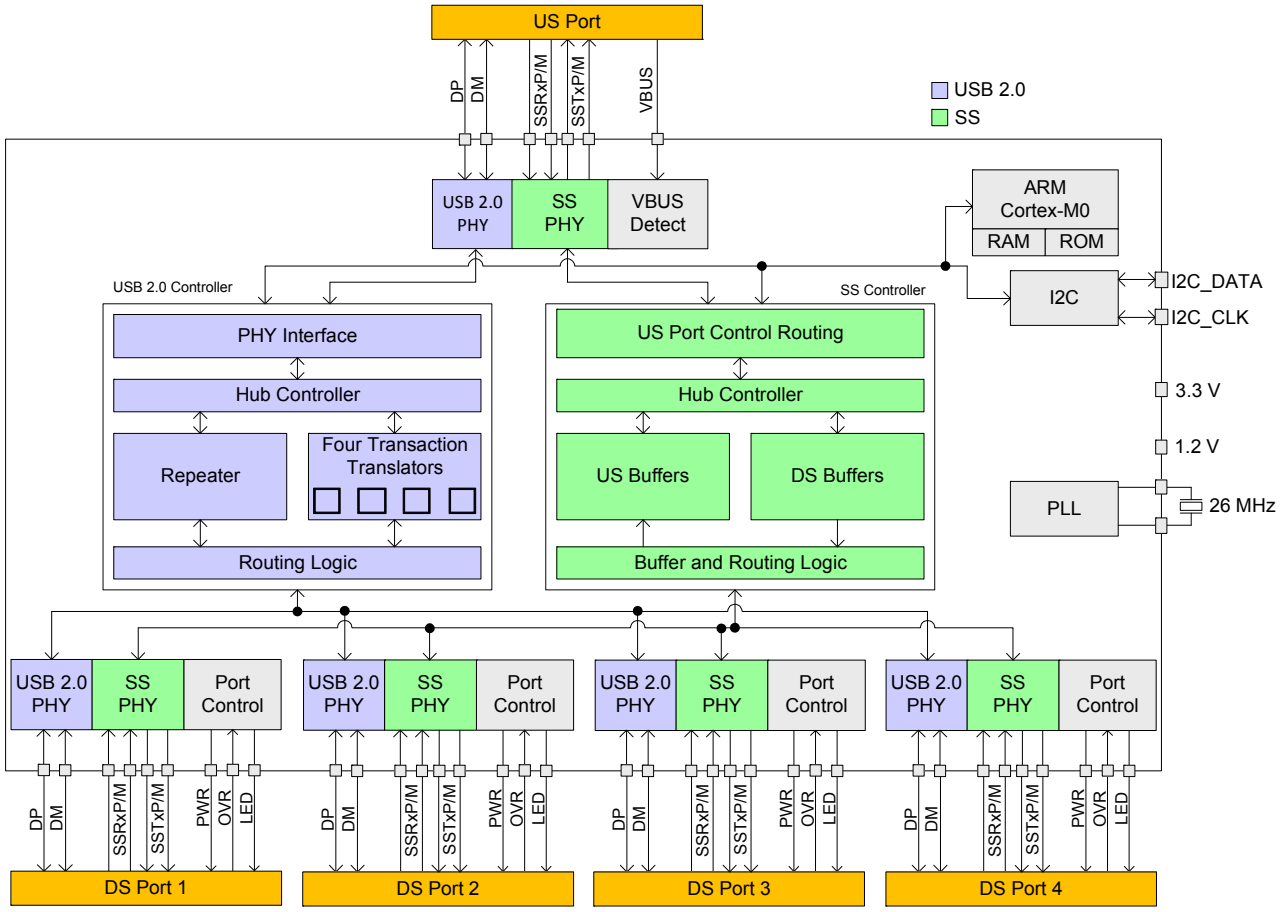
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB 3.0 Hub Controller
Core Processor	ARM® Cortex®-M0
Program Memory Type	ROM (32kB)
Controller Series	CYUSB
RAM Size	16K x 8
Interface	I²C
Number of I/O	10
Voltage - Supply	1.14V ~ 1.26V, 2.5V ~ 2.7V, 3V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3304-68ltxc

Block Diagram



Contents

Architecture Overview

The Block Diagram on page 2 shows the HX3 architecture. HX3 consists of two independent hub controllers (SS and USB 2.0), the Cortex-M0 CPU subsystem, an I^2C interface, and port controller blocks.

SS Hub Controller

This block supports the SS hub functionality based on the USB 3.0 specification. The SS hub controller supports the following:

- SS link power management (U0, U1, U2, U3 states)
- Full-duplex data transmission

USB 2.0 Hub Controller

This block supports the LS, FS, and HS hub functionalities. It includes the repeater, frame timer, and four transaction translators.

The USB 2.0 hub controller block supports the following:

- USB 2.0 link power management (L0, L1, L2, L3 states)
- Suspend, resume, and remote wake-up signaling
- Multi-TT (one TT for each DS port)

CPU

The ARM Cortex-M0 CPU subsystem is used for the following functions:

- System configuration and initialization
- Battery charging control
- Vendor-specific commands for the USB-to-I^2C bridge
- String-descriptor support
- Suspend status indicator
- Shared Link support in embedded systems

I^2C Interface

The I^2C interface in HX3 supports the following:

- I^2C Slave, Master, and Multi-master configurations
  - Configure HX3 by an external I^2C master in I^2C slave mode
  - Configure HX3 from an I^2C EEPROM
  - Multi-master mode to share EEPROM with other I^2C masters
- In-System Programming of the I^2C EEPROM from HX3's US port

Port Controller

The port controller block controls DS port power to comply with the BC v1.2 and USB 3.0 specifications. This block also controls the US port power in the ACA-Dock mode. Control signals for external power switches are implemented within the chip. HX3 controls the external power switches at power-on to reduce in-rush current.

The port controller block supports the following:

- Overcurrent detection
- SS and USB 2.0 port indicators for each DS port
- Ganged and individual power control modes
- Automatic port numbering based on active ports

Applications

- Standalone hubs
- PC and tablet motherboards
- Docking station
- Hand-held cradles
- Monitors
- Digital TVs
- Set-top boxes
- Printers

HX3 Product Options

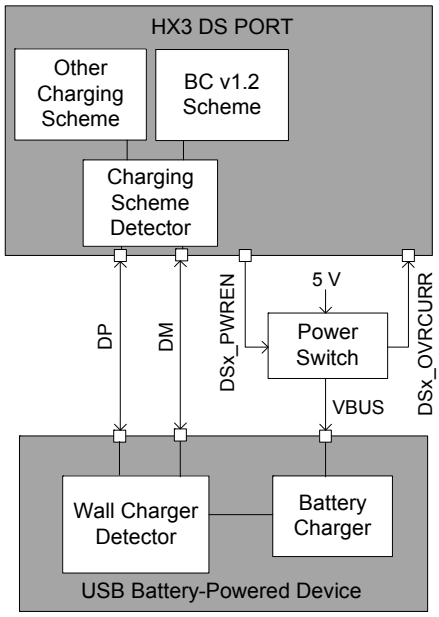
Table 1. HX3 Product Options

Features	CYUSB3302	CYUSB3304	CYUSB3312	CYUSB3314	CYUSB3324	CYUSB3326	CYUSB3328	CYUSB2302-68LTXI	CYUSB2304-68LTXI
Number of DS ports	2 (USB 3.0)	4 (USB 3.0)	2 (USB 3.0)	4 (USB 3.0)	4 (USB 3.0)	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	8 (4 SS, 4 USB 2.0)	2 (USB 2.0)	4 (USB 2.0)
Number of Shared Link ports	0	0	0	0	0	2[1]	4	0	0
BC v1.2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACA-Dock	No	No	No	No	Yes	No	Yes	No	No
External Power Switch Control	Ganged	Ganged	Individual and Ganged	Individual and Ganged	Individual and Ganged	Individual	Individual	Ganged	Ganged
Pin-Strap support	No	No	Yes	Yes	Yes	Yes	Yes	No	No
I^2C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Vendor command	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Port indicators	No	No	Yes	Yes	Yes	No	No	No	No
Packages[2]	68-QFN, 100-ball BGA	68-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	68-QFN, 100-ball BGA	68-QFN, 100-ball BGA
Temperature range	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial (88-QFN only) and Commercial	Industrial and Commercial	Industrial and Commercial

Notes
1. DS1 and DS2 are Shared link Ports.
2. BGA Industrial Grade packages are limited to 1 W of active power. For power calculations refer to Table 10 on page 33.

When the US port is disconnected from the host, HX3 detects if any of the DS ports are connected to a device requesting charging. It determines the charging method and then switches to the appropriate signaling based on the detected charging specification as shown in Figure 4. The hub either emulates a USB-compliant dedicated charging port by connecting DP and DM (see the BC v1.2 specification) or other supported proprietary charging schemes.

Figure 4. Ghost Charge Implementation in HX3



Ghost Charge is enabled by default and can be disabled through configuration. Refer to Configuration Options on page 24.

Vendor-Command Support

HX3 supports vendor-specific requests and can also enumerate as a vendor-specific device. The vendor-specific request can be used to (a) bridge USB and I^2C and (b) configure HX3. This feature can be used for the following applications:

- Firmware upgrade of an external ASSP connected to HX3 through USB
- In-System programming (ISP) of an EEPROM connected to HX3 through USB

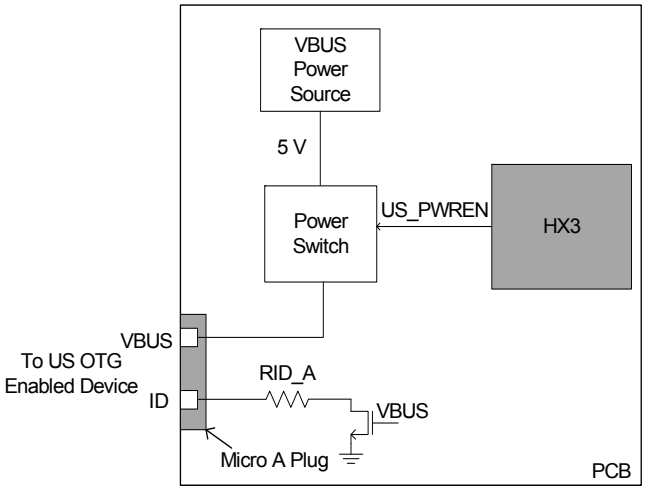
ACA-Dock Support

In traditional USB topologies, the host provides VBUS to enable and charge the connected devices. For OTG hosts, however, an ACA-Dock provides VBUS and a method to charge the host. HX3 supports the ACA-Dock standard (see BC v1.2 specification) by integrating the functions of the adapter controller.

Figure 5 shows the ACA-Dock system. If the ACA-Dock feature is enabled, HX3 turns on the external power switch to drive VBUS on the US port. To inform the OTG host that it is connected to an ACA-Dock, the ID pin is tied to ground using a resistor RID_A,[3] as shown in Figure 5. The ACA-Dock feature can be disabled using the Configuration Options on page 24.

For example, a BC v1.2 compliant phone such as a Sony Xperia (neo V) can be docked to a HX3-based ACA-Dock system. The phone acts as an OTG host and the ACA-Dock charges the phone connected to the US port while also powering the four DS ports.

Figure 5. ACA-Dock Support



Note
3. 124 kΩ is the recommended RID_A value as per BC v1.2 specification, but some portable devices use custom RID_A values.

Figure 8. HX3 100-Ball BGA Pinout for CYUSB3302

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
NC	NC	NC	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**	**B9**	**B10**
NC	NC	NC	VDD_IO	VSS	AVDD33	NC	NC	NC	DVDD12
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**
US_TXM	NC	NC	NC	NC	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**	**D9**	**D10**
US_TXP	NC	NC	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**	**E8**	**E9**	**E10**
DVDD12	RREF_USB2	NC	NC	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**	**F9**	**F10**
US_RXM	VSS	AVDD33	MODE_SEL[1]	DVDD12	OVRCURR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**	**G9**	**G10**
US_RXP	VBUS_DS	SUSPEND	RESERVED1	MODE_SEL[0]	VDD_IO	PWR_EN	I2C_DATA	VSS	DS2_RXM
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**	**H9**	**H10**
AVDD12	VBUS_US	VDD_EFUSE	RESERVED2	RREF_SS	VSS	DS2_TXM	DS2_TXP	NC	AVDD12
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**	**J10**
VSS	AVDD12	VSS	GPIO	NC	I2C_CLK	NC	NC	VSS	NC
K1	**K2**	**K3**	**K4**	**K5**	**K6**	**K7**	**K8**	**K9**	**K10**
NC	NC	DVDD12	NC	NC	NC	NC	NC	DVDD12	NC

Figure 9. HX3 100-Ball BGA Pinout for CYUSB3304

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
NC	DS4_DM	DS4_DP	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**	**B9**	**B10**
NC	NC	NC	VDD_IO	VSS	AVDD33	NC	NC	NC	DVDD12
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**10**
US_TXM	NC	NC	DS3_DP	DS3_DM	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**	**D9**	**D10**
US_TXP	NC	NC	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**	**E8**	**E9**	**E10**
DVDD12	RREF_USB2	NC	NC	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**	**F9**	**F10**
US_RXM	VSS	AVDD33	MODE_SEL[1]	DVDD12	OVRCURR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**	**G9**	**G10**
US_RXP	VBUS_DS	SUSPEND	RESERVED1	MODE_SEL[0]	VDD_IO	PWR_EN	I2C_DATA	VSS	DS2_RXM
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**	**H9**	**H10**
AVDD12	VBUS_US	VDD_EFUSE	RESERVED2	RREF_SS	VSS	DS2_TXM	DS2_TXP	NC	AVDD12
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**	**J10**
VSS	AVDD12	VSS	GPIO	NC	I2C_CLK	NC	NC	VSS	DS3_RXM
K1	**K2**	**K3**	**K4**	**K5**	**K6**	**K7**	**K8**	**K9**	**K10**
DS4_TXP	DS4_TXM	DVDD12	DS4_RXP	DS4_RXM	NC	DS3_TXP	DS3_TXM	DVDD12	DS3_RXP

Table 2. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB3302 and CYUSB3304 *(continued)*

Pin Name		Type	68-QFN Pin#	100-BGA Ball #	Description
CYUSB3302	CYUSB3304				
RESERVED1		I/O	21	G4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
RESERVED2		I	22	H4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
Mode Select, Clock, and Reset					
MODE_SEL[0]		I	23	G5	Device operation mode select bit 0; refer to Table 5 on page 24
MODE_SEL[1]		I	24	F4	Device operation mode select bit 1; refer to Table 5 on page 24
XTL_OUT		A	54	E6	Crystal out
XTL_IN		A	55	E5	Crystal in
RESETN		I	31	F7	Active LOW reset input
I2C_CLK		I/O	32	J6	I^2C clock
I2C_DATA		I/O	33	G8	I^2C data
SUSPEND		I/O	20	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and Ground					
VDD_EFUSE		PWR	19	H3	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V.
AVDD12		PWR	10, 16, 34, 46, 52, 53	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND		PWR	40	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12		PWR	1, 3, 7, 13, 27, 37, 43, 49,	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS _US		PWR	17	H2	This pin must be connected to VBUS from US port
VBUS_DS		PWR	18	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	4, 56, 61, 66	A4, A7, B6, F3	3.3 V analog supply
VDD_IO		PWR	28	B4, E7, G6	3.3 V I/O supply
USB Precision Resistors					
RREF_USB2		A	2	E2	Connect pin to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY.
RREF_SS		A	26	H5	Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration.

Note
4. These pins are Do Not Use (DNU); they must be left floating.

Figure 11. HX3 88-Pin QFN 4-Port Pinout

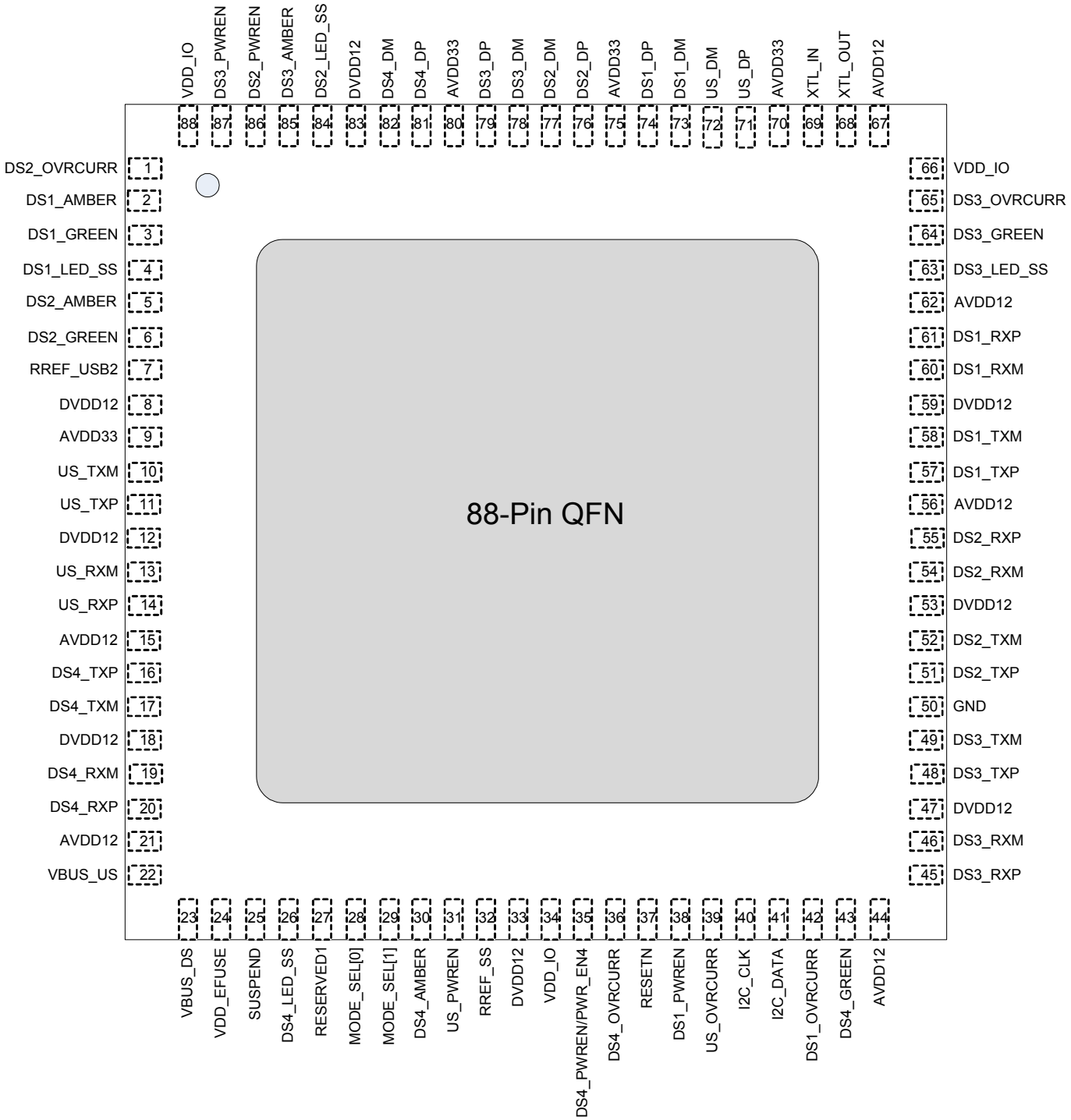


Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314 CYUSB3324 CYUSB3326 CYUSB3328				
US Port					
US_RXP		I	14	G1	SuperSpeed receive plus
US_RXM		I	13	F1	SuperSpeed receive minus
US_TXP		O	11	D1	SuperSpeed transmit plus
US_TXM		O	10	C1	SuperSpeed transmit minus
US_DP		I/O	71	A9	USB 2.0 data plus
US_DM		I/O	72	A8	USB 2.0 data minus
US_OVRCURR		I	39	K6	CYUSB3324/3328: Overcurrent detect input for US port in ACA-Dock mode. If ACA-Dock mode is disabled using Configuration Options on page 24, this pin must be pulled HIGH using a 10 kΩ to VDD_IO. Other part numbers: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
US_PWREN[5]		I/O	31	J5	CYUSB3324/3328: VBUS power enable output for US port in ACA-Dock mode. If ACA-Dock mode is disabled using Configuration Options on page 24, this pin can be left floating if Pin-Strap is not enabled. Other part numbers: This pin can be left floating if Pin-Strap (Pin# 63) is not enabled.
PWR_SW_POL[6]					This pin is called PWR_SW_POL in pin-strap configuration mode.
DS1 Port					
DS1_RXP		I	61	D10	SuperSpeed receive plus
DS1_RXM		I	60	C10	SuperSpeed receive minus
DS1_TXP		O	57	F8	SuperSpeed transmit plus
DS1_TXM		O	58	E8	SuperSpeed transmit minus
DS1_DP		I/O	74	C7	USB 2.0 data plus
DS1_DM		I/O	73	C8	USB 2.0 data minus
DS1_OVRCURR		I	42	J8	Overcurrent detect input for DS1 port
DS1_PWREN[5]		I/O	38	J7	VBUS power enable output for DS1 port. When the port is disabled, this pin is in tristate.
DS1_CDP_EN[6]					This pin is called DS1_CDP_EN in pin-strap configuration mode.
DS1_AMBER[5]		I/O	2	C2	LED_AMBER output for DS1 port
ACA_DOCK[6]					This pin is called ACA-DOCK in pin-strap configuration mode.
DS1_GREEN[5]		I/O	3	D3	CYUSB3312/3314/3324: LED_GREEN output for DS1 port
DS1_VBUSEN_SL[5]					CYUSB3326/3328: VBUS power enable output for SS port 1
PORT_DISABLE[0][6]					This pin is called PORT_DISABLE[0] in pin-strap configuration mode.
DS1_LED_SS[5]		I/O	4	D2	LED_SS output for DS1 port
PORT_DISABLE[1][6]					This pin is called PORT_DISABLE[1] in pin-strap configuration mode.

Notes
5. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
6. For pin-strap configuration details, refer to Table 6 on page 25.

Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X *(continued)*

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314 CYUSB3324 CYUSB3326 CYUSB3328				
DS2 Port					
DS2_RXP		I	55	F10	SuperSpeed receive plus
DS2_RXM		I	54	G10	SuperSpeed receive minus
DS2_TXP		O	51	H8	SuperSpeed transmit plus
DS2_TXM		O	52	H7	SuperSpeed transmit minus
DS2_DP		I/O	76	A6	USB 2.0 data plus
DS2_DM		I/O	77	A5	USB 2.0 data minus
DS2_OVRCURR		I	1	B1	Overcurrent detect input for DS2 port
DS2_PWREN[7]		I/O	86	B2	VBUS power enable output for DS2 port. When the port is disabled, this pin is in tristate.
DS2_CDP_EN[8]					This pin is called DS2_CDP_EN in the pin-strap configuration mode.
DS2_AMBER[7]		I/O	5	E4	LED_AMBER output for DS2 port
NON_REMOVABLE[0][8]					This pin is called NON_REMOVABLE[0] in the pin-strap configuration mode.
DS2_GREEN[7]		I/O	6	E3	CYUSB3312/3314/3324: LED_GREEN output for DS2 port
DS2_VBUSEN_SL[7]					CYUSB3326/3328: VBUS power enable output for SS port 2
NON_REMOVABLE[1][8]					This pin is called NON_REMOVABLE[1] in the pin-strap configuration mode.
DS2_LED_SS[7]		I/O	84	C3	LED_SS output for DS2 port
PWR_EN_SEL[8]					This pin is called PWR_EN_SEL in the pin-strap configuration mode.
DS3 Port					
NC	DS3_RXP	I	45	K10	SuperSpeed receive plus
NC	DS3_RXM	I	46	J10	SuperSpeed receive minus
NC	DS3_TXP	O	48	K7	SuperSpeed transmit plus
NC	DS3_TXM	O	49	K8	SuperSpeed transmit minus
NC	DS3_DP	I/O	79	C4	USB 2.0 data plus
NC	DS3_DM	I/O	78	C5	USB 2.0 data minus
DS3_OVRCURR		I	65	B7	CYUSB3314/3324/3326/3328: Overcurrent detect input for DS3 port CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
DS3_PWREN[7]		I/O	87	A1	VBUS power enable output for DS3 port. When the port is disabled, this pin is in tristate.
DS3_CDP_EN[8]					This pin is called DS3_CDP_EN in the pin-strap configuration mode.
DS3_AMBER[7]		I/O	85	B3	LED_AMBER output for DS3 port
VID_SEL[2][8]					This pin is called VID_SEL[2] in the pin-strap configuration mode.

Notes
7. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
8. For pin-strap configuration details, refer to Table 6 on page 25.

Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X *(continued)*

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312 / CYUSB3314 / CYUSB3324 / CYUSB3326 / CYUSB3328					
DS3_GREEN[9]		I/O	64	B8	CYUSB3312/3314/3324: LED_GREEN output for DS3 port
DS3_VBUSEN_SL[9]					CYUSB3328: VBUS power enable output for SS port 3
VID_SEL[1][10]					This pin is called VID_SEL[1] in the pin-strap configuration mode. For pin-strap configuration details, refer to Table 6 on page 25.
DS3_LED_SS[9]		I/O	63	B9	LED_SS output for DS3 port
PIN_STRAP[10]					This pin is called PIN_STRAP in pin-strap configuration mode. When connected to VDD_IO through a 10-kΩ resistor, this pin enables pin-strap configuration mode for HX3.
DS4 Port					
NC	DS4_RXP	I	20	K4	SuperSpeed receive plus
NC	DS4_RXM	I	19	K5	SuperSpeed receive minus
NC	DS4_TXP	O	16	K1	SuperSpeed transmit plus
NC	DS4_TXM	O	17	K2	SuperSpeed transmit minus
NC	DS4_DP	I/O	81	A3	USB 2.0 data plus
NC	DS4_DM	I/O	82	A2	USB 2.0 data minus
DS4_OVRCURR		I	36	F6	CYUSB3314/3324/3326/3328: Overcurrent detect input for DS4 port. CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
DS4_PWREN/PWR_EN4		I/O	35	G7	VBUS power enable output for DS4 port. This pin is also used as power enable output when configured in ganged power mode using the Blaster Plus tool. When the port is disabled, this pin is in tristate.
DS4_CDP_EN[10]					This pin is called DS4_CDP_EN in the pin-strap configuration mode.
DS4_AMBER[9]		I/O	30	J4	LED_AMBER output for DS4 port
I2C_DEV_ID[10]					This pin is called I2C_DEV_ID in the pin-strap configuration mode.
DS4_GREEN[9]		I/O	43	H9	CYUSB3312/3314/3324: LED_GREEN output for DS4 port
DS4_VBUSEN_SL					CYUSB3328: VBUS power enable output for SS port 4
VID_SEL[0][10]					This pin is called VID_SEL[0] in the pin-strap configuration mode.
DS4_LED_SS		I/O	26	H4	LED_SS output for DS4 port. The LED must be connected to GND as shown in Figure 16 on page 25. If LED is not used, this pin must be pulled HIGH using a 10 kΩ to VDD_IO.
RESERVED1		I	27	G4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
Mode Select, Clock, and Reset					
MODE_SEL[0]		I	28	G5	Device operation mode select bit 0; refer to Table 5 on page 24
MODE_SEL[1]		I	29	F4	Device operation mode select bit 1; refer to Table 5 on page 24
XTL_OUT		A	68	E6	Crystal out
XTL_IN		A	69	E5	Crystal in
RESETN		I	37	F7	Active LOW reset input
I2C_CLK		I/O	40	J6	I^2C clock
I2C_DATA		I/O	41	G8	I^2C data

Notes
9. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
10. For pin-strap configuration details, refer to Table 6 on page 25.

Temperature range of 25 °C–70 °C and programming voltage of 2.5 V–2.7 V.

Pin-Strap Configuration

Pin-straps are supported for select product options (see Table 1 on page 5) to provide reconfigurability without an additional EEPROM. The pin-strap configuration is enabled by pulling the Pin #63 of 88-pin QFN HIGH. Table 6 on page 25 shows the configuration options supported through pin-straps and the GPIOs used for this purpose. Figure 16 and Figure 17 show how the GPIOs need to be connected if pin-strap and LED connection are required or only pin-strap is required.

HX3 samples pin-strap GPIOs at power-up. Floating straps are considered as invalid and the default configuration is used. If PIN_STRAP (Pin #63 of 88-pin QFN) is floating, all strap inputs are considered invalid. A GPIO is considered strapped "1" or "0" when connected with a weak pull-up (10 kΩ) or pull-down (10 kΩ) respectively. After the initial sampling at power-up and reset, the GPIOs are used in their normal functions.

Figure 16. Pin-Strap With LED or LED-Only Connection

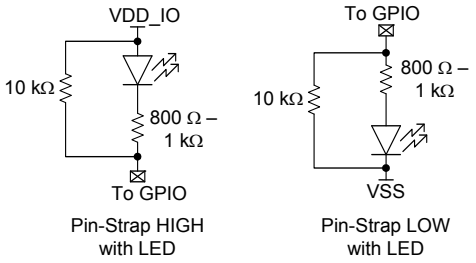


Figure 17. Pin-Strap Connection

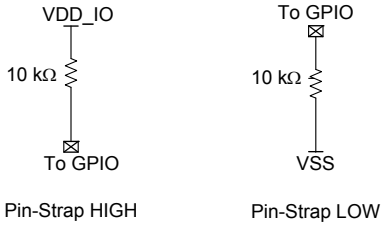


Table 6. Pin-Strap Configuration

88-QFN Pin #	Pin-Strap Name	Strapped '0'[11]		Strapped '1'[11]	
30	I2C_DEV_ID[12]	ID 0: HX3 I²C slave address (7 bits) is 0x60. This is also the default I²C slave address for the 68-pin QFN package.		ID 1: HX3 I²C slave address (7 bits) is 0x58	
31	PWR_SW_POL	Power enable and overcurrent will be active LOW		Power enable and overcurrent will be active HIGH	
2	ACA_DOCK	Disabled		Enabled	
84	PWR_EN_SEL	Individual		Gang	
63	PIN_STRAP[13]	No pin-strapping		Pin-strapping configuration enabled	
4	PORT_DISABLE[1]	PORT_DISABLE[1:0] = b'00: DS1, DS2, DS3, DS4 active b'01: DS1, DS2, DS3 active b'10: DS1, DS2 active b'11: DS1 active Pin-straps cannot enable ports disabled by factory setting.			
3	PORT_DISABLE[0]				
6	NON_REMOVABLE[1][14]	NON_REMOVABLE[1:0] = b'00: DS1, DS2, DS3, DS4 removable b'01: DS1, DS2, DS3 removable b'10: DS1, DS2 removable b'11: DS1 removable			
5	NON_REMOVABLE[0][14]				
85	VID[2]	Reserved. If PIN_STRAP is enabled and CY VID is required, strap VID[2:0] to '1'.			
64	VID[1]				
43	VID[0]				
38	DS1_CDP_EN[15]	strapped '0'	strapped '1'	strapped '0'	strapped '1'
		DS1 CDP enabled	DS1 CDP disabled	DS1 CDP disabled	DS1 CDP enabled
86	DS2_CDP_EN[15]	DS2 CDP enabled	DS2 CDP disabled	DS2 CDP disabled	DS2 CDP enabled
87	DS3_CDP_EN[15]	DS3 CDP enabled	DS3 CDP disabled	DS3 CDP disabled	DS3 CDP enabled
35	DS4_CDP_EN[15]	DS4 CDP enabled	DS4 CDP disabled	DS4 CDP disabled	DS4 CDP enabled

Notes
11. See Figure 16 and Figure 17.
12. I2C_DEV_ID is valid only when HX3 is in I²C slave mode.
13. VID, PORT_DISABLE, NON_REMOVABLE are group straps. If one of the pins in a group strap is floating (INVALID), that group input will be INVALID and the default will not be overwritten.
14. These DS ports are exposed ports and the connected devices can be removed.
15. DSx_CDP_EN will be active LOW input when PWR_SW_POL is set to active LOW; similarly DSx_CDP_EN will be active HIGH input when PWR_SW_POL is set to active HIGH.

Table 7. EEPROM Map *(continued)*

I²C Offset	Bits	Name	Default	Description
9	7:0	DID [7:0]	00 - 88-pin QFN, 10 - 68-pin QFN	Custom Device ID - revision - LSB
10	7:0	DID [15:8]	50	Custom Device ID - revision - MSB
11	7:0	Reserved	0	Reserved
12	7:4	SHARED_LINK_EN	b'0000	Enable Shared Link on DS port bit[7:4]=DS4, DS3, DS2, DS1 0: Shared Link not enabled 1: Shared Link enabled
	3:0	SHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a SuperSpeed port is active. bit[3:0] = DS4, DS3, DS2, DS1 0: Not active 1: Active
13	7:0	POWER_ON_TIME	0x32	Time (in 2-ms intervals) from the time the power-on sequence begins on a port until power is good on that port (bPwron2PwrGood)
14	7:4	REMOVABLE_PORTS [3:0]	b'1111	Indicates if the port is removable. bit[7:4]=DS4, DS3, DS2, DS1 0: Non-removable 1: Removable
	3:0	UHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a USB 2.0 port is active. bit[3:0]=DS4, DS3, DS2, DS1 0: Not active 1: Active
15	7	SS_LED_PIN_CONTROL	0	Port 1–4: SS LED disable 0: DS[1:4]_LED_SS are LEDs. The LED glows when the SS port is active and not in disabled state. 1: DS[1:4]_LED_SS are not LEDs
	6	GREEN_LED_PIN_CONTROL	0	Port 1–4: USB 2.0 Green LED disable 0: DS[1:4]_GREEN are LEDs 1: DS[1:4]_GREEN are not LEDs
	5	AMBER_LED_PIN_CONTROL	0	Port 1–4: USB 2.0 Amber LED disable 0: DS[1:4]_AMBER are LEDs 1: DS[1:4]_AMBER are not LEDs
	4	PORT_INDICATORS	1	Port indicators supported 0: Port indicators are not supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request has no effect. 1: Port indicators are supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request controls the indicators.
	3	COMPOUND_HUB	0	Identifies a compound device. 0: Hub is not part of a compound device. 1: Hub is part of a compound device.
	2:1	Reserved	0	Reserved
	0	GANG	0	1: Ganged power switch enable for all DS ports 0: Individual port power switch enable for each DS port

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature..... –65 °C to +150 °C

Operating temperature ..... –40 °C to +85 °C

Electrostatic discharge voltage ..... 2200 V

Oscillator or crystal frequency ..... 26 MHz ±150 ppm

I/O voltage supply .....3 V to 3.6 V

Maximum input sink current per I/O ..... 4 mA

Electrical Specifications

HX3 meets all USB-IF Electrical Compliance specifications.

DC Electrical Characteristics

Table 8. DC Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
DVDD12	1.2 V core supply	–	1.14	1.2	1.26	V
VDD_EFUSE	eFuse supply	Normal operation	1.14	1.2	1.26	V
		Programming	2.5	2.6	2.7	V
AVDD12	1.2 V analog supply	–	1.14	1.2	1.26	V
VDD_IO	3.3 V I/O supply	–	3	3.3	3.6	V
AVDD33	3.3 V analog supply	–	3	3.3	3.6	V
V_{IH}	Input HIGH voltage	–	0.7 × VDD_IO	–	VDD_IO	V
V_{IL}	Input LOW voltage	–	0	–	0.3 × VDD_IO	V
V_{OH}	Output HIGH voltage	Output HIGH voltage at $I_{OH} \leq +4$ mA	2.4	–	–	V
V_{OL}	Output LOW voltage	Output LOW voltage at $I_{OL} \geq -4$ mA	–	–	0.4	V
I_{OS}	Input sink current	LED GPIO usage	–	–	4	mA
I_{IX}	Input leakage current	All I/O signals held at VDD_IO or GND	–1	–	1	µA
I_{OZ}	Output HI-Z leakage current	–	–	–	10	µA
I_{CC}	1.2 V supplies combined operating current	–	–	410	526	mA
I_{CC}	3.3 V supplies combined operating current	–	–	260	286	mA
V_{RAMP}	Voltage ramp rate on core and I/O supplies	Voltage ramp must be monotonic	0.2	–	50	V/ms
V_N	Noise level permitted on core and I/O supplies	Max p-p noise level permitted on all supplies except AVDD	–	–	100	mV
V_{N_USB}	Noise level permitted on AVDD12 and AVDD33 supply	Max p-p noise level permitted USB supply	–	–	20	mV

Power Consumption

Table 9 provides the power consumption estimates for HX3 under different conditions. Table 10 summarizes the power consumption for various combinations of devices connected to DS ports.

For example, to calculate the HX3 power consumption for three SS devices connected to DS ports (and no device connected to one DS port), and a US port connected to a USB 3.0 host:

Power consumption = [a] + 2*[g] = 492.5 + 2*76 = 644 mW

[a] is the active power consumption for the US port connected to a USB 3.0 host and the SS device connected to the DS port.

[g] is the incremental power consumption for an additional SS device connected to the DS port.

Table 9. Power Consumption Estimates for Various Usage Scenarios

Device Condition	Number and Speed of DS Ports Connected	Typical Consumption			Comments
		Supply Current (mA)		Power (mW)	
		1.2 V	3.3 V		
Suspend [18]	NA	12.0	7.1	37.8	–
Active power with USB 3.0 host [19]	1 SS	204.1	75.0	492.5	[a]
	1 HS	51.2	45.2	210.7	[b]
	1 FS	51.2	34.0	173.7	[c]
	1 SS + 1 HS	218.0	103.4	602.9	[d]
Active power with USB 2.0 host [19, 20]	1 HS	51.2	45.2	210.7	[e]
	1 FS	51.2	34.0	173.7	[f]
Incremental active power for additional DS port	SS	39.4	8.7	76.0	[g]
	HS	7.0	19.8	73.7	[h]
	FS	7.0	14.2	55.2	[i]
Active power saving per disabled DS port[21]	–	10.6	9.6	44.4	[j]

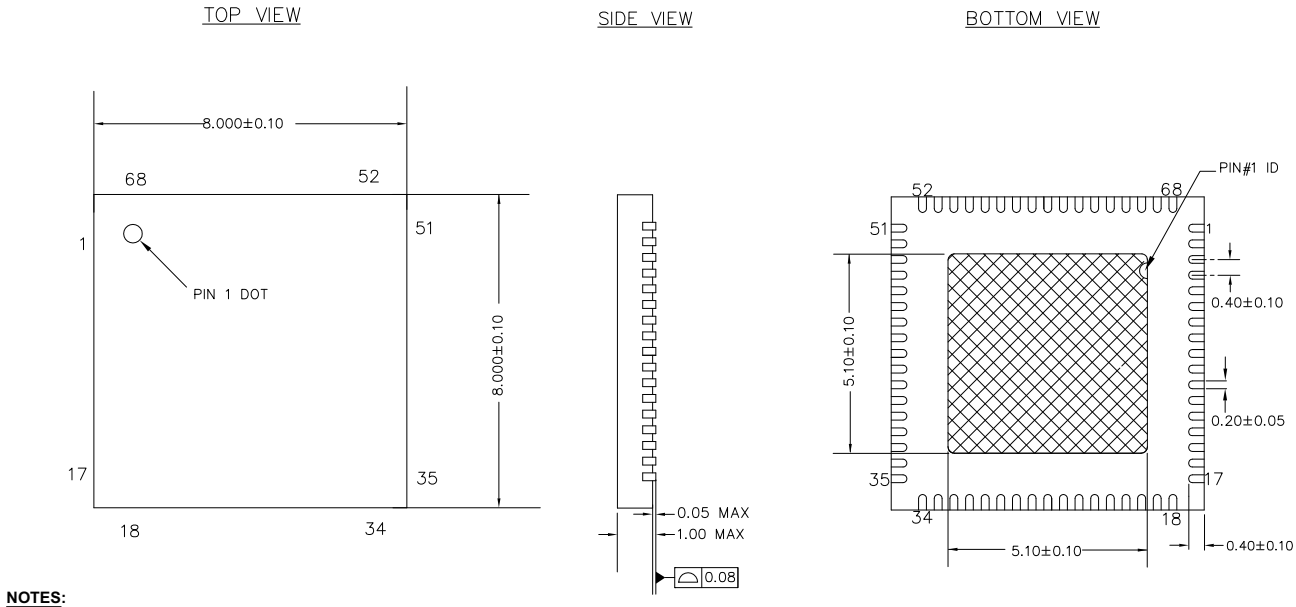
Table 10. Power Consumption Under Various Configurations

Configuration	Number of DS Devices Connected With Data Transfer	Typical Consumption			Comments
		Supply Current (mA)		Power (mW)	
		1.2 V	3.3 V		
USB 3.0 4-Port Hub (USB 3.0 host)	4 SS devices	322	101	720	[a] + 3*[g]
	3 SS + 1 HS devices	297	121	755	[d] + 2*[g]
	3 SS devices	283	92	644	[a] + 2*[g]
USB 3.0 4-Port Hub with one port disabled (USB 3.0 host)	3 SS devices	272	83	600	[a] + 2*[g] - [j]
	2 SS + 1 HS devices	247	103	634	[d] + [g] - [j]
Shared Link with eight DS ports	4 SS + 4 HS devices	357	189	1052	[d] + 3*([g] + [h])
USB 2.0 4-Port Hub (USB 2.0 host)	4 HS devices	72	105	432	[e] + 3*[h]
	3 HS + 1 FS devices	72	99	413	[e] + 2*[h] + [i]

Notes
18. US port in low-power state (SS in U3 and USB 2.0 in L2).
19. All four DS ports are enabled.
20. US SS disabled using configuration options. Refer to Table 7 on page 26 for I^2C configuration options.
21. Power saving applicable only with a USB 3.0 host. DS ports can be disabled through configuration options. Refer to Table 6 on page 25 for pin-strapping and Table 7 on page 26 for I^2C configuration options.

Package Diagrams

Figure 18. 68-pin QFN (8 × 8 × 1.0 mm) LT68B 5.1 × 5.1 mm EPAD (Sawn) Package Outline

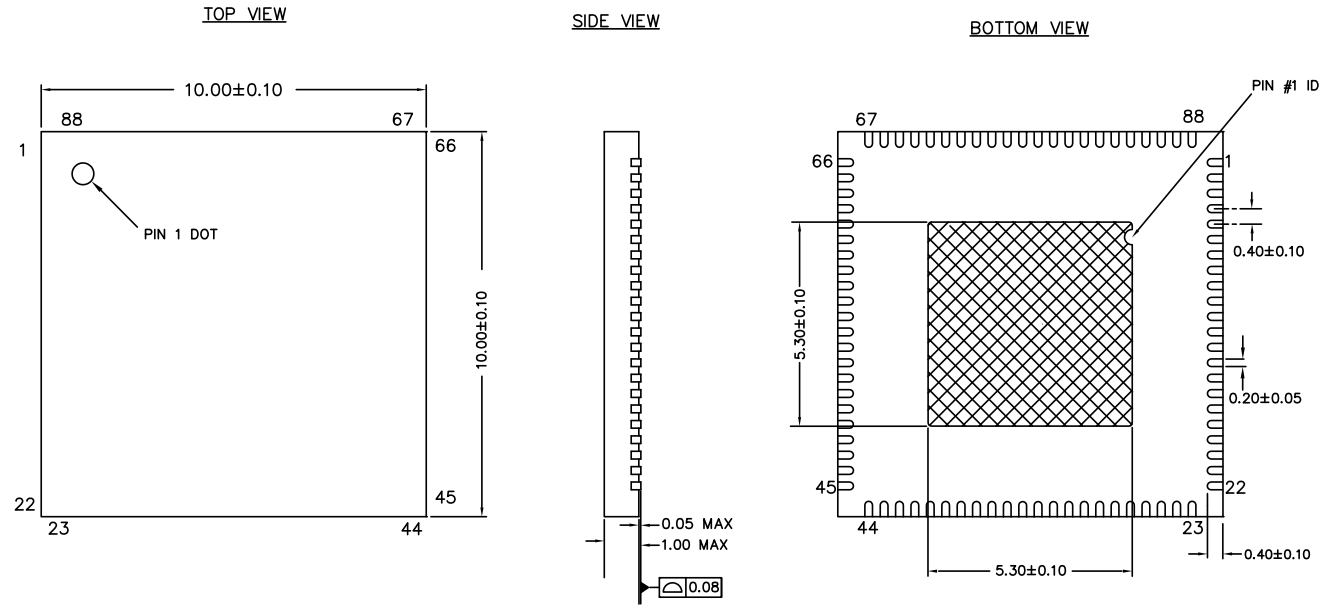


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC#: MO-220
3. ALL DIMENSIONS ARE IN MILLIMETERS

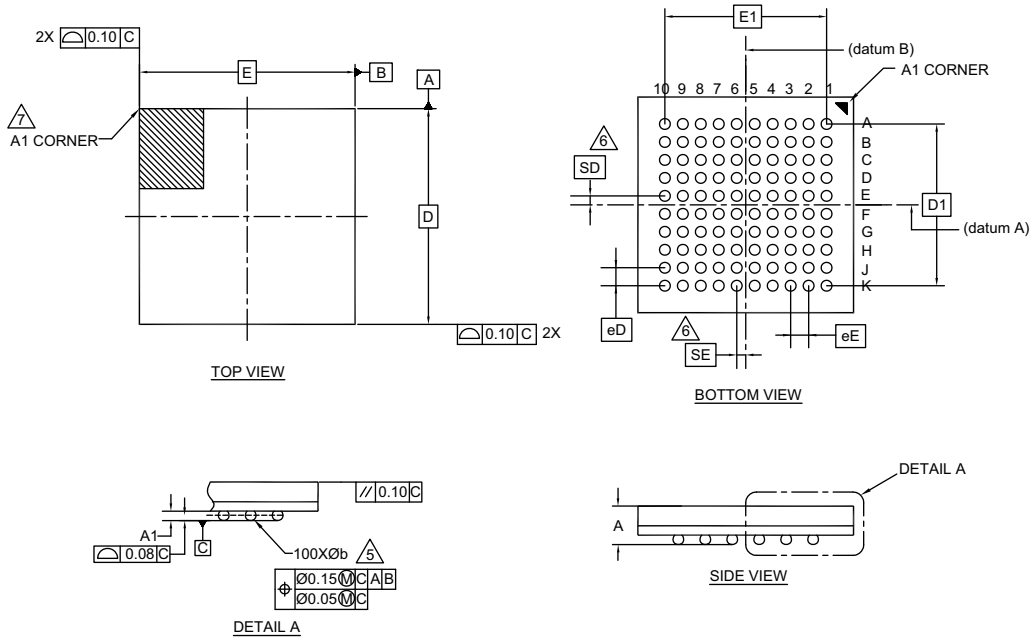
001-78925 *B

Figure 19. 88-pin QFN (10 × 10 × 1.0 mm) LT88B 5.3 × 5.3 EPAD (Sawn) Package Outline



001-76569 *B

Figure 20. 100-Ball BGA (6.0 × 6.0 × 1.0 mm) BZ100 Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	6.00 BSC		
E	6.00 BSC		
D1	4.50 BSC		
E1	4.50 BSC		
MD	10		
ME	10		
N	100		
∅ b	0.25	0.30	0.35
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.25 BSC		
SE	0.25 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-195C.

51-85209 *F

Silicon Revision History

This datasheet is applicable for the USB-IF certified (TID# 330000060) HX3 Rev. *D and Rev. *C Silicon.

Rev. *D: This Silicon revision improves the yield of HX3, and is drop-in compatible for all the part numbers. There is no need to change the board design or layout to use the HX3 Rev. *D Silicon. Products are completely compatible with the HX3 Rev. *C Silicon.

Rev. *C: This Silicon revision fixes the errata applicable to the Rev. *A Silicon.

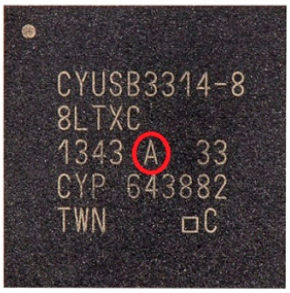
The following table defines the changes between Rev. *A, Rev. *C, and Rev. *D Silicon.

No.	Items	Part Numbers	Rev. *A	Rev. *C	Rev. *D
1	USB-IF Compliance	All	Requires firmware on external EEPROM	No external EEPROM required	No external EEPROM required
2	FS-only hub or host connected to HX3 Upstream Port	All	Not supported	Supported	Supported
3	Suspend Power	All	90 mW	37.8 mW	37.8 mW

Method of Identification

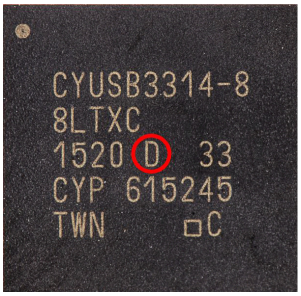
Markings on row 3 of the HX3 package differentiate Rev. *D Silicon from Rev. *C Silicon and Rev. *A Silicon as indicated in the example below. Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

HX3 REV *A SILICON



HX3 REV *C SILICON

HX3 REV *D SILICON



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