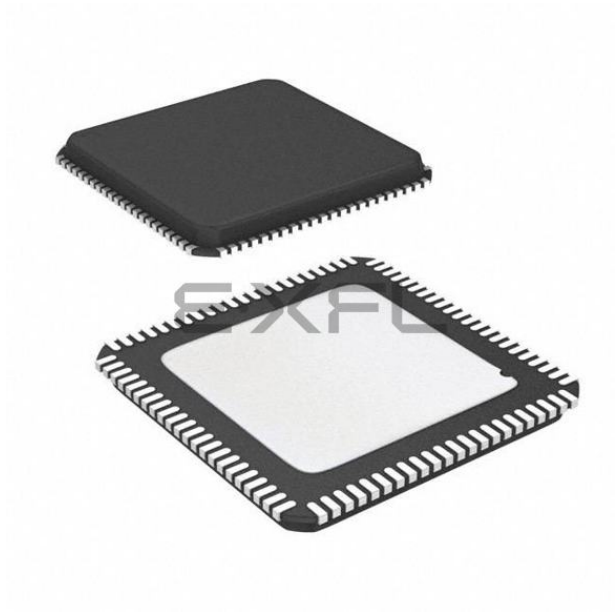

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## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

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## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Active |
| Applications | USB 3.0 Hub Controller |
| Core Processor | ARM® Cortex®-M0 |
| Program Memory Type | ROM (32kB) |
| Controller Series | CYUSB |
| RAM Size | 16K x 8 |
| Interface | I²C |
| Number of I/O | 10 |
| Voltage - Supply | 1.14V ~ 1.26V, 2.5V ~ 2.7V, 3V ~ 3.6V |
| Operating Temperature | 0°C ~ 70°C |
| Mounting Type | Surface Mount |
| Package / Case | 88-VFQFN Exposed Pad |
| Supplier Device Package | 88-QFN (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3312-88ltxct |

## Contents

## HX3 Product Options

### Table 1. HX3 Product Options

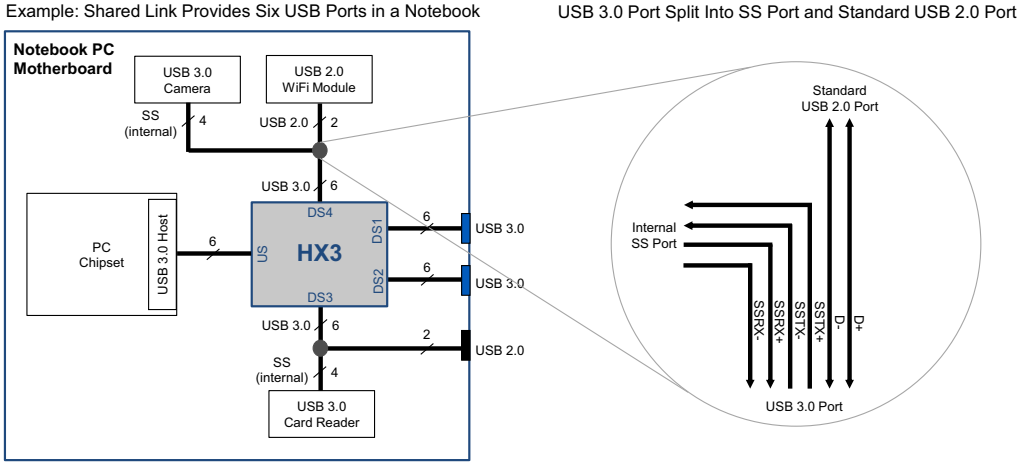
| Features | CYUSB3302 | CYUSB3304 | CYUSB3312 | CYUSB3314 | CYUSB3324 | CYUSB3326 | CYUSB3328 | CYUSB2302-68LTXI | CYUSB2304-68LTXI |
|---|---|---|---|---|---|---|---|---|---|
| Number of DS ports | 2 (USB 3.0) | 4 (USB 3.0) | 2 (USB 3.0) | 4 (USB 3.0) | 4 (USB 3.0) | 6 (2 USB 3.0, 2 SS, 2 USB 2.0) | 8 (4 SS, 4 USB 2.0) | 2 (USB 2.0) | 4 (USB 2.0) |
| Number of Shared Link ports | 0 | 0 | 0 | 0 | 0 | 2[1] | 4 | 0 | 0 |
| BC v1.2 | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| ACA-Dock | No | No | No | No | Yes | No | Yes | No | No |
| External Power Switch Control | Ganged | Ganged | Individual and Ganged | Individual and Ganged | Individual and Ganged | Individual | Individual | Ganged | Ganged |
| Pin-Strap support | No | No | Yes | Yes | Yes | Yes | Yes | No | No |
| $I^2C$ | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Vendor command | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Port indicators | No | No | Yes | Yes | Yes | No | No | No | No |
| Packages[2] | 68-QFN, 100-ball BGA | 68-QFN, 100-ball BGA | 88-QFN, 100-ball BGA | 88-QFN, 100-ball BGA | 88-QFN, 100-ball BGA | 88-QFN, 100-ball BGA | 88-QFN, 100-ball BGA | 68-QFN, 100-ball BGA | 68-QFN, 100-ball BGA |
| Temperature range | Industrial and Commercial | Industrial and Commercial | Industrial and Commercial | Industrial and Commercial | Industrial and Commercial | Industrial and Commercial | Industrial (88-QFN only) and Commercial | Industrial and Commercial | Industrial and Commercial |

**Notes**
1. DS1 and DS2 are Shared link Ports.
2. BGA Industrial Grade packages are limited to 1 W of active power. For power calculations refer to Table 10 on page 33.

# Product Features

## Shared Link

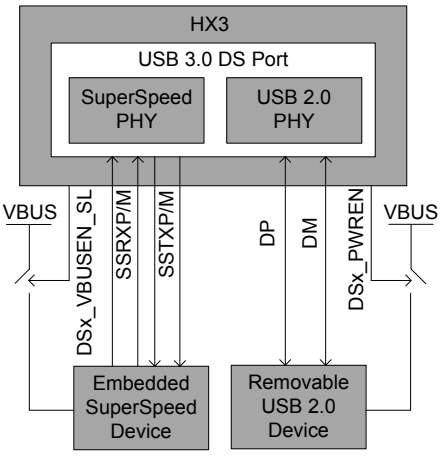
**Figure 1. Application of Shared Link in a Notebook**




Shared Link is a Cypress-proprietary feature that enables a USB 3.0 port to be split into an embedded SS port and a standard USB 2.0 port. Shared Link enables a maximum of eight DS ports from a four-port USB 3.0 hub.

For example, if one of the DS ports is connected to an embedded SS device, such as a USB 3.0 camera, HX3 enables the system designer to reuse the USB 2.0 signals of that specific port to connect to a standard USB 2.0 port. Figure 1 shows how Shared Link can be used in an application.

**Figure 2. DS Port VBUS Control in Shared Link**




The Shared Link mode requires a separate VBUS control for the removable USB 2.0 device and the embedded SS device. Figure 2 shows the VBUS control implementation.

To ensure that the embedded SS device does not fall back to USB 2.0 operation, an external power switch is required. This switch is controlled by HX3, which generates an output signal called DSx_VBUSEN_SL. This signal controls the VBUS for the embedded device.

DSx_PWREN is another output signal generated by HX3 and controls VBUS for the removable USB 2.0 device. For example, when an overcurrent condition occurs, DSx_PWREN turns off the port power.

## Ghost Charge

Ghost Charge is a Cypress-proprietary feature for charging USB devices on the DS port when the US port is not connected to a host. For example, in a docking station with HX3 as shown in Figure 3, when the laptop is undocked, HX3 will emulate a dedicated charging port (DCP) to provide charge to a phone connected on a DS port.

**Figure 3. Ghost Charge**


Charge a smartphone without docking the notebook

## Pin Information

**Figure 6. HX3 68-Pin QFN 2-Port Pinout**

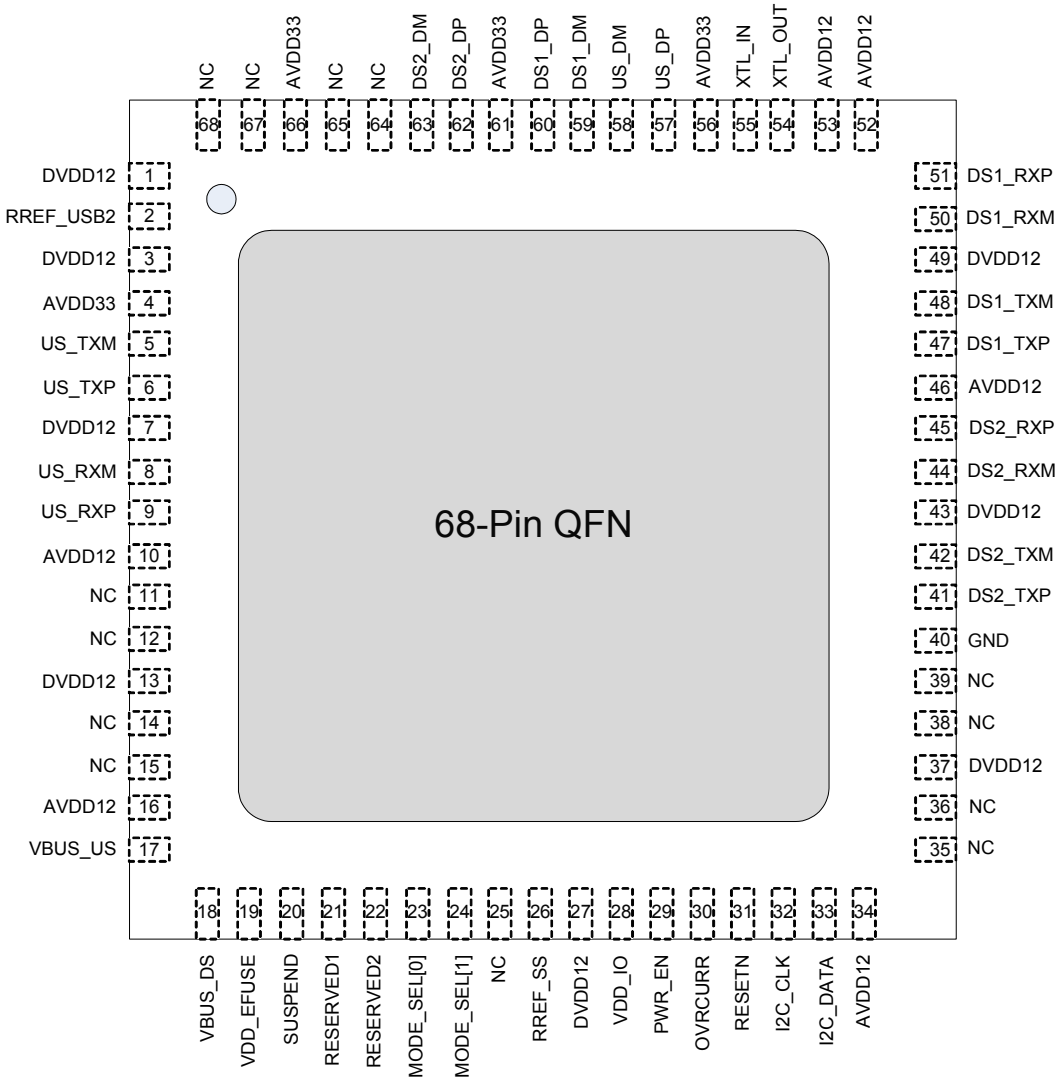


**Figure 7. HX3 68-Pin QFN 4-Port Pinout**

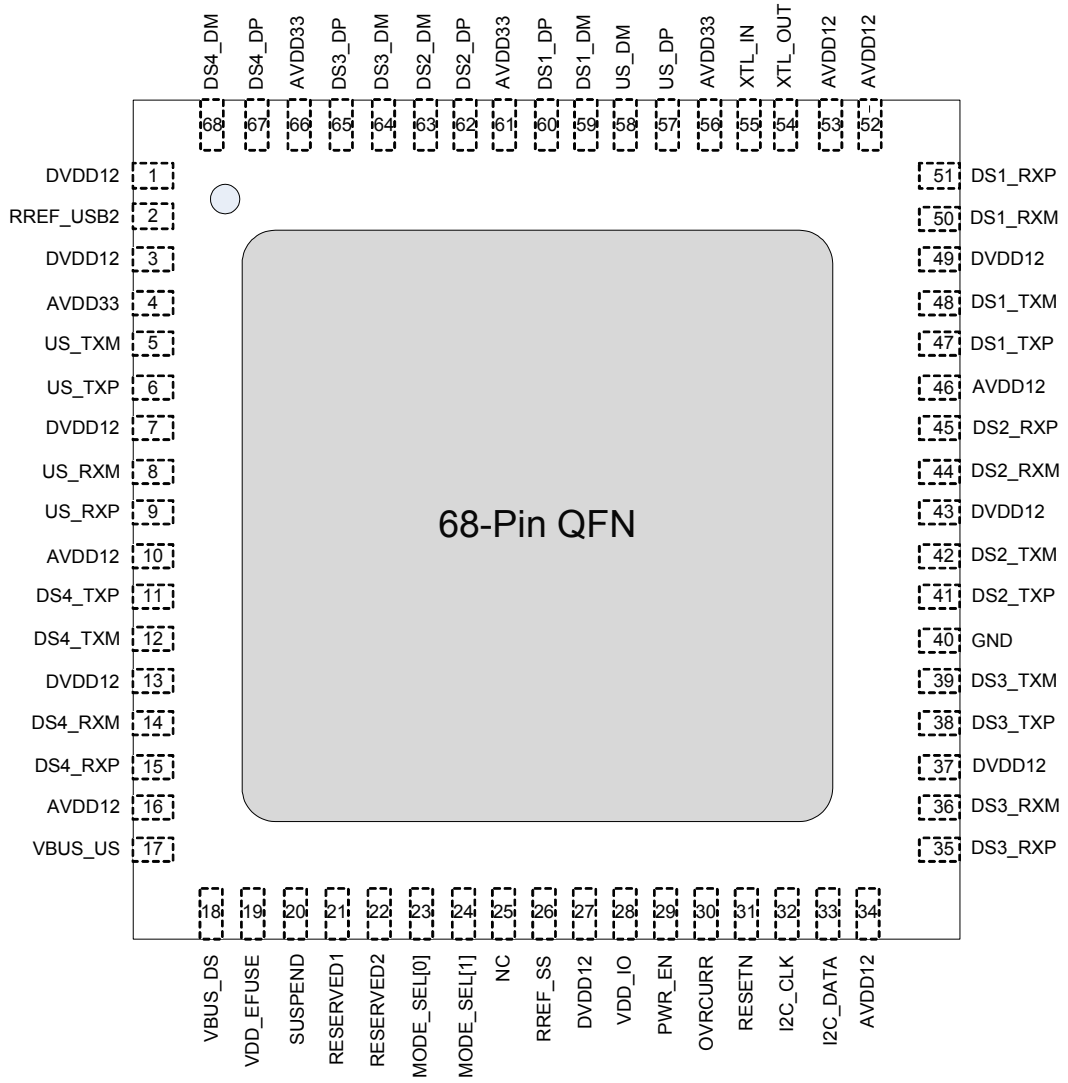


**Table 2. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB3302 and CYUSB3304**

| Pin Name | | Type | 68-QFN Pin# | 100-BGA Ball # | Description |
|---|---|---|---|---|---|
| CYUSB3302 | CYUSB3304 | | | | |
| **US Port** | | | | | |
| US_RXP | | I | 9 | G1 | SuperSpeed receive plus |
| US_RXM | | I | 8 | F1 | SuperSpeed receive minus |
| US_TXP | | O | 6 | D1 | SuperSpeed transmit plus |
| US_TXM | | O | 5 | C1 | SuperSpeed transmit minus |
| US_DP | | I/O | 57 | A9 | USB 2.0 data plus |
| US_DM | | I/O | 58 | A8 | USB 2.0 data minus |
| DS1 Port | | | | | |
| DS1_RXP | | I | 51 | D10 | SuperSpeed receive plus |
| DS1_RXM | | I | 50 | C10 | SuperSpeed receive minus |
| DS1_TXP | | O | 47 | F8 | SuperSpeed transmit plus |
| DS1_TXM | | O | 48 | E8 | SuperSpeed transmit minus |
| DS1_DP | | I/O | 60 | C7 | USB 2.0 data plus |
| DS1_DM | | I/O | 59 | C8 | USB 2.0 data minus |
| **DS2 Port** | | | | | |
| DS2_RXP | | I | 45 | F10 | SuperSpeed receive plus |
| DS2_RXM | | I | 44 | G10 | SuperSpeed receive minus |
| DS2_TXP | | O | 41 | H8 | SuperSpeed transmit plus |
| DS2_TXM | | O | 42 | H7 | SuperSpeed transmit minus |
| DS2_DP | | I/O | 62 | A6 | USB 2.0 data plus |
| DS2_DM | | I/O | 63 | A5 | USB 2.0 data minus |
| **DS3 Port** | | | | | |
| NC | DS3_RXP | I | 35 | K10 | SuperSpeed receive plus |
| NC | DS3_RXM | I | 36 | J10 | SuperSpeed receive minus |
| NC | DS3_TXP | O | 38 | K7 | SuperSpeed transmit plus |
| NC | DS3_TXM | O | 39 | K8 | SuperSpeed transmit minus |
| NC | DS3_DP | I/O | 65 | C4 | USB 2.0 data plus |
| NC | DS3_DM | I/O | 64 | C5 | USB 2.0 data minus |
| **DS4 Port** | | | | | |
| NC | DS4_RXP | I | 15 | K4 | SuperSpeed receive plus |
| NC | DS4_RXM | I | 14 | K5 | SuperSpeed receive minus |
| NC | DS4_TXP | O | 11 | K1 | SuperSpeed transmit plus |
| NC | DS4_TXM | O | 12 | K2 | SuperSpeed transmit minus |
| NC | DS4_DP | I/O | 67 | A3 | USB 2.0 data plus |
| NC | DS4_DM | I/O | 68 | A2 | USB 2.0 data minus |
| OVRCURR | | I | 30 | F6 | Ganged overcurrent input |
| PWR_EN | | I/O | 29 | G7 | Ganged power enable output |
| NC | | I/O | 25 | NA | NC |

**Table 2. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB3302 and CYUSB3304** *(continued)*

| Pin Name | | Type | 68-QFN Pin# | 100-BGA Ball # | Description |
|---|---|---|---|---|---|
| CYUSB3302 | CYUSB3304 | | | | |
| RESERVED1 | | I/O | 21 | G4 | This pin must be pulled HIGH using a 10 kΩ to VDD_IO. |
| RESERVED2 | | I | 22 | H4 | This pin must be pulled HIGH using a 10 kΩ to VDD_IO. |
| **Mode Select, Clock, and Reset** | | | | | |
| MODE_SEL[0] | | I | 23 | G5 | Device operation mode select bit 0; refer to Table 5 on page 24 |
| MODE_SEL[1] | | I | 24 | F4 | Device operation mode select bit 1; refer to Table 5 on page 24 |
| XTL_OUT | | A | 54 | E6 | Crystal out |
| XTL_IN | | A | 55 | E5 | Crystal in |
| RESETN | | I | 31 | F7 | Active LOW reset input |
| I2C_CLK | | I/O | 32 | J6 | $I^2C$ clock |
| I2C_DATA | | I/O | 33 | G8 | $I^2C$ data |
| SUSPEND | | I/O | 20 | G3 | Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state. |
| **Power and Ground** | | | | | |
| VDD_EFUSE | | PWR | 19 | H3 | 1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V. |
| AVDD12 | | PWR | 10, 16, 34, 46, 52, 53 | A10, C9, F9, H1, H10, J2 | 1.2 V analog supply |
| GND | | PWR | 40 | B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9 | GND pin |
| DVDD12 | | PWR | 1, 3, 7, 13, 27, 37, 43, 49, | B10, D4, D6, D8, E1, E10, F5, K3, K9 | 1.2 V core supply |
| VBUS _US | | PWR | 17 | H2 | This pin must be connected to VBUS from US port |
| VBUS_DS | | PWR | 18 | G2 | This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply. |
| AVDD33 | | PWR | 4, 56, 61, 66 | A4, A7, B6, F3 | 3.3 V analog supply |
| VDD_IO | | PWR | 28 | B4, E7, G6 | 3.3 V I/O supply |
| **USB Precision Resistors** | | | | | |
| RREF_USB2 | | A | 2 | E2 | Connect pin to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY. |
| RREF_SS | | A | 26 | H5 | Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration. |

**Note**
4. These pins are Do Not Use (DNU); they must be left floating.

**Table 3. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB2302 and CYUSB2304**

| Pin Name | | Type | 68-QFN Pin# | 100-BGA Ball # | Description |
|---|---|---|---|---|---|
| CYUSB2302 | CYUSB2304 | | | | |
| **US Port** | | | | | |
| NC | | I | 9 | G1 | SuperSpeed receive plus |
| NC | | I | 8 | F1 | SuperSpeed receive minus |
| NC | | O | 6 | D1 | SuperSpeed transmit plus |
| NC | | O | 5 | C1 | SuperSpeed transmit minus |
| US_DP | | I/O | 57 | A9 | USB 2.0 data plus |
| US_DM | | I/O | 58 | A8 | USB 2.0 data minus |
| DS1 Port | | | | | |
| NC | | I | 51 | D10 | SuperSpeed receive plus |
| NC | | I | 50 | C10 | SuperSpeed receive minus |
| NC | | O | 47 | F8 | SuperSpeed transmit plus |
| NC | | O | 48 | E8 | SuperSpeed transmit minus |
| DS1_DP | | I/O | 60 | C7 | USB 2.0 data plus |
| DS1_DM | | I/O | 59 | C8 | USB 2.0 data minus |
| **DS2 Port** | | | | | |
| NC | | I | 45 | F10 | SuperSpeed receive plus |
| NC | | I | 44 | G10 | SuperSpeed receive minus |
| NC | | O | 41 | H8 | SuperSpeed transmit plus |
| NC | | O | 42 | H7 | SuperSpeed transmit minus |
| DS2_DP | | I/O | 62 | A6 | USB 2.0 data plus |
| DS2_DM | | I/O | 63 | A5 | USB 2.0 data minus |
| **DS3 Port** | | | | | |
| NC | NC | I | 35 | K10 | SuperSpeed receive plus |
| NC | NC | I | 36 | J10 | SuperSpeed receive minus |
| NC | NC | O | 38 | K7 | SuperSpeed transmit plus |
| NC | NC | O | 39 | K8 | SuperSpeed transmit minus |
| NC | DS3_DP | I/O | 65 | C4 | USB 2.0 data plus |
| NC | DS3_DM | I/O | 64 | C5 | USB 2.0 data minus |
| **DS4 Port** | | | | | |
| NC | NC | I | 15 | K4 | SuperSpeed receive plus |
| NC | NC | I | 14 | K5 | SuperSpeed receive minus |
| NC | NC | O | 11 | K1 | SuperSpeed transmit plus |
| NC | NC | O | 12 | K2 | SuperSpeed transmit minus |
| NC | DS4_DP | I/O | 67 | A3 | USB 2.0 data plus |
| NC | DS4_DM | I/O | 68 | A2 | USB 2.0 data minus |
| OVRCURR | | I | 30 | F6 | Ganged overcurrent input |
| PWR_EN | | I/O | 29 | G7 | Ganged power enable output |
| NC | | I/O | 25 | NA | NC |

**Table 3. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB2302 and CYUSB2304** *(continued)*

| Pin Name | | Type | 68-QFN Pin# | 100-BGA Ball # | Description |
|---|---|---|---|---|---|
| CYUSB2302 | CYUSB2304 | | | | |
| RESERVED1 | | I/O | 21 | G4 | This pin must be pulled HIGH using a 10 kΩ to VDD_IO. |
| RESERVED2 | | I | 22 | H4 | This pin must be pulled HIGH using a 10 kΩ to VDD_IO. |
| **Mode Select, Clock, and Reset** | | | | | |
| MODE_SEL[0] | | I | 23 | G5 | Device operation mode select bit 0; refer to Table 5 on page 24 |
| MODE_SEL[1] | | I | 24 | F4 | Device operation mode select bit 1; refer to Table 5 on page 24 |
| XTL_OUT | | A | 54 | E6 | Crystal out |
| XTL_IN | | A | 55 | E5 | Crystal in |
| RESETN | | I | 31 | F7 | Active LOW reset input |
| I2C_CLK | | I/O | 32 | J6 | $I^2C$ clock |
| I2C_DATA | | I/O | 33 | G8 | $I^2C$ data |
| SUSPEND | | I/O | 20 | G3 | Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state. |
| **Power and Ground** | | | | | |
| VDD_EFUSE | | PWR | 19 | H3 | 1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V. |
| AVDD12 | | PWR | 10, 16, 34, 46, 52, 53 | A10, C9, F9, H1, H10, J2 | 1.2 V analog supply |
| GND | | PWR | 40 | B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9 | GND pin |
| DVDD12 | | PWR | 1, 3, 7, 13, 27, 37, 43, 49, | B10, D4, D6, D8, E1, E10, F5, K3, K9 | 1.2 V core supply |
| VBUS _US | | PWR | 17 | H2 | This pin must be connected to VBUS from US port |
| VBUS_DS | | PWR | 18 | G2 | This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply. |
| AVDD33 | | PWR | 4, 56, 61, 66 | A4, A7, B6, F3 | 3.3 V analog supply |
| VDD_IO | | PWR | 28 | B4, E7, G6 | 3.3 V I/O supply |
| **USB Precision Resistors** | | | | | |
| RREF_USB2 | | A | 2 | E2 | Connect pin to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY. |
| RREF_SS | | A | 26 | H5 | Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration. |

**Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X** *(continued)*

| Pin Name | | Type | Pin# | Ball# | Description |
|---|---|---|---|---|---|
| CYUSB3312 | CYUSB3314<br>CYUSB3324<br>CYUSB3326<br>CYUSB3328 | | | | |
| **DS2 Port** | | | | | |
| DS2_RXP | | I | 55 | F10 | SuperSpeed receive plus |
| DS2_RXM | | I | 54 | G10 | SuperSpeed receive minus |
| DS2_TXP | | O | 51 | H8 | SuperSpeed transmit plus |
| DS2_TXM | | O | 52 | H7 | SuperSpeed transmit minus |
| DS2_DP | | I/O | 76 | A6 | USB 2.0 data plus |
| DS2_DM | | I/O | 77 | A5 | USB 2.0 data minus |
| DS2_OVRCURR | | I | 1 | B1 | Overcurrent detect input for DS2 port |
| DS2_PWREN[7] | | I/O | 86 | B2 | VBUS power enable output for DS2 port. When the port is disabled, this pin is in tristate. |
| DS2_CDP_EN[8] | | | | | This pin is called DS2_CDP_EN in the pin-strap configuration mode. |
| DS2_AMBER[7] | | I/O | 5 | E4 | LED_AMBER output for DS2 port |
| NON_REMOVABLE[0][8] | | | | | This pin is called NON_REMOVABLE[0] in the pin-strap configuration mode. |
| DS2_GREEN[7] | | I/O | 6 | E3 | CYUSB3312/3314/3324: LED_GREEN output for DS2 port |
| DS2_VBUSEN_SL[7] | | | | | CYUSB3326/3328: VBUS power enable output for SS port 2 |
| NON_REMOVABLE[1][8] | | | | | This pin is called NON_REMOVABLE[1] in the pin-strap configuration mode. |
| DS2_LED_SS[7] | | I/O | 84 | C3 | LED_SS output for DS2 port |
| PWR_EN_SEL[8] | | | | | This pin is called PWR_EN_SEL in the pin-strap configuration mode. |
| **DS3 Port** | | | | | |
| NC | DS3_RXP | I | 45 | K10 | SuperSpeed receive plus |
| NC | DS3_RXM | I | 46 | J10 | SuperSpeed receive minus |
| NC | DS3_TXP | O | 48 | K7 | SuperSpeed transmit plus |
| NC | DS3_TXM | O | 49 | K8 | SuperSpeed transmit minus |
| NC | DS3_DP | I/O | 79 | C4 | USB 2.0 data plus |
| NC | DS3_DM | I/O | 78 | C5 | USB 2.0 data minus |
| DS3_OVRCURR | | I | 65 | B7 | CYUSB3314/3324/3326/3328: Overcurrent detect input for DS3 port<br>CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO. |
| DS3_PWREN[7] | | I/O | 87 | A1 | VBUS power enable output for DS3 port. When the port is disabled, this pin is in tristate. |
| DS3_CDP_EN[8] | | | | | This pin is called DS3_CDP_EN in the pin-strap configuration mode. |
| DS3_AMBER[7] | | I/O | 85 | B3 | LED_AMBER output for DS3 port |
| VID_SEL[2][8] | | | | | This pin is called VID_SEL[2] in the pin-strap configuration mode. |

**Notes**
7. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
8. For pin-strap configuration details, refer to Table 6 on page 25.

**Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X** *(continued)*

| Pin Name | | Type | Pin# | Ball# | Description |
|---|---|---|---|---|---|
| CYUSB3312 / CYUSB3314 / CYUSB3324 / CYUSB3326 / CYUSB3328 | | | | | |
| DS3_GREEN[9] | | I/O | 64 | B8 | CYUSB3312/3314/3324: LED_GREEN output for DS3 port |
| DS3_VBUSEN_SL[9] | | | | | CYUSB3328: VBUS power enable output for SS port 3 |
| VID_SEL[1][10] | | | | | This pin is called VID_SEL[1] in the pin-strap configuration mode. For pin-strap configuration details, refer to Table 6 on page 25. |
| DS3_LED_SS[9] | | I/O | 63 | B9 | LED_SS output for DS3 port |
| PIN_STRAP[10] | | | | | This pin is called PIN_STRAP in pin-strap configuration mode. When connected to VDD_IO through a 10-kΩ resistor, this pin enables pin-strap configuration mode for HX3. |
| **DS4 Port** | | | | | |
| NC | DS4_RXP | I | 20 | K4 | SuperSpeed receive plus |
| NC | DS4_RXM | I | 19 | K5 | SuperSpeed receive minus |
| NC | DS4_TXP | O | 16 | K1 | SuperSpeed transmit plus |
| NC | DS4_TXM | O | 17 | K2 | SuperSpeed transmit minus |
| NC | DS4_DP | I/O | 81 | A3 | USB 2.0 data plus |
| NC | DS4_DM | I/O | 82 | A2 | USB 2.0 data minus |
| DS4_OVRCURR | | I | 36 | F6 | CYUSB3314/3324/3326/3328: Overcurrent detect input for DS4 port. CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO. |
| DS4_PWREN/PWR_EN4 | | I/O | 35 | G7 | VBUS power enable output for DS4 port. This pin is also used as power enable output when configured in ganged power mode using the Blaster Plus tool. When the port is disabled, this pin is in tristate. |
| DS4_CDP_EN[10] | | | | | This pin is called DS4_CDP_EN in the pin-strap configuration mode. |
| DS4_AMBER[9] | | I/O | 30 | J4 | LED_AMBER output for DS4 port |
| I2C_DEV_ID[10] | | | | | This pin is called I2C_DEV_ID in the pin-strap configuration mode. |
| DS4_GREEN[9] | | I/O | 43 | H9 | CYUSB3312/3314/3324: LED_GREEN output for DS4 port |
| DS4_VBUSEN_SL | | | | | CYUSB3328: VBUS power enable output for SS port 4 |
| VID_SEL[0][10] | | | | | This pin is called VID_SEL[0] in the pin-strap configuration mode. |
| DS4_LED_SS | | I/O | 26 | H4 | LED_SS output for DS4 port. The LED must be connected to GND as shown in Figure 16 on page 25. If LED is not used, this pin must be pulled HIGH using a 10 kΩ to VDD_IO. |
| RESERVED1 | | I | 27 | G4 | This pin must be pulled HIGH using a 10 kΩ to VDD_IO. |
| **Mode Select, Clock, and Reset** | | | | | |
| MODE_SEL[0] | | I | 28 | G5 | Device operation mode select bit 0; refer to Table 5 on page 24 |
| MODE_SEL[1] | | I | 29 | F4 | Device operation mode select bit 1; refer to Table 5 on page 24 |
| XTL_OUT | | A | 68 | E6 | Crystal out |
| XTL_IN | | A | 69 | E5 | Crystal in |
| RESETN | | I | 37 | F7 | Active LOW reset input |
| I2C_CLK | | I/O | 40 | J6 | $I^2C$ clock |
| I2C_DATA | | I/O | 41 | G8 | $I^2C$ data |

**Notes**
9. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
10. For pin-strap configuration details, refer to Table 6 on page 25.

Temperature range of 25 °C–70 °C and programming voltage of 2.5 V–2.7 V.

*Pin-Strap Configuration*

Pin-straps are supported for select product options (see Table 1 on page 5) to provide reconfigurability without an additional EEPROM. The pin-strap configuration is enabled by pulling the Pin #63 of 88-pin QFN HIGH. Table 6 on page 25 shows the configuration options supported through pin-straps and the GPIOs used for this purpose. Figure 16 and Figure 17 show how the GPIOs need to be connected if pin-strap and LED connection are required or only pin-strap is required.

HX3 samples pin-strap GPIOs at power-up. Floating straps are considered as invalid and the default configuration is used. If PIN_STRAP (Pin #63 of 88-pin QFN) is floating, all strap inputs are considered invalid. A GPIO is considered strapped "1" or "0" when connected with a weak pull-up (10 kΩ) or pull-down (10 kΩ) respectively. After the initial sampling at power-up and reset, the GPIOs are used in their normal functions.

**Figure 16. Pin-Strap With LED or LED-Only Connection**

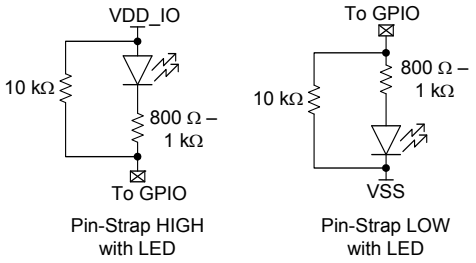



**Figure 17. Pin-Strap Connection**

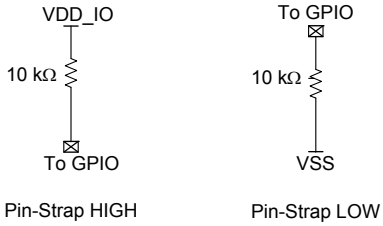



**Table 6. Pin-Strap Configuration**

| 88-QFN Pin # | Pin-Strap Name | Strapped '0'[11] | | Strapped '1'[11] | |
|---|---|---|---|---|---|
| 30 | I2C_DEV_ID[12] | ID 0: HX3 I²C slave address (7 bits) is 0x60. This is also the default I²C slave address for the 68-pin QFN package. | | ID 1: HX3 I²C slave address (7 bits) is 0x58 | |
| 31 | PWR_SW_POL | Power enable and overcurrent will be active LOW | | Power enable and overcurrent will be active HIGH | |
| 2 | ACA_DOCK | Disabled | | Enabled | |
| 84 | PWR_EN_SEL | Individual | | Gang | |
| 63 | PIN_STRAP[13] | No pin-strapping | | Pin-strapping configuration enabled | |
| 4 | PORT_DISABLE[1] | PORT_DISABLE[1:0] =<br>b'00: DS1, DS2, DS3, DS4 active<br>b'01: DS1, DS2, DS3 active<br>b'10: DS1, DS2 active<br>b'11: DS1 active<br>Pin-straps cannot enable ports disabled by factory setting. | | | |
| 3 | PORT_DISABLE[0] | | | | |
| 6 | NON_REMOVABLE[1][14] | NON_REMOVABLE[1:0] =<br>b'00: DS1, DS2, DS3, DS4 removable<br>b'01: DS1, DS2, DS3 removable<br>b'10: DS1, DS2 removable<br>b'11: DS1 removable | | | |
| 5 | NON_REMOVABLE[0][14] | | | | |
| 85 | VID[2] | Reserved. If PIN_STRAP is enabled and CY VID is required, strap VID[2:0] to '1'. | | | |
| 64 | VID[1] | | | | |
| 43 | VID[0] | | | | |
| 38 | DS1_CDP_EN[15] | strapped '0' | strapped '1' | strapped '0' | strapped '1' |
| | | DS1 CDP enabled | DS1 CDP disabled | DS1 CDP disabled | DS1 CDP enabled |
| 86 | DS2_CDP_EN[15] | DS2 CDP enabled | DS2 CDP disabled | DS2 CDP disabled | DS2 CDP enabled |
| 87 | DS3_CDP_EN[15] | DS3 CDP enabled | DS3 CDP disabled | DS3 CDP disabled | DS3 CDP enabled |
| 35 | DS4_CDP_EN[15] | DS4 CDP enabled | DS4 CDP disabled | DS4 CDP disabled | DS4 CDP enabled |

**Notes**
11. See Figure 16 and Figure 17.
12. I2C_DEV_ID is valid only when HX3 is in I²C slave mode.
13. VID, PORT_DISABLE, NON_REMOVABLE are group straps. If one of the pins in a group strap is floating (INVALID), that group input will be INVALID and the default will not be overwritten.
14. These DS ports are exposed ports and the connected devices can be removed.
15. DSx_CDP_EN will be active LOW input when PWR_SW_POL is set to active LOW; similarly DSx_CDP_EN will be active HIGH input when PWR_SW_POL is set to active HIGH.

### *I²C Configuration*

When enabled for I²C configuration through the MODE_SEL pins (See Table 5 on page 24), HX3 can be configured as an I²C master or as an I²C slave. HX3's configuration data is a maximum of 197 bytes and HX3's firmware is 10 KB. Note that HX3's firmware also includes configuration settings.

### *HX3 as I²C Master*

HX3 reads configurations from an external I²C EEPROM with sizes ranging from 16 to 64 KB. An example of a supported EEPROM is 24LC128. Based on the contents of the bSignature and bImageType fields in Table 7 on page 26, HX3 performs one of the following actions:

- Loads custom configuration settings from the EEPROM when bSignature is "CY" and bImageType is 0xD4.
- Loads the Cypress-provided firmware from the EEPROM when bSignature is "CY" and bImageType is 0xB0. This firmware also includes configuration settings.
- If bSignature ≠ "CY", HX3 enumerates in the vendor-specific mode.

The contents of the EEPROM can be updated with the easy-to-use Cypress Blaster Plus tool. Blaster Plus is a GUI-based tool to configure HX3. This tool allows to do the following:

- Download the Cypress-provided firmware from a PC via HX3's US port and store it on an EEPROM connected to HX3's I²C port.
- Read the configuration settings from the EEPROM. These settings are displayed in the Blaster Plus GUI. Modify settings as required.
- Write back the updated settings on to the EEPROM. In addition, an image file can be created for external use.

The Blaster Plus tool, user guide, and the Cypress-provided firmware are available at www.cypress.com/hx3.

### *HX3 as I²C Slave*

An external I²C master can program the configuration settings into HX3 according to the EEPROM map in Table 7 on page 26. Alternatively, the HX3 firmware (<10 KB), which includes configuration settings, can also be programmed. It is recommended to use the Blaster Plus tool to create the HX3 firmware or configuration image file. HX3's I²C slave address needs to be provided while creating the image file. Refer to Table 6 for HX3's I²C slave address.

**Table 7. EEPROM Map**

| I²C Offset | Bits | Name | Default | Description |
|---|---|---|---|---|
| 0 | 7:0 | bSignature LSB ("C") | 0x43 | The first byte of the 2-byte signature initialized with "CY" ASCII text.<br>When the signature is not valid, the hub enumerates as a vendor-specific device. |
| 1 | 7:0 | bSignature MSB ("Y") | 0x59 | The second byte of the 2-byte signature initialized with "CY" ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device. |
| 2 | 7:6 | bImageCTL | b'00 | Reserved |
| | 5:4 | I²C Speed | b'11 | b'01: 400 kHz<br>b'11: 100 kHz |
| | 3:1 | bImageCTL | b'000 | Reserved |
| | 0 | bImageCTL | 0 | 0: Execution binary file<br>1: Data file |
| 3 | 7:0 | bImageType | 0xD4 | 0xD4: Load only configuration<br>0xB0: Load firmware boot image<br>All other bImageType will return an error code. |
| 4 | 7:0 | bD4Length | 40 | bD4Length is defined in bytes as the length from offset 5.<br>I²C offset bytes 0–4 are the header bytes.<br>bD4Length = 6: Only update VID, PID, and DID<br>bD4Length = 18: Configuration options (no PHY trim)<br>bD4Length = 40: Configuration options with PHY trim options<br>bD4Length > 40: User must provide valid string descriptors<br>bD4Length > 192: Error |
| 5 | 7:0 | VID [7:0] | 0xB4 | Custom Vendor ID - LSB |
| 6 | 7:0 | VID [15:8] | 0x04 | Custom Vendor ID - MSB |
| 7 | 7:0 | PID [7:0] | 0x04 | Custom Product ID (PID)<br>Default: 0x6504<br>If separate PID is used for USB 2.0, the USB 2.0 PID will be read from offset 35 and 36.<br>Else, USB 2.0 PID = PID+2; Default: 0x6506 |
| 8 | 7:0 | PID [15:8] | 0x65 | |

**Table 7. EEPROM Map** *(continued)*

| I²C Offset | Bits | Name | Default | Description |
|---|---|---|---|---|
| 16 | 7 | SUSPEND_INDICATOR_DISABLE | 0 | 0: Suspend indicator enabled<br>1: Suspend indicator disabled |
| | 6 | SS_US_DISABLE | 0 | Hub mode of operation (USB 3.0 or USB 2.0)<br>0: USB 3.0 hub and USB 2.0 hub enabled<br>1: USB 3.0 hub disabled and USB 2.0 hub enabled |
| | 5 | PWR_EN_POLARITY | 0 | Power switch control output polarity<br>0: Active LOW<br>1: Active HIGH |
| | 4:0 | PORT_POLARITY | b'00000 | USB 2.0 DP and DM swapped<br>bit[4:0]=DS4, DS3, DS2, DS1, US<br>1: Port polarity swapped<br>0: Port polarity not swapped |
| 17 | 7:5 | Reserved | 0 | Reserved |
| | 4 | BC_ENABLE | 1 | 0: BC v1.2 disabled<br>1: BC v1.2 enabled |
| | 3 | ACA_DOCK | 0 | If this bit is set, enable ACA-Dock on the US port |
| | 2 | APPLE_XA | 0 | 0: Max limit for Apple charging 2.1 A<br>1: Max limit for Apple charging 1 A |
| | 1 | Reserved | 0 | Reserved |
| | 0 | GHOST_CHARGE_EN | 1 | 0: Ghost Charging disabled<br>1: Ghost Charging enabled |
| 18 | 7:4 | CDP_EN[3:0] | b'1111 | Per-port charging setting<br>bit[7:4]=DS4, DS3, DS2, DS1<br>0: CDP disabled<br>1: CDP enabled |
| | 3:0 | DCP_EN[3:0] | b'0000 | Per-port charging setting<br>bit[3:0]=DS4, DS3, DS2, DS1<br>0: DCP disabled<br>1: DCP enabled |
| 19 | 7 | EMBEDDED_HUB | 0 | If this bit is set, the US is as an embedded port and VBUS connected to VBUS_US pin is ignored. |
| | 6 | ILLEGAL_DESCRIPTOR | 1 | If this bit is set, the USB 2.0 hub controller will accept both 0x00 and 0x29 as valid descriptor types. If '0', only 0x29 will be accepted as a valid descriptor type. |
| | 5 | Reserved | 1 | Reserved |
| | 4 | OC_POLARITY | 0 | Overcurrent input polarity<br>0: Active LOW<br>1: Active HIGH |
| | 3:0 | OC_TIMER | b'1000 | Time in milliseconds for which the overcurrent inputs will be filtered |
| 20 | 7:0 | Reserved | 0 | Reserved |
| 21 | 7:4 | Reserved | 0 | Reserved |
| | 3 | STRING_DESCRIPTOR_ENABLE[16] | 0 | 0: String descriptor support is disabled<br>1: String descriptor support is enabled<br>When string descriptors are not supported, the hub controller returns a non-zero index (compile-time programmable) for each string which is supported, and 0x00 for each string not supported, as indicated by this field. |
| | 2:0 | Reserved | 0 | Reserved |
| 22 | 7:0 | Reserved | 0 | Reserved |

**Note**
16. When the string descriptor supports LangID, Manufacturer, Product and Serial Number, the serial number must be unique for each device.

## Power Consumption

Table 9 provides the power consumption estimates for HX3 under different conditions. Table 10 summarizes the power consumption for various combinations of devices connected to DS ports.

For example, to calculate the HX3 power consumption for three SS devices connected to DS ports (and no device connected to one DS port), and a US port connected to a USB 3.0 host:

Power consumption = [a] + 2*[g] = 492.5 + 2*76 = 644 mW

[a] is the active power consumption for the US port connected to a USB 3.0 host and the SS device connected to the DS port.

[g] is the incremental power consumption for an additional SS device connected to the DS port.

**Table 9. Power Consumption Estimates for Various Usage Scenarios**

| Device Condition | Number and Speed of DS Ports Connected | Typical Consumption | | | Comments |
|---|---|---|---|---|---|
| | | Supply Current (mA) | | Power (mW) | |
| | | 1.2 V | 3.3 V | | |
| Suspend [18] | NA | 12.0 | 7.1 | 37.8 | – |
| Active power with USB 3.0 host [19] | 1 SS | 204.1 | 75.0 | 492.5 | [a] |
| | 1 HS | 51.2 | 45.2 | 210.7 | [b] |
| | 1 FS | 51.2 | 34.0 | 173.7 | [c] |
| | 1 SS + 1 HS | 218.0 | 103.4 | 602.9 | [d] |
| Active power with USB 2.0 host [19, 20] | 1 HS | 51.2 | 45.2 | 210.7 | [e] |
| | 1 FS | 51.2 | 34.0 | 173.7 | [f] |
| Incremental active power for additional DS port | SS | 39.4 | 8.7 | 76.0 | [g] |
| | HS | 7.0 | 19.8 | 73.7 | [h] |
| | FS | 7.0 | 14.2 | 55.2 | [i] |
| Active power saving per disabled DS port[21] | – | 10.6 | 9.6 | 44.4 | [j] |

**Table 10. Power Consumption Under Various Configurations**

| Configuration | Number of DS Devices Connected With Data Transfer | Typical Consumption | | | Comments |
|---|---|---|---|---|---|
| | | Supply Current (mA) | | Power (mW) | |
| | | 1.2 V | 3.3 V | | |
| USB 3.0 4-Port Hub (USB 3.0 host) | 4 SS devices | 322 | 101 | 720 | [a] + 3*[g] |
| | 3 SS + 1 HS devices | 297 | 121 | 755 | [d] + 2*[g] |
| | 3 SS devices | 283 | 92 | 644 | [a] + 2*[g] |
| USB 3.0 4-Port Hub with one port disabled (USB 3.0 host) | 3 SS devices | 272 | 83 | 600 | [a] + 2*[g] - [j] |
| | 2 SS + 1 HS devices | 247 | 103 | 634 | [d] + [g] - [j] |
| Shared Link with eight DS ports | 4 SS + 4 HS devices | 357 | 189 | 1052 | [d] + 3*([g] + [h]) |
| USB 2.0 4-Port Hub (USB 2.0 host) | 4 HS devices | 72 | 105 | 432 | [e] + 3*[h] |
| | 3 HS + 1 FS devices | 72 | 99 | 413 | [e] + 2*[h] + [i] |

**Notes**
18. US port in low-power state (SS in U3 and USB 2.0 in L2).
19. All four DS ports are enabled.
20. US SS disabled using configuration options. Refer to Table 7 on page 26 for $I^2C$ configuration options.
21. Power saving applicable only with a USB 3.0 host. DS ports can be disabled through configuration options. Refer to Table 6 on page 25 for pin-strapping and Table 7 on page 26 for $I^2C$ configuration options.

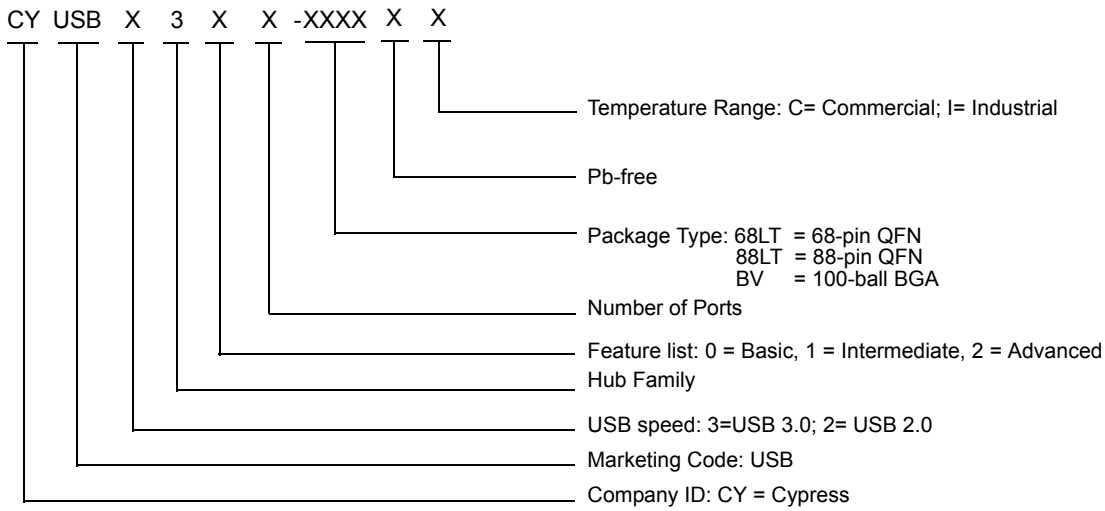
## Ordering Information

Table 11 lists HX3's ordering information. The table contains only the part numbers that are currently available for order. Additional part numbers for industrial temperature range can be made available on request. For more information, visit the Cypress website or contact the local sales representative.

**Table 11. Ordering Information**

| Serial No. | Ordering Part Number | Number of DS Ports | Number of Shared Link Ports | Ghost Charge | ACA-Dock | Temperature | Package |
|---|---|---|---|---|---|---|---|
| 1. | CYUSB3302-68LTXC | 2 (USB 3.0) | 0 | Yes | No | 0-70 °C | 68-QFN |
| 2. | CYUSB3302-68LTXI | 2 (USB 3.0) | 0 | Yes | No | –40-85 °C | 68-QFN |
| 3. | CYUSB3304-68LTXC | 4 (USB 3.0) | 0 | Yes | No | 0-70 °C | 68-QFN |
| 4. | CYUSB3304-68LTXI | 4 (USB 3.0) | 0 | Yes | No | –40-85 °C | 68-QFN |
| 5. | CYUSB3312-88LTXC | 2 (USB 3.0) | 0 | Yes | No | 0-70 °C | 88-QFN |
| 6. | CYUSB3312-88LTXI | 2 (USB 3.0) | 0 | Yes | No | –40-85 °C | 88-QFN |
| 7. | CYUSB3314-88LTXC | 4 (USB 3.0) | 0 | Yes | No | 0-70 °C | 88-QFN |
| 8. | CYUSB3314-88LTXI | 4 (USB 3.0) | 0 | Yes | No | –40-85 °C | 88-QFN |
| 9. | CYUSB3324-88LTXC | 4 (USB 3.0) | 0 | Yes | Yes | 0-70 °C | 88-QFN |
| 10. | CYUSB3324-88LTXI | 4 (USB 3.0) | 0 | Yes | Yes | –40-85 °C | 88-QFN |
| 11. | CYUSB3326-88LTXC | 6 (2 USB 3.0, 2 SS, 2 USB 2.0) | 2 | Yes | No | 0-70 °C | 88-QFN |
| 12. | CYUSB3326-88LTXI | 6 (2 USB 3.0, 2 SS, 2 USB 2.0) | 2 | Yes | No | –40-85 °C | 88-QFN |
| 13. | CYUSB3328-88LTXC | 8 (4 SS, 4 USB 2.0) | 4 | Yes | Yes | 0-70 °C | 88-QFN |
| 14. | CYUSB3328-88LTXI | 8 (4 SS, 4 USB 2.0) | 4 | Yes | Yes | –40-85 °C | 88-QFN |
| 15. | CYUSB3302-BVXC | 2 (USB 3.0) | 0 | Yes | No | 0-70 °C | 100-BGA |
| 16. | CYUSB3302-BVXI | 2 (USB 3.0) | 0 | Yes | No | –40-85 °C | 100-BGA |
| 17. | CYUSB3304-BVXC | 4 (USB 3.0) | 0 | Yes | No | 0-70 °C | 100-BGA |
| 18. | CYUSB3304-BVXI | 4 (USB 3.0) | 0 | Yes | No | –40-85 °C | 100-BGA |
| 19. | CYUSB3312-BVXC | 2 (USB 3.0) | 0 | Yes | No | 0-70 °C | 100-BGA |
| 20. | CYUSB3312-BVXI | 2 (USB 3.0) | 0 | Yes | No | –40-85 °C | 100-BGA |
| 21. | CYUSB3314-BVXC | 4 (USB 3.0) | 0 | Yes | No | 0-70 °C | 100-BGA |
| 22. | CYUSB3314-BVXI | 4 (USB 3.0) | 0 | Yes | No | –40-85 °C | 100-BGA |
| 23. | CYUSB3324-BVXC | 4 (USB 3.0) | 0 | Yes | Yes | 0-70 °C | 100-BGA |
| 24. | CYUSB3324-BVXI | 4 (USB 3.0) | 0 | Yes | Yes | –40-85 °C | 100-BGA |
| 25. | CYUSB3326-BVXC | 6 (2 USB 3.0, 2 SS, 2 USB 2.0) | 2 | Yes | No | 0-70 °C | 100-BGA |
| 26. | CYUSB3326-BVXI | 6 (2 USB 3.0, 2 SS, 2 USB 2.0) | 2 | Yes | No | –40-85 °C | 100-BGA |
| 27. | CYUSB3328-BVXC | 8 (4 SS, 4 USB 2.0) | 4 | Yes | Yes | 0-70 °C | 100-BGA |
| 28. | CYUSB2302-68LTXI | 2 (USB 2.0) | 0 | Yes | No | –40-85 °C | 68-QFN |
| 29. | CYUSB2304-68LTXI | 4 (USB 2.0) | 0 | Yes | No | –40-85 °C | 68-QFN |

## Ordering Code Definitions



## Packaging

**Table 12. Package Characteristics**

| Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_A$ | Operating ambient temperature | –40 | – | 85 | °C |
| $T_J$ | Operating junction temperature | –40 | – | 125 | °C |
| $T_{JA}$ | Package $J_A$ (68-pin QFN) | – | 16.2 | – | °C/W |
| $T_{JA}$ | Package $J_A$ (88-pin QFN) | – | 15.7 | – | °C/W |
| $T_{JA}$ | Package $J_A$ (100-ball BGA) | – | 35 | – | °C/W |
| $T_{JC}$ | Package $J_C$ (68-pin QFN) | – | 23.8 | – | °C/W |
| $T_{JC}$ | Package $J_C$ (88-pin QFN) | – | 18.9 | – | °C/W |
| $T_{JC}$ | Package $J_C$ (100-ball BGA) | – | 12 | – | °C/W |

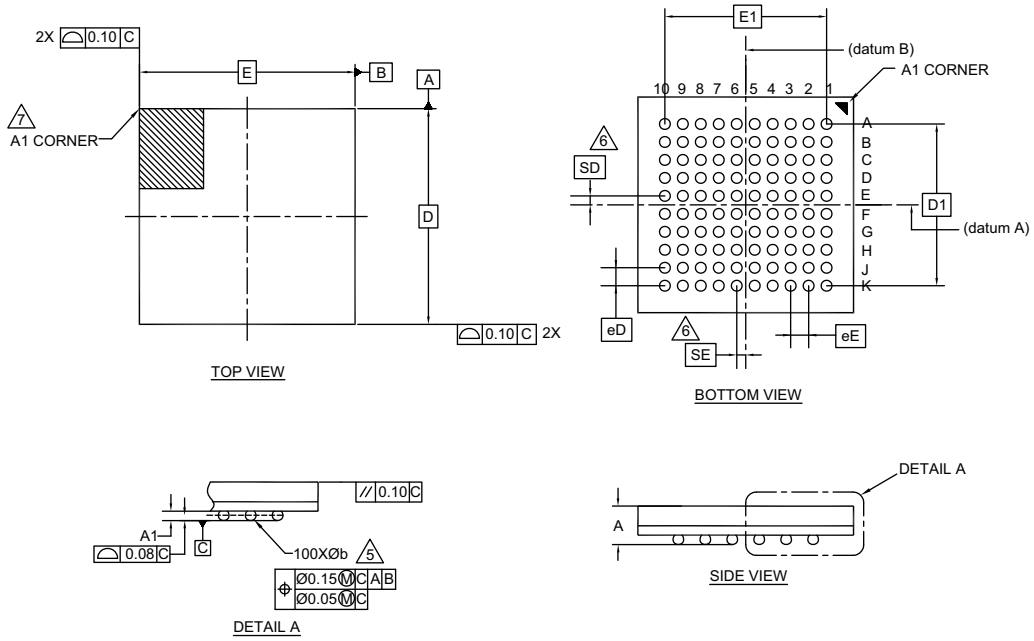
**Table 13. Solder Reflow Peak Temperature**

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---|---|---|
| 68-pin QFN | 260 °C | 30 seconds |
| 88-pin QFN | 260 °C | 30 seconds |
| 100-ball BGA | 260 °C | 30 seconds |

**Table 14. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Package | MSL |
|---|---|
| 68-pin QFN | MSL 3 |
| 88-pin QFN | MSL 3 |
| 100-ball BGA | MSL 3 |

**Figure 20. 100-Ball BGA (6.0 × 6.0 × 1.0 mm) BZ100 Package Outline**




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.00 |
| A1 | 0.16 | - | - |
| D | 6.00 BSC | | |
| E | 6.00 BSC | | |
| D1 | 4.50 BSC | | |
| E1 | 4.50 BSC | | |
| MD | 10 | | |
| ME | 10 | | |
| N | 100 | | |
| ∅ b | 0.25 | 0.30 | 0.35 |
| eD | 0.50 BSC | | |
| eE | 0.50 BSC | | |
| SD | 0.25 BSC | | |
| SE | 0.25 BSC | | |

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-195C.

51-85209 *F

## Acronyms

**Table 15. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| ACA | Accessory Charging Adapter |
| ASSP | Application-Specific Standard Product |
| BC | Battery Charging |
| CDP | Charging Downstream Port |
| DS | DownStream |
| DCP | Dedicated Charging Port |
| DNU | Do Not Use |
| DWG | Device Working Group |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| FS | Full-Speed |
| FW | FirmWare |
| GND | GrouND |
| GPIO | General-Purpose Input/Output |
| HS | Hi-Speed |
| ISP | In-System Programming |
| I/O | Input/Output |
| LS | Low-Speed |
| NC | No Connect |
| OTG | On-The-Go |
| PID | Product ID |
| POR | Power-On Reset |
| ROM | Read-Only Memory |
| SCL | Serial CLock |
| SDA | Serial DAta |
| SS | SuperSpeed |
| TT | Transaction Translator |
| US | UpStream |
| VID | Vendor ID |

## Reference Documents

*USB 2.0 Specification*

*USB 3.0 Specification*

*Battery Charging Specification*

## Document Conventions

### Units of Measure

**Table 16. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degree celsius |
| Ω | ohm |
| Gbps | gigabit per second |
| KB | kilobyte |
| kHz | kilohertz |
| kΩ | kiloohm |
| Mbps | megabit per second |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| ms | millisecond |
| mW | milliwatt |
| ns | nanosecond |
| ppm | parts per million |
| V | volt |