

Welcome to **E-XFL.COM**

<u>Embedded - Microcontrollers - Application</u>
<u>Specific</u>: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are <u>Embedded - Microcontrollers - Application Specific</u>?

Application charific microcontrollars are angineered to

Details	
Product Status	Active
Applications	USB 3.0 Hub Controller
Core Processor	ARM® Cortex®-M0
Program Memory Type	ROM (32kB)
Controller Series	CYUSB
RAM Size	16K x 8
Interface	I ² C
Number of I/O	10
Voltage - Supply	1.14V ~ 1.26V, 2.5V ~ 2.7V, 3V ~ 3.6V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3312-bvxi

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

CYUSB330x/CYUSB331x CYUSB332x/CYUSB230x



Contents

Architecture Overview	4
SS Hub Controller	4
USB 2.0 Hub Controller	
CPU	
I2C Interface	
Port Controller	4
Applications	
HX3 Product Options	
Product Features	
Shared Link	6
Ghost Charge	6
Vendor-Command Support	
ACA-Dock Support	
Pin Information	
System Interfaces	24
Upstream Port (US)	
Downstream Ports (DS1, 2, 3, 4)	
Communication Interfaces (I2C)	24
Oscillator	24
GPIOs	24
Power Control	24
Reset	24
Configuration Mode Select	24
Configuration Options	

EMI	31
ESD	31
Absolute Maximum Ratings	32
Electrical Specifications	32
DC Electrical Characteristics	32
Power Consumption	
Ordering Information	34
Ordering Code Definitions	35
Packaging	36
Package Diagrams	37
Acronyms	39
Reference Documents	39
Document Conventions	
Units of Measure	39
Silicon Revision History	
Method of Identification	40
Document History Page	41
Sales, Solutions, and Legal Information	42
Worldwide Sales and Design Support	42
Products	42
PSoC®Solutions	42
Cypress Developer Community	42
Technical Support	42



HX3 Product Options

Table 1. HX3 Product Options

Features	CYUSB3302	CYUSB3304	CYUSB3312	CYUSB3314	CYUSB3324	CYUSB3326	CYUSB3328	CYUSB2302- 68LTXI	CYUSB2304- 68LTXI
Number of DS ports	2 (USB 3.0)	4 (USB 3.0)	2 (USB 3.0)	4 (USB 3.0)	4 (USB 3.0)	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	8 (4 SS, 4 USB 2.0)	2 (USB 2.0)	4 (USB 2.0)
Number of Shared Link ports	0	0	0	0	0	2 ^[1]	4	0	0
BC v1.2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACA-Dock	No	No	No	No	Yes	No	Yes	No	No
External Power Switch Control	Ganged	Ganged	Individual and Ganged	Individual and Ganged	Individual and Ganged	Individual	Individual	Ganged	Ganged
Pin-Strap support	No	No	Yes	Yes	Yes	Yes	Yes	No	No
I ² C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Vendor command	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Port indicators	No	No	Yes	Yes	Yes	No	No	No	No
Packages ^[2]	68-QFN, 100-ball BGA	68-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	68-QFN, 100-ball BGA	68-QFN, 100-ball BGA
Temperature range	Industrial and Commercial	Industrial (88-QFN only) and Commercial	Industrial and Commercial	Industrial and Commercial					

DS1 and DS2 are Shared link Ports.
 BGA Industrial Grade packages are limited to 1 W of active power. For power calculations refer to Table 10 on page 33.



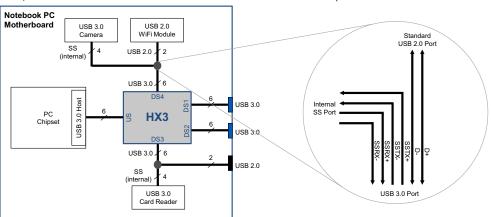
Product Features

Shared Link

Figure 1. Application of Shared Link in a Notebook

Example: Shared Link Provides Six USB Ports in a Notebook

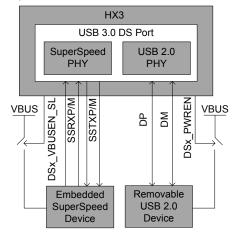
USB 3.0 Port Split Into SS Port and Standard USB 2.0 Port



Shared Link is a Cypress-proprietary feature that enables a USB 3.0 port to be split into an embedded SS port and a standard USB 2.0 port. Shared Link enables a maximum of eight DS ports from a four-port USB 3.0 hub.

For example, if one of the DS ports is connected to an embedded SS device, such as a USB 3.0 camera, HX3 enables the system designer to reuse the USB 2.0 signals of that specific port to connect to a standard USB 2.0 port. Figure 1 shows how Shared Link can be used in an application.

Figure 2. DS Port VBUS Control in Shared Link



The Shared Link mode requires a separate VBUS control for the removable USB 2.0 device and the embedded SS device. Figure 2 shows the VBUS control implementation.

To ensure that the embedded SS device does not fall back to USB 2.0 operation, an external power switch is required. This switch is controlled by HX3, which generates an output signal called DSx_VBUSEN_SL. This signal controls the VBUS for the embedded device.

DSx_PWREN is another output signal generated by HX3 and controls VBUS for the removable USB 2.0 device. For example, when an overcurrent condition occurs, DSx_PWREN turns off the port power.

Ghost Charge

Ghost Charge is a Cypress-proprietary feature for charging USB devices on the DS port when the US port is not connected to a host. For example, in a docking station with HX3 as shown in Figure 3, when the laptop is undocked, HX3 will emulate a dedicated charging port (DCP) to provide charge to a phone connected on a DS port.

Figure 3. Ghost Charge

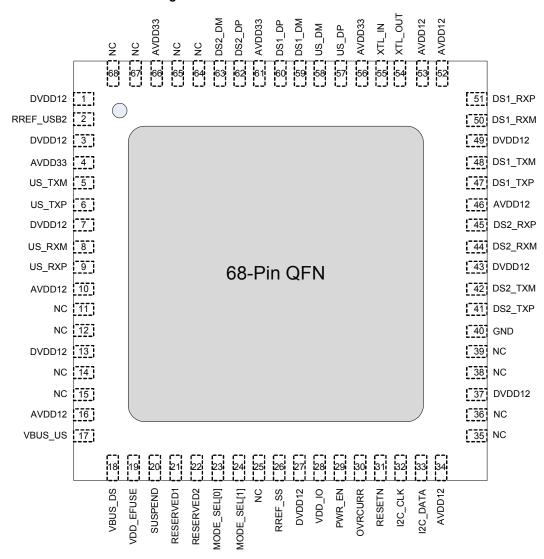


Charge a smartphone without docking the notebook



Pin Information

Figure 6. HX3 68-Pin QFN 2-Port Pinout





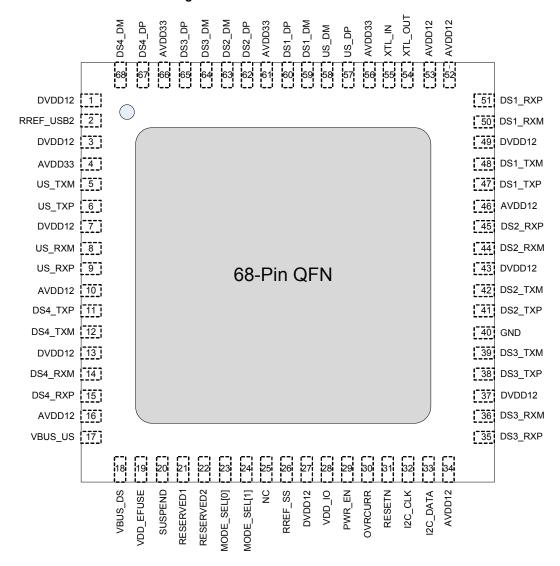


Figure 7. HX3 68-Pin QFN 4-Port Pinout



Table 2. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB3302 and CYUSB3304 (continued)

Pin Name			400 000	
CYUSB3302 CYUSB3304	Туре	68-QFN Pin#	100-BGA Ball #	Description
RESERVED1	I/O	21	G4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
RESERVED2	ı	22	H4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
		Mo	de Select, Clo	ck, and Reset
MODE_SEL[0]	I	23	G5	Device operation mode select bit 0; refer to Table 5 on page 24
MODE_SEL[1]	I	24	F4	Device operation mode select bit 1; refer to Table 5 on page 24
XTL_OUT	Α	54	E6	Crystal out
XTL_IN	Α	55	E5	Crystal in
RESETN	I	31	F7	Active LOW reset input
I2C_CLK	I/O	32	J6	I ² C clock
I2C_DATA	I/O	33	G8	I ² C data
SUSPEND	I/O	20	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
			Power and	Ground
VDD_EFUSE	PWR	19	НЗ	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V.
AVDD12	PWR	10, 16, 34, 46, 52, 53	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND	PWR	40	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12	PWR	1, 3, 7, 13, 27, 37, 43, 49,	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS_US	PWR	17	H2	This pin must be connected to VBUS from US port
VBUS_DS	PWR	18	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33	PWR	4, 56, 61, 66	A4, A7, B6, F3	3.3 V analog supply
VDD_IO	PWR	28	B4, E7, G6	3.3 V I/O supply
			USB Precision	Resistors
RREF_USB2	Α	2	E2	Connect pin to a precision resistor (6.04 k Ω ±1%) to generate a current reference for USB 2.0 PHY.
RREF_SS	Α	26	H5	Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration.
RREF_USB2	A	2	USB Precision E2	Resistors Connect pin to a precision resistor (6.04 k Ω ±1%) to generate a current reference for USB 2.0 PHY. Connect pin to a precision resistor (200 Ω ±1%) for SS PHY

Note

^{4.} These pins are Do Not Use (DNU); they must be left floating.



Table 3. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB2302 and CYUSB2304 (continued)

				· ,
Pin Name CYUSB2302 CYUSB2304	Type	68-QFN Pin#	100-BGA Ball #	Description
RESERVED1	I/O	21	G4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
RESERVED2	I	22	H4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
		Mo	ode Select, Clo	ck, and Reset
MODE_SEL[0]	I	23	G5	Device operation mode select bit 0; refer to Table 5 on page 24
MODE_SEL[1]	I	24	F4	Device operation mode select bit 1; refer to Table 5 on page 24
XTL_OUT	Α	54	E6	Crystal out
XTL_IN	Α	55	E5	Crystal in
RESETN	I	31	F7	Active LOW reset input
I2C_CLK	I/O	32	J6	I ² C clock
I2C_DATA	I/O	33	G8	I ² C data
SUSPEND	I/O	20	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
			Power and	Ground
VDD_EFUSE	PWR	19	НЗ	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V.
AVDD12	PWR	10, 16, 34, 46, 52, 53	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND	PWR	40	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12	PWR	1, 3, 7, 13, 27, 37, 43, 49,	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS_US	PWR	17	H2	This pin must be connected to VBUS from US port
VBUS_DS	PWR	18	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33	PWR	4, 56, 61, 66	A4, A7, B6, F3	3.3 V analog supply
VDD_IO	PWR	28	B4, E7, G6	3.3 V I/O supply
			USB Precision	Resistors
RREF_USB2	Α	2	E2	Connect pin to a precision resistor (6.04 k Ω ±1%) to generate a current reference for USB 2.0 PHY.
RREF_SS	Α	26	H5	Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration.



DS3_PWREN DS2_PWREN DS3_AMBER DS2_LED_ DS2_DM XTL_OUT AVDD33 AVDD12 DS1_DM Ol_ddv 88 DVDD12 DS4 DM DS3_DM DS4 DP DS3_DP DS2_DP **AVDD33** US_DM **AVDD33** US_DP XTL_IN 87 83 80 79 69 81 72 DS2_OVRCURR [1] 66 VDD_IO 65 2 DS3_OVRCURR DS1_AMBER DS1_GREEN 3 64 DS3_GREEN DS1_LED_SS 4 63 DS3_LED_SS DS2_AMBER 5 62 AVDD12 DS2_GREEN 6 61 DS1_RXP 7 RREF_USB2 60 DS1_RXM 8 59 DVDD12 DVDD12 58 AVDD33 9 DS1_TXM 10 57 DS1_TXP US_TXM US TXP 111 56 AVDD12 88-Pin QFN DVDD12 12 55 DS2_RXP US_RXM 13 54 DS2_RXM 53 DVDD12 US_RXP 14 AVDD12 15 52 DS2_TXM 51 DS2_TXP DS4_TXP 16 50 DS4_TXM 17 GND DVDD12 18 49 DS3_TXM DS4_RXM 19 48 DS3_TXP DS4_RXP 47 DVDD12 20 AVDD12 21 46 DS3_RXM VBUS_US 22 45 DS3_RXP 30 25 26 27 28 29 31 DVDD12 VDD_IO RESETN 12C_CLK VBUS_DS VDD_EFUSE RREF_SS SUSPEND DS4_LED_SS RESERVED1 MODE_SEL[0] MODE_SEL[1] DS4_AMBER US_PWREN DS4 PWREN/PWR EN4 JS4_OVRCURR DS1_PWREN US_OVRCURR I2C_DATA DS1_OVRCURR DS4_GREEN AVDD12

Figure 11. HX3 88-Pin QFN 4-Port Pinout

Document Number: 001-73643 Rev. *P



Figure 13. HX3 100-Ball BGA Pinout for CYUSB3314, CYUSB332x

A1	A2	А3	A4	A 5	A6	A 7	A8	А9	A10
DS3_PWR EN	DS4_DM	DS4_DP	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
DS2_OVR CURR	DS2_PWR EN	DS3_AMB ER	VDD_IO	VSS	AVDD33	DS3_OVR CURR	DS3_GRE EN	DS3_LED _SS	DVDD12
C1	C2	C3	C4	C5	C6	C 7	C8	C9	C10
US_TXM	DS1_AMB ER	DS2_LED _SS	DS3_DP	DS3_DM	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
US_TXP	DS1_LED _SS	DS1_GRE EN	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
DVDD12	RREF_US B2	DS2_GRE EN	DS2_AMB ER	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
US_RXM	VSS	AVDD33	MODE_SE L[1]	DVDD12	DS4_OVR CURR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
US_RXP	VBUS_DS	SUSPEND	RESERVE D1	MODE_SE L[0]	VDD_IO	DS4_PWR EN	I2C_DATA	VSS	DS2_RXM
H1	H2	Н3	H4	H5	Н6	H7	H8	Н9	H10
AVDD12	VBUS_US	VDD_EFU SE	DS4_LED _SS	RREF_SS	VSS	DS2_TXM	DS2_TXP	DS4_GRE EN	AVDD12
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
VSS	AVDD12	VSS	DS4_AMB ER	US_PWR EN	I2C_CLK	DS1_PWR EN	DS1_OVR CURR	VSS	DS3_RXM
K1	K2	K3	K4	K5	K6	K 7	K8	K9	K10
DS4_TXP	DS4_TXM	DVDD12	DS4_RXP	DS4_RXM	US_OVRC URR	DS3_TXP	DS3_TXM	DVDD12	DS3_RXP



Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X (continued)

CYUSB3314 CYUSB3324 CYUSB3328 CYUSB33328 CYUSB3328 CY	Pin	Name				
DS3_VBUSEN_SLI* 9		CYUSB3324 CYUSB3326 CYUSB3328	Туре	Pin#	Ball#	Description
NC DS4_RXM 1 19 19 19 19 19 19 19	_					CYUSB3312/3314/3324: LED_GREEN output for DS3 port
DS3_LED_SS 9	DS3_VBU	USEN_SL ^[9]	I/O	64	B8	· · · · · ·
PIN_STRAP ^[10] I/O 63 B9 This pin is called PIN_STRAP in pin-strap configuration mode. When connected to VDD_IO through a 10-kΩ resistor, this pin enables pin-strap configuration mode for HX3. DS4_RXP	_					
Connected to VDD_IO through a 10-kΩ resistor, this pin enables pin-strap configuration mode for HX3. NC	DS3_L	.ED_SS ^[9]				
NC	PIN_S	TRAP ^[10]	I/O	63	В9	connected to VDD IO through a 10-k Ω resistor, this pin enables
NC						DS4 Port
NC		_	I	20	K4	
NC	NC	DS4_RXM	ı	19	K5	SuperSpeed receive minus
NC		_			K1	SuperSpeed transmit plus
NC DS4_DM I/O 82 A2 USB 2.0 data minus		_		17	K2	
DS4_OVRCURR I 36 F6 CYUSB3314/3324/3326/3328: Overcurrent detect input for DS4 port. CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO. DS4_PWREN/PWR_EN4 I/O 35 G7 WSUS power enable output for DS4 port. This pin is also used as power enable output when configured in ganged power mode using the Blaster Plus tool. When the port is disabled, this pin is in tristate. DS4_CDP_ENI ^{TIOJ} I/O 30 J4 EED_AMBER output for DS4 port This pin is called DS4_CDP_EN in the pin-strap configuration mode. DS4_GREENI ^{IOJ} I/O 43 H9 CYUSB3312/3314/3324: LED_GREEN output for DS4 port DS4_VBUSEN_SL I/O 43 H9 CYUSB3312/3314/3324: LED_GREEN output for DS4 port This pin is called VID_SEL[0] in the pin-strap configuration mode. DS4_LED_SS I/O 26 H4 Shown in Figure 16 on page 25. If LED is not used, this pin must be pulled HIGH using a 10 kΩ to VDD_IO. RESERVED1 I 27 G4 This pin must be pulled HIGH using a 10 kΩ to VDD_IO. Mode Select, Clock, and Reset MODE_SEL[0] I 28 G5 Device operation mode select bit 0; refer to Table 5 on page 24 XTL_OUT A 68 E6 Crystal out XTL_IN A 69 E5 Crystal in RESETN I 37 F7 Active LOW reset input I2C_CLK I/O 40 J6 I ² C clock	NC	DS4_DP	I/O	81	A3	USB 2.0 data plus
DS4_DVRCORR I 36 F6 CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO. DS4_PWREN/PWR_EN4 I/O 35 G7 VBUS power enable output for DS4 port. This pin is also used as power enable output when configured in ganged power mode using the Blaster Plus tool. When the port is disabled, this pin is in tristate. This pin is called DS4_CDP_EN in the pin-strap configuration mode. DS4_AMBER ^[9] I/O 30 J4 LED_AMBER output for DS4 port This pin is called I2C_DEV_ID in the pin-strap configuration mode. DS4_GREEN ^[9] CYUSB3312/3314/3324: LED_GREEN output for DS4 port This pin is called VID_SEL[0] in the pin-strap configuration mode. DS4_USBSEL[0] ^[10] CYUSB3328: VBUS power enable output for SS port 4 This pin is called VID_SEL[0] in the pin-strap configuration mode. LED_SS output for DS4 port. The LED must be connected to GND as shown in Figure 16 on page 25. If LED is not used, this pin must be pulled HIGH using a 10 kΩ to VDD_IO. Mode Select, Clock, and Reset MODE_SEL[0] I 28 G5 Device operation mode select bit 0; refer to Table 5 on page 24 MODE_SEL[1] I 29 F4 Device operation mode select bit 1; refer to Table 5 on page 24 XTL_OUT A 68 E6 Crystal out XTL_IN A 69 E5 Crystal in RESETN I 37 F7 Active LOW reset input I2C_CLK I/O 40 J6 I ² C clock	NC	DS4_DM	I/O	82	A2	USB 2.0 data minus
DS4_PWREN/PWR_EN4	DS4_O	VRCURR	I	36	F6	
DS4_AMBER ^[9] I/O 30 J4 LED_AMBER output for DS4 port This pin is called I2C_DEV_ID in the pin-strap configuration mode. DS4_GREEN ^[9] DS4_VBUSEN_SL VIO_SEL[0] ^[10] VID_SEL[0] ^[10] I/O 43 H9 CYUSB3312/3314/3324: LED_GREEN output for DS4 port CYUSB3328: VBUS power enable output for SS port 4 This pin is called VID_SEL[0] in the pin-strap configuration mode. LED_SS output for DS4 port. The LED must be connected to GND as shown in Figure 16 on page 25. If LED is not used, this pin must be pulled HIGH using a 10 kΩ to VDD_IO. RESERVED1 I 27 G4 This pin must be pulled HIGH using a 10 kΩ to VDD_IO. Mode Select, Clock, and Reset MODE_SEL[0] I 28 G5 Device operation mode select bit 0; refer to Table 5 on page 24 MODE_SEL[1] I 29 F4 Device operation mode select bit 1; refer to Table 5 on page 24 XTL_OUT A 68 E6 Crystal out XTL_IN A 69 E5 Crystal in RESETN I 37 F7 Active LOW reset input I2C_CLK I/O 40 J6 I ² C clock	DS4_PWRE	EN/PWR_EN4	I/O	35	G7	enable output when configured in ganged power mode using the Blaster
I/O 30 J4 This pin is called I2C_DEV_ID in the pin-strap configuration mode.	DS4_CI	DP_EN ^[10]				This pin is called DS4_CDP_EN in the pin-strap configuration mode.
This pin is called I2C_DEV_ID in the pin-strap configuration mode. DS4_GREEN ^[9] DS4_VBUSEN_SL VID_SEL[0] ^[10] I/O 43 H9 CYUSB3312/3314/3324: LED_GREEN output for DS4 port CYUSB3328: VBUS power enable output for SS port 4 This pin is called VID_SEL[0] in the pin-strap configuration mode. LED_SS output for DS4 port. The LED must be connected to GND as shown in Figure 16 on page 25. If LED is not used, this pin must be pulled HIGH using a 10 kΩ to VDD_IO. RESERVED1 I 27 G4 This pin must be pulled HIGH using a 10 kΩ to VDD_IO. Mode Select, Clock, and Reset MODE_SEL[0] I 28 G5 Device operation mode select bit 0; refer to Table 5 on page 24 MODE_SEL[1] I 29 F4 Device operation mode select bit 1; refer to Table 5 on page 24 XTL_OUT A 68 E6 Crystal out XTL_IN A 69 E5 Crystal in RESETN I 37 F7 Active LOW reset input I2C_CLK I/O 40 J6 I ² C clock	DS4_A	AMBER ^[9]	1/0	30	J4	LED_AMBER output for DS4 port
DS4_VBUSEN_SL I/O 43 H9 CYUSB3328: VBUS power enable output for SS port 4 This pin is called VID_SEL[0] in the pin-strap configuration mode. LED_SS output for DS4 port. The LED must be connected to GND as shown in Figure 16 on page 25. If LED is not used, this pin must be pulled HIGH using a 10 kΩ to VDD_IO. RESERVED1 I 27 G4 This pin must be pulled HIGH using a 10 kΩ to VDD_IO. Mode Select, Clock, and Reset MODE_SEL[0] I 28 G5 Device operation mode select bit 0; refer to Table 5 on page 24 MODE_SEL[1] I 29 F4 Device operation mode select bit 1; refer to Table 5 on page 24 XTL_OUT A 68 E6 Crystal out XTL_IN A 69 E5 Crystal in RESETN I 37 F7 Active LOW reset input I2C_CLK I/O 40 J6 I ² C clock I ² C c	I2C_DI	EV_ID ^[10]	1/0			This pin is called I2C_DEV_ID in the pin-strap configuration mode.
VID_SEL[0][10] This pin is called VID_SEL[0] in the pin-strap configuration mode. LED_SS output for DS4 port. The LED must be connected to GND as shown in Figure 16 on page 25. If LED is not used, this pin must be pulled HIGH using a 10 kΩ to VDD_IO. RESERVED1 I 27 G4 This pin must be pulled HIGH using a 10 kΩ to VDD_IO. Mode Select, Clock, and Reset MODE_SEL[0] I 28 G5 Device operation mode select bit 0; refer to Table 5 on page 24 MODE_SEL[1] I 29 F4 Device operation mode select bit 1; refer to Table 5 on page 24 XTL_OUT A 68 E6 Crystal out XTL_IN A 69 E5 Crystal in RESETN I 37 F7 Active LOW reset input I2C_CLK I/O 40 J6 I²C clock	DS4_0	GREEN ^[9]				CYUSB3312/3314/3324: LED_GREEN output for DS4 port
DS4_LED_SS	DS4_VE	BUSEN_SL	I/O	43	H9	CYUSB3328: VBUS power enable output for SS port 4
DS4_LED_SS I/O 26	VID_S	SEL[0] ^[10]				This pin is called VID_SEL[0] in the pin-strap configuration mode.
MODE_SEL[0] I 28 G5 Device operation mode select bit 0; refer to Table 5 on page 24 MODE_SEL[1] I 29 F4 Device operation mode select bit 1; refer to Table 5 on page 24 XTL_OUT A 68 E6 Crystal out XTL_IN A 69 E5 Crystal in RESETN I 37 F7 Active LOW reset input I2C_CLK I/O 40 J6 I ² C clock	DS4_I	LED_SS	I/O	26	H4	shown in Figure 16 on page 25. If LED is not used, this pin must be pulled
MODE_SEL[0] I 28 G5 Device operation mode select bit 0; refer to Table 5 on page 24 MODE_SEL[1] I 29 F4 Device operation mode select bit 1; refer to Table 5 on page 24 XTL_OUT A 68 E6 Crystal out XTL_IN A 69 E5 Crystal in RESETN I 37 F7 Active LOW reset input I2C_CLK I/O 40 J6 I ² C clock	RESE	ERVED1	I	27	G4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
MODE_SEL[1] I 29 F4 Device operation mode select bit 1; refer to Table 5 on page 24 XTL_OUT A 68 E6 Crystal out XTL_IN A 69 E5 Crystal in RESETN I 37 F7 Active LOW reset input I2C_CLK I/O 40 J6 I ² C clock					Mode Se	elect, Clock, and Reset
XTL_OUT A 68 E6 Crystal out XTL_IN A 69 E5 Crystal in RESETN I 37 F7 Active LOW reset input I2C_CLK I/O 40 J6 I²C clock	MODE_SEL[0]		I	28	G5	Device operation mode select bit 0; refer to Table 5 on page 24
XTL_IN A 69 E5 Crystal in RESETN I 37 F7 Active LOW reset input I2C_CLK I/O 40 J6 I ² C clock	MODE	E_SEL[1]	I	29	F4	Device operation mode select bit 1; refer to Table 5 on page 24
RESETN I 37 F7 Active LOW reset input I2C_CLK I/O 40 J6 I ² C clock	XTL_OUT		Α	68	E6	Crystal out
RESETN I 37 F7 Active LOW reset input I2C_CLK I/O 40 J6 I ² C clock	XT	TL_IN	Α	69	E5	Crystal in
I2C_CLK I/O 40 J6 I ² C clock			ı	37	F7	<u> </u>
			I/O		J6	
			I/O	41	G8	I ² C data

This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
 For pin-strap configuration details, refer to Table 6 on page 25.



Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X (continued)

Dim A	lama.				
PIII N	Name				
	CYUSB3314				
CYUSB3312	CYUSB3324	Type	Pin#	Ball#	Description
C100b3312	CYUSB3326				
	CYUSB3328				
SUSF	PEND	I/O	25	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
				Po	wer and Ground
VDD_E	EFUSE	PWR	24	НЗ	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V
AVDD12		PWR	15, 21, 44, 56, 62, 67	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND		PWR	50	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVD	DD12	PWR	8, 12, 18, 33, 47, 53, 59, 83	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS	S_US	PWR	22	H2	CYUSB3324/3328: Connect the VBUS_US pin to the local 5 V supply. If ACA-Dock mode is disabled using Configuration Options on page 24, this pin must be connected to VBUS from US port. Other part numbers: This pin must be connected to VBUS from US port.
VBUS	S_DS	PWR	23	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	9, 70, 75, 80	A4, A7, B6, F3	3.3 V analog supply
VDD_IO F		PWR	34, 66, 88	B4, E7, G6	3.3 V I/O supply
				USB F	Precision Resistors
RREF_	USB2	Α	7	E2	Connect pin to a precision resistor (6.04 k Ω ±1%) to generate a current reference for USB 2.0 PHY.
RREI	F_SS	Α	32	H5	Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration.



Temperature range of 25 °C–70 °C and programming voltage of 2.5 V–2.7 V.

Pin-Strap Configuration

Pin-straps are supported for select product options (see Table 1 on page 5) to provide reconfigurability without an additional EEPROM. The pin-strap configuration is enabled by pulling the Pin #63 of 88-pin QFN HIGH. Table 6 on page 25 shows the configuration options supported through pin-straps and the GPIOs used for this purpose. Figure 16 and Figure 17 show how the GPIOs need to be connected if pin-strap and LED connection are required or only pin-strap is required.

HX3 samples pin-strap GPIOs at power-up. Floating straps are considered as invalid and the default configuration is used. If PIN_STRAP (Pin #63 of 88-pin QFN) is floating, all strap inputs are considered invalid. A GPIO is considered strapped "1" or "0" when connected with a weak pull-up (10 k Ω) or pull-down (10 k Ω) respectively. After the initial sampling at power-up and reset, the GPIOs are used in their normal functions.

Figure 16. Pin-Strap With LED or LED-Only Connection

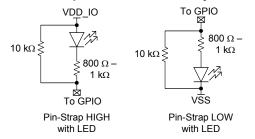


Figure 17. Pin-Strap Connection

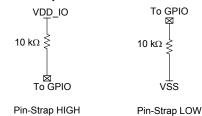


Table 6. Pin-Strap Configuration

88-QFN Pin #	Pin-Strap Name	Strappo	ed '0' ^[11]	Strapp	ed '1' ^[11]		
30	I2C_DEV_ID ^[12]	ID 0: HX3 I ² C slave at This is also the defaulthe 68-pin QFN packa	ddress (7 bits) is 0x60. t I ² C slave address for ge.	ID 1: HX3 I ² C slave address (7 bits) is 0x58			
31	PWR_SW_POL	Power enable and ove LOW	ercurrent will be active	Power enable and ove HIGH	ercurrent will be active		
2	ACA_DOCK	Disa	abled	Ena	abled		
84	PWR_EN_SEL	Indiv	vidual	Ga	ang		
63	PIN_STRAP ^[13]	No pin-s	strapping	Pin-strapping con	figuration enabled		
4	PORT_DISABLE[1]	PORT_DISABLE[1:0]					
3	PORT_DISABLE[0]	b'00: DS1, DS2, DS3, DS4 active b'01: DS1, DS2, DS3 active b'10: DS1, DS2 active b'11: DS1 active Pin-straps cannot enable ports disabled by factory setting.					
6	NON_REMOVABLE[1] ^[14]	NON_REMOVABLE[1	:0] =				
5	NON_REMOVABLE[0] ^[14]	b'00: DS1, DS2, DS3, b'01: DS1, DS2, DS3 b'10: DS1, DS2 remov b'11: DS1 removable	removable				
85	VID[2]						
64	VID[1]	Reserved. If PIN_STR	RAP is enabled and CY	VID is required, strap V	/ID[2:0] to '1'.		
43	VID[0]						
38	DS1 CDP EN ^[15]	strapped '0'	strapped '1'	strapped '0'	strapped '1'		
30	D21_CDP_EN.	DS1 CDP enabled	DS1 CDP disabled	DS1 CDP disabled	DS1 CDP enabled		
86	DS2_CDP_EN ^[15]	DS2 CDP enabled	DS2 CDP disabled	DS2 CDP disabled	DS2 CDP enabled		
87	DS3_CDP_EN ^[15]	DS3 CDP enabled	DS3 CDP disabled	DS3 CDP disabled	DS3 CDP enabled		
35	DS4_CDP_EN ^[15]	DS4 CDP enabled	DS4 CDP disabled	DS4 CDP disabled	DS4 CDP enabled		

- 11. See Figure 16 and Figure 17.
- 12. I2C_DEV_ID is valid only when HX3 is in I²C slave mode.
- 13. VID, PORT_DISABLE, NON_REMOVABLE are group straps. If one of the pins in a group strap is floating (INVALID), that group input will be INVALID and the default will not be overwritten.
- 14. These DS ports are exposed ports and the connected devices can be removed.
- 15. DSx_CDP_EN will be active LOW input when PWR_SW_POL is set to active LOW; similarly DSx_CDP_EN will be active HIGH input when PWR_SW_POL is set to active HIGH.



 Table 7. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
9		DID [7:0]	00 - 88-pin QFN, 10 - 68-pin QFN	Custom Device ID - revision - LSB
10		DID [15:8]	50	Custom Device ID - revision - MSB
11		Reserved	0	Reserved
12	7:4	SHARED_LINK_EN	b'0000	Enable Shared Link on DS port bit[7:4]=DS4, DS3, DS2, DS1 0: Shared Link not enabled 1: Shared Link enabled
	3:0	SHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a SuperSpeed port is active. bit[3:0] = DS4, DS3, DS2, DS1 0: Not active 1: Active
13	7:0	POWER_ON_TIME	0x32	Time (in 2-ms intervals) from the time the power-on sequence begins on a port until power is good on that port (bPwron2PwrGood)
14	7:4	REMOVABLE_PORTS [3:0]	b'1111	Indicates if the port is removable. bit[7:4]=DS4, DS3, DS2, DS1 0: Non-removable 1: Removable
	3:0	UHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a USB 2.0 port is active. bit[3:0]=DS4, DS3, DS2, DS1 0: Not active 1: Active
15	7	SS_LED_PIN_CONTROL	0	Port 1–4: SS LED disable 0: DS[1:4]_LED_SS are LEDs. The LED glows when the SS port is active and not in disabled state. 1: DS[1:4]_LED_SS are not LEDs
	6	GREEN_LED_PIN_CONTROL	0	Port 1–4: USB 2.0 Green LED disable 0: DS[1:4]_GREEN are LEDs 1: DS[1:4]_GREEN are not LEDs
	5	AMBER_LED_PIN_CONTROL	0	Port 1–4: USB 2.0 Amber LED disable 0: DS[1:4]_AMBER are LEDs 1: DS[1:4]_AMBER are not LEDs
	4	PORT_INDICATORS	1	Port indicators supported 0: Port indicators are not supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request has no effect. 1: Port indicators are supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request controls the indicators.
	3	COMPOUND_HUB	0	Identifies a compound device. 0: Hub is not part of a compound device. 1: Hub is part of a compound device.
	2:1	Reserved	0	Reserved
	0	GANG	0	Ganged power switch enable for all DS ports Individual port power switch enable for each DS port



Table 7. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
51 + X	7:0	bString: Product	'C', 0, 'Y', 0, '-', 0, 'H', 0, 'X', 0, '3', 0, ' ', 0, 'H', 0, 'U', 0, 'B', 0	Product string: UNICODE UTF-16LE per USB 2.0 specification: "CY-HX3 HUB"
49 + X + Y	7:0	bLength: Serial Number (Z)	22	Serial number string length ("bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number" should be less than or equal to 152 bytes). Z ≤ 66.
50 + X + Y	7:0	DescType	3	String descriptor type (constant value)
51 + X + Y	7:0	bString: Serial Number	'1', 0, '2', 0, '3', 0, '4', 0, '5', 0, '6', 0, '7', 0, '8', 0, '9', 0, 'A', 0	Serial number string: UNICODE UTF-16LE per USB 2.0 specification: "123456789A"

EMI ESD

HX3 meets the EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. HX3 tolerates EMI conducted by aggressors outlined by the above specifications and continues to function as expected.

HX3 has a built-in ESD protection on all pins. The ESD protection level provided on these ports is 2.2 kV Human Body Model (HBM) based on the JESD22-A114 specification.



Power Consumption

Table 9 provides the power consumption estimates for HX3 under different conditions. Table 10 summarizes the power consumption for various combinations of devices connected to DS ports.

For example, to calculate the HX3 power consumption for three SS devices connected to DS ports (and no device connected to one DS port), and a US port connected to a USB 3.0 host:

Power consumption = [a] + 2*[g] = 492.5 + 2*76 = 644 mW

[a] is the active power consumption for the US port connected to a USB 3.0 host and the SS device connected to the DS port.

[g] is the incremental power consumption for an additional SS device connected to the DS port.

Table 9. Power Consumption Estimates for Various Usage Scenarios

		Typical Consumption				
Device Condition	Number and Speed of DS Ports Connected	Supply Current (mA)		Dawer (malA)	Comments	
	2010100000	1.2 V 3.3 V		Power (mW)		
Suspend [18]	NA	12.0	7.1	37.8	_	
	1 SS	204.1	75.0	492.5	[a]	
Active power with USB 3.0 host [19]	1 HS	51.2	45.2	210.7	[b]	
Active power with USB 3.0 nost 199	1 FS	51.2	34.0	173.7	[c]	
	1 SS + 1 HS	218.0	103.4	602.9	[d]	
Active power with USB 2.0 host [19,	1 HS	51.2	45.2	210.7	[e]	
20]	1 FS	51.2	34.0	173.7	[f]	
	SS	39.4	8.7	76.0	[g]	
Incremental active power for additional DS port	HS	7.0	19.8	73.7	[h]	
	FS	7.0	14.2	55.2	[i]	
Active power saving per disabled DS port ^[21]	-	10.6	9.6	44.4	Ü	

Table 10. Power Consumption Under Various Configurations

	Number of DS Devices	Typical Consumption			
Configuration	Connected With Data Transfer	Supply Current (mA)		Dower (m)A/)	Comments
		1.2 V	3.3 V	Power (mW)	
USB 3.0	4 SS devices	322	101	720	[a] + 3*[g]
4-Port Hub (USB 3.0 host)	3 SS + 1 HS devices	297	121	755	[d] + 2*[g]
	3 SS devices	283	92	644	[a] + 2*[g]
USB 3.0	3 SS devices	272	83	600	[a] + 2*[g] - [j]
4-Port Hub with one port disabled (USB 3.0 host)	2 SS + 1 HS devices	247	103	634	[d] + [g] - [j]
Shared Link with eight DS ports	4 SS + 4 HS devices	357	189	1052	[d] + 3*([g] + [h])
USB 2.0	4 HS devices	72	105	432	[e] + 3*[h]
4-Port Hub (USB 2.0 host)	3 HS + 1 FS devices	72	99	413	[e] + 2*[h] + [i]

^{18.} US port in low-power state (SS in U3 and USB 2.0 in L2).

^{19.} All four DS ports are enabled.

^{20.} US SS disabled using configuration options. Refer to Table 7 on page 26 for I²C configuration options.

^{21.} Power saving applicable only with a USB 3.0 host. DS ports can be disabled through configuration options. Refer to Table 6 on page 25 for pin-strapping and Table 7 on page 26 for I²C configuration options.



Package Diagrams

Figure 18. 68-pin QFN (8 × 8 × 1.0 mm) LT68B 5.1 × 5.1 mm EPAD (Sawn) Package Outline

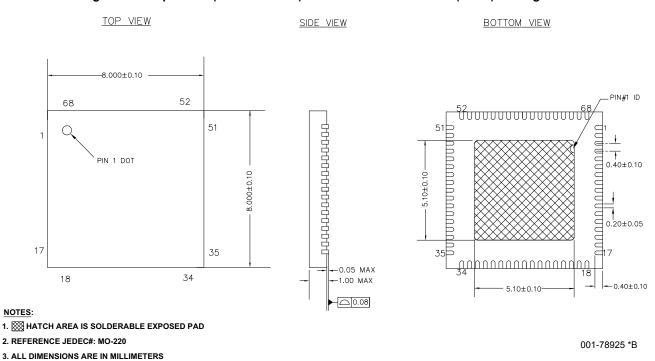
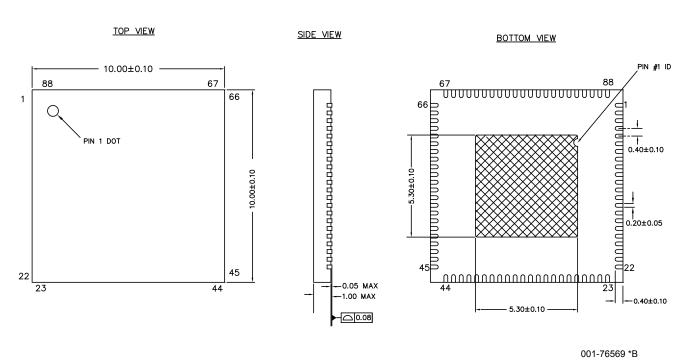


Figure 19. 88-pin QFN (10 \times 10 \times 1.0 mm) LT88B 5.3 \times 5.3 EPAD (Sawn) Package Outline



Document Number: 001-73643 Rev. *P Page 37 of 42



2X 0.10 C (datum B) A1 CORNER Ð В Α 000000000 A1 CORNER <u></u> SD D1 D (datum A) 0000000000 0.10 C 2X eD SE TOP VIEW **BOTTOM VIEW** DETAIL A // 0.10 C A1 C o o oto o o 100хøь <u>/</u>5 Ø0.15(M)C|A|B SIDE VIEW DETAIL A

Figure 20. 100-Ball BGA (6.0 × 6.0 × 1.0 mm) BZ100 Package Outline

SYMBOL	DIMENSIONS			
	MIN.	NOM.	MAX.	
Α	-	-	1.00	
A1	0.16	-	-	
D	6.00 BSC			
Е		6.00 BSC		
D1	4.50 BSC			
E1	4.50 BSC			
MD	10			
ME	10			
N	100			
Øb	0.25 0.30 0.35		0.35	
eD	0.50 BSC			
eE	0.50 BSC			
SD	0.25 BSC			
SE	0.25 BSC			

NOTES:

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- 2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- 3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- 4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

 SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

 N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- 6 "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

 WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW
 "SD" OR "SE" = 0.
 - WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- 8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
- 9. JEDEC SPECIFICATION NO. REF.: MO-195C.

51-85209 *F



Silicon Revision History

This datasheet is applicable for the USB-IF certified (TID# 330000060) HX3 Rev. *D and Rev. *C Silicon.

Rev. *D: This Silicon revision improves the yield of HX3, and is drop-in compatible for all the part numbers. There is no need to change the board design or layout to use the HX3 Rev. *D Silicon. Products are completely compatible with the HX3 Rev. *C Silicon.

Rev. *C: This Silicon revision fixes the errata applicable to the Rev. *A Silicon.

The following table defines the changes between Rev. *A, Rev. *C, and Rev. *D Silicon.

No.	Items	Part Numbers	Rev. *A	Rev. *C	Rev. *D
1	USB-IF Compliance	All	Requires firmware on external EEPROM	No external EEPROM required	No external EEPROM required
	FS-only hub or host connected to HX3 Upstream Port	All	Not supported	Supported	Supported
3	Suspend Power	All	90 mW	37.8 mW	37.8 mW

Method of Identification

Markings on row 3 of the HX3 package differentiate Rev. *D Silicon from Rev. *C Silicon and Rev. *A Silicon as indicated in the example below. Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

HX3 REV *A SILICON



HX3 REV *C SILICON



HX3 REV *D SILICON





Document History Page

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*E	4271496	MURT	02/21/2014	Changed status from Preliminary to Final.
*F	4291210	MURT	02/25/2014	Post to external web.
*G	4308926	MURT	03/14/2014	Updated System Interfaces: Updated Configuration Options: Updated HX3 as I2C Slave: Updated Table 7.
*H	4463533	MURT	08/01/2014	Updated Features: Updated TID#. Updated Electrical Specifications: Updated Power Consumption: Updated Table 9: Updated details corresponding to suspend power. Removed Errata.
*	4483117	RAJM	08/22/2014	Added Silicon Revision History.
*J	4499514	RAJM	09/15/2014	Added BGA package information.
*K	4582512	PRJI	11/28/2014	Updated HX3 Product Options: Updated Table 1. Updated Pin Information: Updated Table 4.
*L	4632890	НВМ	01/20/2015	Updated Pin Information: Updated Figure 12. Updated Figure 13. Updated Table 4. Added Packaging. Updated Package Diagrams: spec 51-85209 – Changed revision from *D to *E.
*M	4669639	HBM	02/24/2015	No technical updates. Completing Sunset Review.
*N	4764583	НВМ	05/13/2015	Updated Package Diagrams: spec 001-76569 – Changed revision from *A to *B. Updated Silicon Revision History. Updated Method of Identification.
*0	4941772	НВМ	11/25/2015	Updated HX3 Product Options: Updated Table 1: Included CYUSB2302-68LTXI and CYUSB2304-68LTXI part numbers related information. Updated Ordering Information: Updated Table 11: Updated part numbers.
*P	5466603	НВМ	10/20/2016	Updated Features: Replaced "USB 3.0-Certified Hub, TID# 330000060" with "USB-IF Certified Hub, TID# 330000060, 30000074". Updated Package Diagrams: spec 51-85209 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Wireless/RF

ARM® Cortex® Microcontrollers cypress.com/arm Automotive cypress.com/automotive Clocks & Buffers cypress.com/clocks Interface cypress.com/interface Internet of Things cypress.com/iot Lighting & Power Control cypress.com/powerpsoc Memory cypress.com/memory **PSoC** cypress.com/psoc Touch Sensing cypress.com/touch **USB Controllers** cypress.com/usb

cypress.com/wireless

PSoC[®]Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2011-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the aliquer of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Document Number: 001-73643 Rev. *P