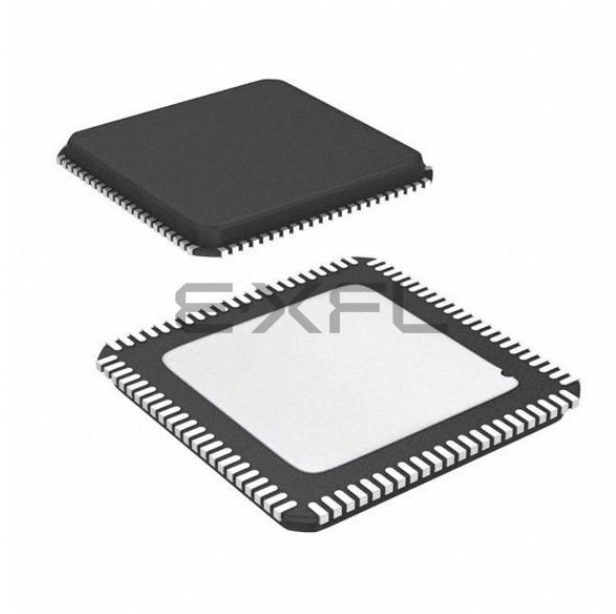

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## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

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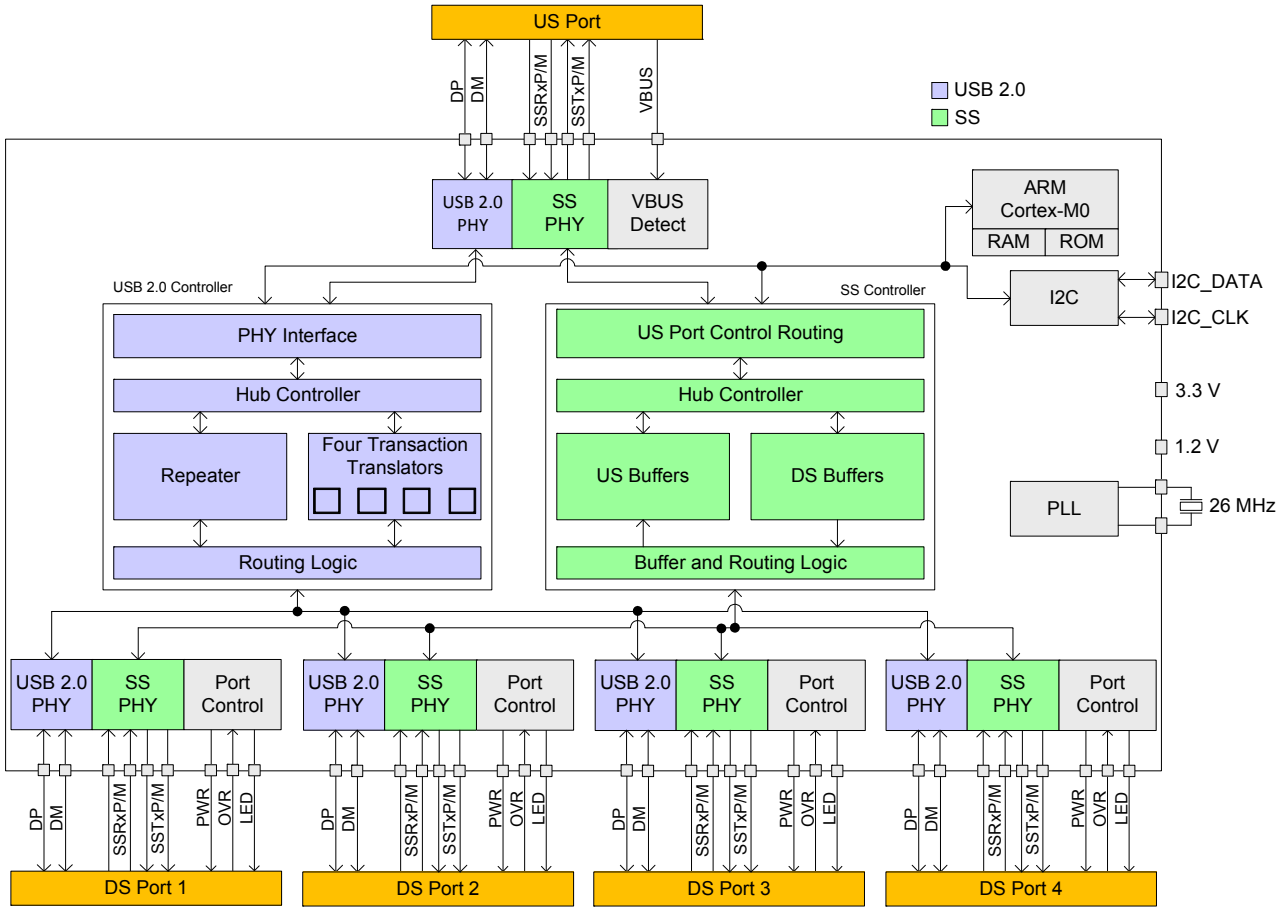
## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Active |
| Applications | USB 3.0 Hub Controller |
| Core Processor | ARM® Cortex®-M0 |
| Program Memory Type | ROM (32kB) |
| Controller Series | CYUSB |
| RAM Size | 16K x 8 |
| Interface | I²C |
| Number of I/O | 10 |
| Voltage - Supply | 1.14V ~ 1.26V, 2.5V ~ 2.7V, 3V ~ 3.6V |
| Operating Temperature | 0°C ~ 70°C |
| Mounting Type | Surface Mount |
| Package / Case | 88-VFQFN Exposed Pad |
| Supplier Device Package | 88-QFN (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3314-88ltxc |

## Block Diagram



## Architecture Overview

The Block Diagram on page 2 shows the HX3 architecture. HX3 consists of two independent hub controllers (SS and USB 2.0), the Cortex-M0 CPU subsystem, an $I^2C$ interface, and port controller blocks.

### SS Hub Controller

This block supports the SS hub functionality based on the USB 3.0 specification. The SS hub controller supports the following:

- SS link power management (U0, U1, U2, U3 states)
- Full-duplex data transmission

### USB 2.0 Hub Controller

This block supports the LS, FS, and HS hub functionalities. It includes the repeater, frame timer, and four transaction translators.

The USB 2.0 hub controller block supports the following:

- USB 2.0 link power management (L0, L1, L2, L3 states)
- Suspend, resume, and remote wake-up signaling
- Multi-TT (one TT for each DS port)

### CPU

The ARM Cortex-M0 CPU subsystem is used for the following functions:

- System configuration and initialization
- Battery charging control
- Vendor-specific commands for the USB-to-$I^2C$ bridge
- String-descriptor support
- Suspend status indicator
- Shared Link support in embedded systems

### $I^2C$ Interface

The $I^2C$ interface in HX3 supports the following:

- $I^2C$ Slave, Master, and Multi-master configurations
  - Configure HX3 by an external $I^2C$ master in $I^2C$ slave mode
  - Configure HX3 from an $I^2C$ EEPROM
  - Multi-master mode to share EEPROM with other $I^2C$ masters
- In-System Programming of the $I^2C$ EEPROM from HX3's US port

### Port Controller

The port controller block controls DS port power to comply with the BC v1.2 and USB 3.0 specifications. This block also controls the US port power in the ACA-Dock mode. Control signals for external power switches are implemented within the chip. HX3 controls the external power switches at power-on to reduce in-rush current.

The port controller block supports the following:

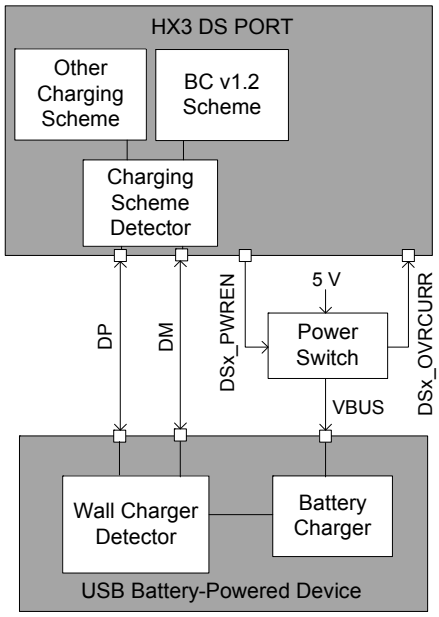
- Overcurrent detection
- SS and USB 2.0 port indicators for each DS port
- Ganged and individual power control modes
- Automatic port numbering based on active ports

## Applications

- Standalone hubs
- PC and tablet motherboards
- Docking station
- Hand-held cradles
- Monitors
- Digital TVs
- Set-top boxes
- Printers

When the US port is disconnected from the host, HX3 detects if any of the DS ports are connected to a device requesting charging. It determines the charging method and then switches to the appropriate signaling based on the detected charging specification as shown in Figure 4. The hub either emulates a USB-compliant dedicated charging port by connecting DP and DM (see the BC v1.2 specification) or other supported proprietary charging schemes.

**Figure 4. Ghost Charge Implementation in HX3**




Ghost Charge is enabled by default and can be disabled through configuration. Refer to Configuration Options on page 24.

## Vendor-Command Support

HX3 supports vendor-specific requests and can also enumerate as a vendor-specific device. The vendor-specific request can be used to (a) bridge USB and $I^2C$ and (b) configure HX3. This feature can be used for the following applications:

- Firmware upgrade of an external ASSP connected to HX3 through USB
- In-System programming (ISP) of an EEPROM connected to HX3 through USB

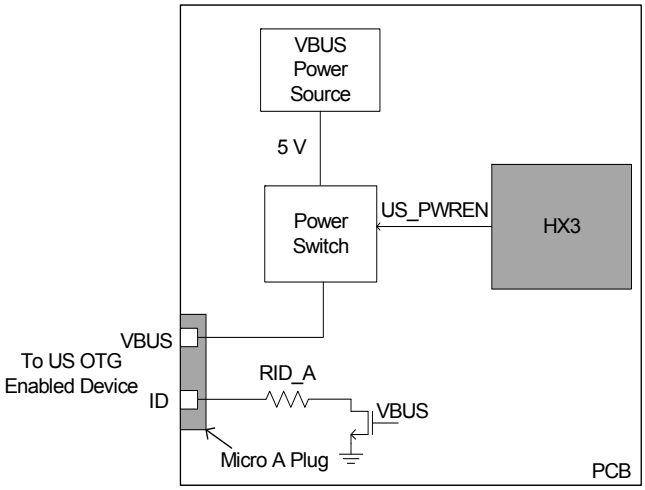
## ACA-Dock Support

In traditional USB topologies, the host provides VBUS to enable and charge the connected devices. For OTG hosts, however, an ACA-Dock provides VBUS and a method to charge the host. HX3 supports the ACA-Dock standard (see BC v1.2 specification) by integrating the functions of the adapter controller.

Figure 5 shows the ACA-Dock system. If the ACA-Dock feature is enabled, HX3 turns on the external power switch to drive VBUS on the US port. To inform the OTG host that it is connected to an ACA-Dock, the ID pin is tied to ground using a resistor RID_A,[3] as shown in Figure 5. The ACA-Dock feature can be disabled using the Configuration Options on page 24.

For example, a BC v1.2 compliant phone such as a Sony Xperia (neo V) can be docked to a HX3-based ACA-Dock system. The phone acts as an OTG host and the ACA-Dock charges the phone connected to the US port while also powering the four DS ports.

**Figure 5. ACA-Dock Support**




**Note**
3. 124 kΩ is the recommended RID_A value as per BC v1.2 specification, but some portable devices use custom RID_A values.

**Figure 7. HX3 68-Pin QFN 4-Port Pinout**

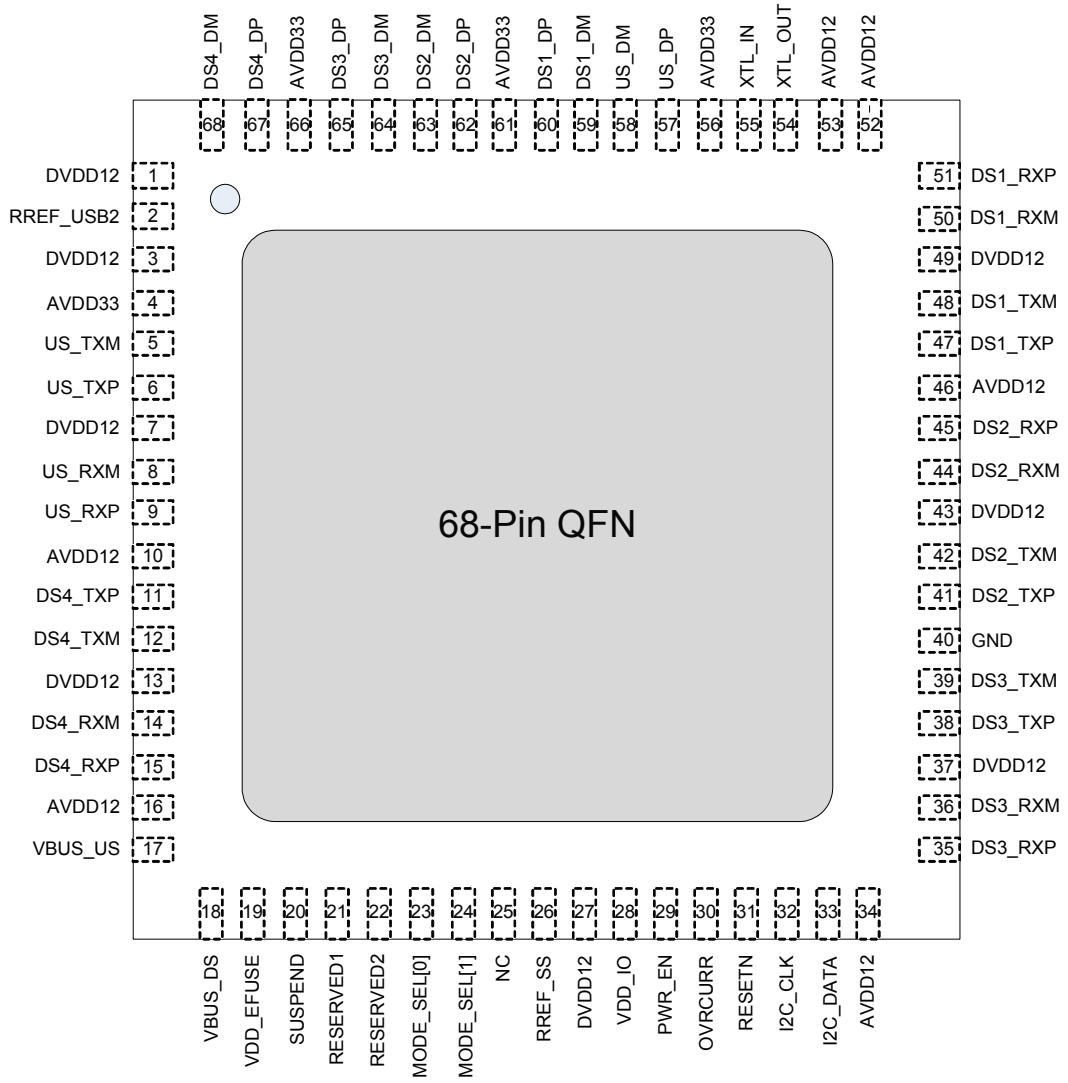


**Figure 8. HX3 100-Ball BGA Pinout for CYUSB3302**

| A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 |
|---|---|---|---|---|---|---|---|---|---|
| NC | NC | NC | AVDD33 | DS2_DM | DS2_DP | AVDD33 | US_DM | US_DP | AVDD12 |
| **B1** | **B2** | **B3** | **B4** | **B5** | **B6** | **B7** | **B8** | **B9** | **B10** |
| NC | NC | NC | VDD_IO | VSS | AVDD33 | NC | NC | NC | DVDD12 |
| **C1** | **C2** | **C3** | **C4** | **C5** | **C6** | **C7** | **C8** | **C9** | **C10** |
| US_TXM | NC | NC | NC | NC | VSS | DS1_DP | DS1_DM | AVDD12 | DS1_RXM |
| **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** | **D8** | **D9** | **D10** |
| US_TXP | NC | NC | DVDD12 | VSS | DVDD12 | VSS | DVDD12 | VSS | DS1_RXP |
| **E1** | **E2** | **E3** | **E4** | **E5** | **E6** | **E7** | **E8** | **E9** | **E10** |
| DVDD12 | RREF_USB2 | NC | NC | XTL_IN | XTL_OUT | VDD_IO | DS1_TXM | VSS | DVDD12 |
| **F1** | **F2** | **F3** | **F4** | **F5** | **F6** | **F7** | **F8** | **F9** | **F10** |
| US_RXM | VSS | AVDD33 | MODE_SEL[1] | DVDD12 | OVRCURR | RESETN | DS1_TXP | AVDD12 | DS2_RXP |
| **G1** | **G2** | **G3** | **G4** | **G5** | **G6** | **G7** | **G8** | **G9** | **G10** |
| US_RXP | VBUS_DS | SUSPEND | RESERVED1 | MODE_SEL[0] | VDD_IO | PWR_EN | I2C_DATA | VSS | DS2_RXM |
| **H1** | **H2** | **H3** | **H4** | **H5** | **H6** | **H7** | **H8** | **H9** | **H10** |
| AVDD12 | VBUS_US | VDD_EFUSE | RESERVED2 | RREF_SS | VSS | DS2_TXM | DS2_TXP | NC | AVDD12 |
| **J1** | **J2** | **J3** | **J4** | **J5** | **J6** | **J7** | **J8** | **J9** | **J10** |
| VSS | AVDD12 | VSS | GPIO | NC | I2C_CLK | NC | NC | VSS | NC |
| **K1** | **K2** | **K3** | **K4** | **K5** | **K6** | **K7** | **K8** | **K9** | **K10** |
| NC | NC | DVDD12 | NC | NC | NC | NC | NC | DVDD12 | NC |

**Table 2. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB3302 and CYUSB3304**

| Pin Name | | Type | 68-QFN Pin# | 100-BGA Ball # | Description |
|---|---|---|---|---|---|
| CYUSB3302 | CYUSB3304 | | | | |
| **US Port** | | | | | |
| US_RXP | | I | 9 | G1 | SuperSpeed receive plus |
| US_RXM | | I | 8 | F1 | SuperSpeed receive minus |
| US_TXP | | O | 6 | D1 | SuperSpeed transmit plus |
| US_TXM | | O | 5 | C1 | SuperSpeed transmit minus |
| US_DP | | I/O | 57 | A9 | USB 2.0 data plus |
| US_DM | | I/O | 58 | A8 | USB 2.0 data minus |
| DS1 Port | | | | | |
| DS1_RXP | | I | 51 | D10 | SuperSpeed receive plus |
| DS1_RXM | | I | 50 | C10 | SuperSpeed receive minus |
| DS1_TXP | | O | 47 | F8 | SuperSpeed transmit plus |
| DS1_TXM | | O | 48 | E8 | SuperSpeed transmit minus |
| DS1_DP | | I/O | 60 | C7 | USB 2.0 data plus |
| DS1_DM | | I/O | 59 | C8 | USB 2.0 data minus |
| **DS2 Port** | | | | | |
| DS2_RXP | | I | 45 | F10 | SuperSpeed receive plus |
| DS2_RXM | | I | 44 | G10 | SuperSpeed receive minus |
| DS2_TXP | | O | 41 | H8 | SuperSpeed transmit plus |
| DS2_TXM | | O | 42 | H7 | SuperSpeed transmit minus |
| DS2_DP | | I/O | 62 | A6 | USB 2.0 data plus |
| DS2_DM | | I/O | 63 | A5 | USB 2.0 data minus |
| **DS3 Port** | | | | | |
| NC | DS3_RXP | I | 35 | K10 | SuperSpeed receive plus |
| NC | DS3_RXM | I | 36 | J10 | SuperSpeed receive minus |
| NC | DS3_TXP | O | 38 | K7 | SuperSpeed transmit plus |
| NC | DS3_TXM | O | 39 | K8 | SuperSpeed transmit minus |
| NC | DS3_DP | I/O | 65 | C4 | USB 2.0 data plus |
| NC | DS3_DM | I/O | 64 | C5 | USB 2.0 data minus |
| **DS4 Port** | | | | | |
| NC | DS4_RXP | I | 15 | K4 | SuperSpeed receive plus |
| NC | DS4_RXM | I | 14 | K5 | SuperSpeed receive minus |
| NC | DS4_TXP | O | 11 | K1 | SuperSpeed transmit plus |
| NC | DS4_TXM | O | 12 | K2 | SuperSpeed transmit minus |
| NC | DS4_DP | I/O | 67 | A3 | USB 2.0 data plus |
| NC | DS4_DM | I/O | 68 | A2 | USB 2.0 data minus |
| OVRCURR | | I | 30 | F6 | Ganged overcurrent input |
| PWR_EN | | I/O | 29 | G7 | Ganged power enable output |
| NC | | I/O | 25 | NA | NC |

**Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X** *(continued)*

| Pin Name | | Type | Pin# | Ball# | Description |
|---|---|---|---|---|---|
| CYUSB3312 | CYUSB3314<br>CYUSB3324<br>CYUSB3326<br>CYUSB3328 | | | | |
| **DS2 Port** | | | | | |
| DS2_RXP | | I | 55 | F10 | SuperSpeed receive plus |
| DS2_RXM | | I | 54 | G10 | SuperSpeed receive minus |
| DS2_TXP | | O | 51 | H8 | SuperSpeed transmit plus |
| DS2_TXM | | O | 52 | H7 | SuperSpeed transmit minus |
| DS2_DP | | I/O | 76 | A6 | USB 2.0 data plus |
| DS2_DM | | I/O | 77 | A5 | USB 2.0 data minus |
| DS2_OVRCURR | | I | 1 | B1 | Overcurrent detect input for DS2 port |
| DS2_PWREN[7] | | I/O | 86 | B2 | VBUS power enable output for DS2 port. When the port is disabled, this pin is in tristate. |
| DS2_CDP_EN[8] | | | | | This pin is called DS2_CDP_EN in the pin-strap configuration mode. |
| DS2_AMBER[7] | | I/O | 5 | E4 | LED_AMBER output for DS2 port |
| NON_REMOVABLE[0][8] | | | | | This pin is called NON_REMOVABLE[0] in the pin-strap configuration mode. |
| DS2_GREEN[7] | | I/O | 6 | E3 | CYUSB3312/3314/3324: LED_GREEN output for DS2 port |
| DS2_VBUSEN_SL[7] | | | | | CYUSB3326/3328: VBUS power enable output for SS port 2 |
| NON_REMOVABLE[1][8] | | | | | This pin is called NON_REMOVABLE[1] in the pin-strap configuration mode. |
| DS2_LED_SS[7] | | I/O | 84 | C3 | LED_SS output for DS2 port |
| PWR_EN_SEL[8] | | | | | This pin is called PWR_EN_SEL in the pin-strap configuration mode. |
| **DS3 Port** | | | | | |
| NC | DS3_RXP | I | 45 | K10 | SuperSpeed receive plus |
| NC | DS3_RXM | I | 46 | J10 | SuperSpeed receive minus |
| NC | DS3_TXP | O | 48 | K7 | SuperSpeed transmit plus |
| NC | DS3_TXM | O | 49 | K8 | SuperSpeed transmit minus |
| NC | DS3_DP | I/O | 79 | C4 | USB 2.0 data plus |
| NC | DS3_DM | I/O | 78 | C5 | USB 2.0 data minus |
| DS3_OVRCURR | | I | 65 | B7 | CYUSB3314/3324/3326/3328: Overcurrent detect input for DS3 port<br>CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO. |
| DS3_PWREN[7] | | I/O | 87 | A1 | VBUS power enable output for DS3 port. When the port is disabled, this pin is in tristate. |
| DS3_CDP_EN[8] | | | | | This pin is called DS3_CDP_EN in the pin-strap configuration mode. |
| DS3_AMBER[7] | | I/O | 85 | B3 | LED_AMBER output for DS3 port |
| VID_SEL[2][8] | | | | | This pin is called VID_SEL[2] in the pin-strap configuration mode. |

**Notes**
7. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
8. For pin-strap configuration details, refer to Table 6 on page 25.

**Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X** *(continued)*

| Pin Name | | Type | Pin# | Ball# | Description |
|---|---|---|---|---|---|
| CYUSB3312 / CYUSB3314 / CYUSB3324 / CYUSB3326 / CYUSB3328 | | | | | |
| DS3_GREEN[9] | | I/O | 64 | B8 | CYUSB3312/3314/3324: LED_GREEN output for DS3 port |
| DS3_VBUSEN_SL[9] | | | | | CYUSB3328: VBUS power enable output for SS port 3 |
| VID_SEL[1][10] | | | | | This pin is called VID_SEL[1] in the pin-strap configuration mode. For pin-strap configuration details, refer to Table 6 on page 25. |
| DS3_LED_SS[9] | | I/O | 63 | B9 | LED_SS output for DS3 port |
| PIN_STRAP[10] | | | | | This pin is called PIN_STRAP in pin-strap configuration mode. When connected to VDD_IO through a 10-kΩ resistor, this pin enables pin-strap configuration mode for HX3. |
| **DS4 Port** | | | | | |
| NC | DS4_RXP | I | 20 | K4 | SuperSpeed receive plus |
| NC | DS4_RXM | I | 19 | K5 | SuperSpeed receive minus |
| NC | DS4_TXP | O | 16 | K1 | SuperSpeed transmit plus |
| NC | DS4_TXM | O | 17 | K2 | SuperSpeed transmit minus |
| NC | DS4_DP | I/O | 81 | A3 | USB 2.0 data plus |
| NC | DS4_DM | I/O | 82 | A2 | USB 2.0 data minus |
| DS4_OVRCURR | | I | 36 | F6 | CYUSB3314/3324/3326/3328: Overcurrent detect input for DS4 port. CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO. |
| DS4_PWREN/PWR_EN4 | | I/O | 35 | G7 | VBUS power enable output for DS4 port. This pin is also used as power enable output when configured in ganged power mode using the Blaster Plus tool. When the port is disabled, this pin is in tristate. |
| DS4_CDP_EN[10] | | | | | This pin is called DS4_CDP_EN in the pin-strap configuration mode. |
| DS4_AMBER[9] | | I/O | 30 | J4 | LED_AMBER output for DS4 port |
| I2C_DEV_ID[10] | | | | | This pin is called I2C_DEV_ID in the pin-strap configuration mode. |
| DS4_GREEN[9] | | I/O | 43 | H9 | CYUSB3312/3314/3324: LED_GREEN output for DS4 port |
| DS4_VBUSEN_SL | | | | | CYUSB3328: VBUS power enable output for SS port 4 |
| VID_SEL[0][10] | | | | | This pin is called VID_SEL[0] in the pin-strap configuration mode. |
| DS4_LED_SS | | I/O | 26 | H4 | LED_SS output for DS4 port. The LED must be connected to GND as shown in Figure 16 on page 25. If LED is not used, this pin must be pulled HIGH using a 10 kΩ to VDD_IO. |
| RESERVED1 | | I | 27 | G4 | This pin must be pulled HIGH using a 10 kΩ to VDD_IO. |
| **Mode Select, Clock, and Reset** | | | | | |
| MODE_SEL[0] | | I | 28 | G5 | Device operation mode select bit 0; refer to Table 5 on page 24 |
| MODE_SEL[1] | | I | 29 | F4 | Device operation mode select bit 1; refer to Table 5 on page 24 |
| XTL_OUT | | A | 68 | E6 | Crystal out |
| XTL_IN | | A | 69 | E5 | Crystal in |
| RESETN | | I | 37 | F7 | Active LOW reset input |
| I2C_CLK | | I/O | 40 | J6 | $I^2C$ clock |
| I2C_DATA | | I/O | 41 | G8 | $I^2C$ data |

**Notes**
9. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
10. For pin-strap configuration details, refer to Table 6 on page 25.

**Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X** *(continued)*

| Pin Name | | Type | Pin# | Ball# | Description |
|---|---|---|---|---|---|
| CYUSB3312 | CYUSB3314<br>CYUSB3324<br>CYUSB3326<br>CYUSB3328 | | | | |
| SUSPEND | | I/O | 25 | G3 | Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state. |
| **Power and Ground** | | | | | |
| VDD_EFUSE | | PWR | 24 | H3 | 1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V |
| AVDD12 | | PWR | 15, 21, 44, 56, 62, 67 | A10, C9, F9, H1, H10, J2 | 1.2 V analog supply |
| GND | | PWR | 50 | B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9 | GND pin |
| DVDD12 | | PWR | 8, 12, 18, 33, 47, 53, 59, 83 | B10, D4, D6, D8, E1, E10, F5, K3, K9 | 1.2 V core supply |
| VBUS _US | | PWR | 22 | H2 | CYUSB3324/3328: Connect the VBUS_US pin to the local 5 V supply. If ACA-Dock mode is disabled using Configuration Options on page 24, this pin must be connected to VBUS from US port.<br>Other part numbers: This pin must be connected to VBUS from US port. |
| VBUS_DS | | PWR | 23 | G2 | This pin is used to power the Apple-charging circuit in HX3.<br>For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply. |
| AVDD33 | | PWR | 9, 70, 75, 80 | A4, A7, B6, F3 | 3.3 V analog supply |
| VDD_IO | | PWR | 34, 66, 88 | B4, E7, G6 | 3.3 V I/O supply |
| **USB Precision Resistors** | | | | | |
| RREF_USB2 | | A | 7 | E2 | Connect pin to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY. |
| RREF_SS | | A | 32 | H5 | Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration. |

## System Interfaces

### Upstream Port (US)

This port is compliant with the USB 3.0 specification and includes an integrated 1.5 kΩ pull-up and termination resistors. It also supports ACA-Dock to enable charging an OTG host connected on the US port.

### Downstream Ports (DS1, 2, 3, 4)

DS ports are compliant with the USB 3.0 specification and integrate 15 kΩ pull-down and termination resistors. Ports can be disabled or enabled, and can be set to removable or non-removable options. BC v1.2 charging is enabled by default and can be disabled on each DS port using the configuration options (see Configuration Options).

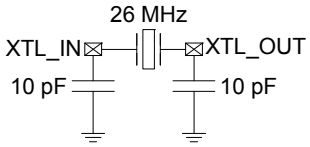
### Communication Interfaces ($I^2C$)

The interface follows the Inter-IC Bus specification, version 3.0, with support for the standard mode (100 kHz) and the fast mode (400 kHz) frequencies. HX3 supports $I^2C$ in the slave and master modes. The $I^2C$ interface supports the multi-master mode of operation. Both the SCL and SDA signals require external pull-up resistors based on the specification. VDD_IO for HX3 is 3.3 V and it is expected that the $I^2C$ pull-up resistors will be connected to the same supply.

### Oscillator

HX3 requires an external crystal with a frequency of 26 MHz and an accuracy of ±150 ppm in parallel resonant, fundamental mode. The crystal drive circuit is capable of a low-power drive level (<200 µW). The crystal connection to the XTL_OUT and XTL_IN pins is shown in Figure 14.

**Figure 14. Crystal Connection**




### GPIOs

HX3 GPIOs are used for overcurrent sensing, controlling external power switches, and driving LEDs. These pins can sink up to 4 mA current each. GPIOs also enable pin-straps for input configuration. Refer to Table 6 for more details.

### Power Control

The PWR_EN[1-4] and OV_CURR[1-4] pins interface HX3 to external power switches. These pins are used to control power switches for DS port power and monitor overcurrent conditions. The power switch polarity and the power control mode (individual and ganged) can be changed using the configuration options.

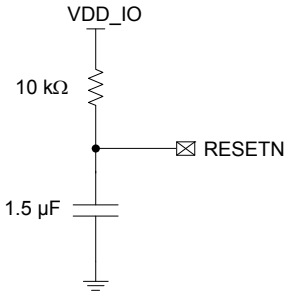
### Reset

HX3 operates with two external power supplies, 3.3 V and 1.2 V. There is no power sequencing requirement between these two supplies. However, the RESETN pin should be held LOW until both these supplies become stable.

The RESETN pin can be tied to VDD_IO through an external resistor and to ground (GND) through an external capacitor (minimum 5 ms time constant), as shown in Figure 15. This creates a clean reset signal for power-on reset (POR).

HX3 does not support internal brown-out detection. If the system requires this feature, an external reset should be provided on the RESETN pin when supplies are below their valid operating ranges.

**Figure 15. Reset Connection**




### Configuration Mode Select

Configuration options are selected through the MODE_SEL pins and the pin-strap enable pin (PIN_STRAP). After power-up, these pins are sampled by an on-chip bootloader to determine the configuration options (see Table 5).

**Table 5. HX3 Boot Sequence**

| MODE SEL[1] | MODE SEL[0] | HX3 Configuration Modes |
|---|---|---|
| 0 | 0 | Reserved. Do not use this mode. |
| 1 | 1 | Internal ROM configuration |
| 0 | 1 | $I^2C$ Master, read configuration from $I^2C$ EEPROM* |
| 1 | 0 | $I^2C$ Slave, configure from an external $I^2C$ Master* |

* Download Cypress-provided firmware from www.cypress.com/hx3.

### Configuration Options

HX3 can be configured by using one of the following:

- eFuse (one-time programmable memory)
- Pin-Strap (read configuration from dedicated pins at power on)
- External $I^2C$ slave such as an EEPROM
- External $I^2C$ master

The $I^2C$ master/slave configuration overrides the pin-strap configuration. Pin-straps override the eFuse configuration, and the eFuse configuration overrides the internal ROM configuration.

*eFuse Configuration*

HX3 contains eFuses, which are OTP elements on the chip that can be electrically blown. The eFuses are read by the bootloader to determine the customer-specific configurations. eFuse programming is supported only at factory and distributor locations where programming conditions can be controlled. eFuse programming is supported under the following conditions:

Temperature range of 25 °C–70 °C and programming voltage of 2.5 V–2.7 V.

*Pin-Strap Configuration*

Pin-straps are supported for select product options (see Table 1 on page 5) to provide reconfigurability without an additional EEPROM. The pin-strap configuration is enabled by pulling the Pin #63 of 88-pin QFN HIGH. Table 6 on page 25 shows the configuration options supported through pin-straps and the GPIOs used for this purpose. Figure 16 and Figure 17 show how the GPIOs need to be connected if pin-strap and LED connection are required or only pin-strap is required.

HX3 samples pin-strap GPIOs at power-up. Floating straps are considered as invalid and the default configuration is used. If PIN_STRAP (Pin #63 of 88-pin QFN) is floating, all strap inputs are considered invalid. A GPIO is considered strapped "1" or "0" when connected with a weak pull-up (10 kΩ) or pull-down (10 kΩ) respectively. After the initial sampling at power-up and reset, the GPIOs are used in their normal functions.

**Figure 16. Pin-Strap With LED or LED-Only Connection**

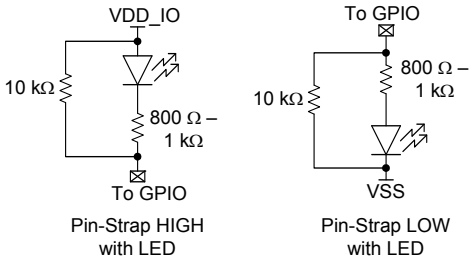



**Figure 17. Pin-Strap Connection**

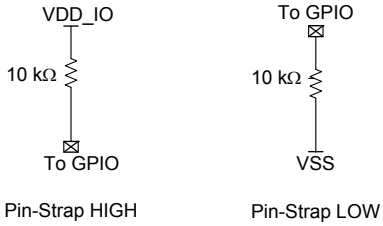



**Table 6. Pin-Strap Configuration**

| 88-QFN Pin # | Pin-Strap Name | Strapped '0'[11] | | Strapped '1'[11] | |
|---|---|---|---|---|---|
| 30 | I2C_DEV_ID[12] | ID 0: HX3 I²C slave address (7 bits) is 0x60. This is also the default I²C slave address for the 68-pin QFN package. | | ID 1: HX3 I²C slave address (7 bits) is 0x58 | |
| 31 | PWR_SW_POL | Power enable and overcurrent will be active LOW | | Power enable and overcurrent will be active HIGH | |
| 2 | ACA_DOCK | Disabled | | Enabled | |
| 84 | PWR_EN_SEL | Individual | | Gang | |
| 63 | PIN_STRAP[13] | No pin-strapping | | Pin-strapping configuration enabled | |
| 4 | PORT_DISABLE[1] | PORT_DISABLE[1:0] =<br>b'00: DS1, DS2, DS3, DS4 active<br>b'01: DS1, DS2, DS3 active<br>b'10: DS1, DS2 active<br>b'11: DS1 active<br>Pin-straps cannot enable ports disabled by factory setting. | | | |
| 3 | PORT_DISABLE[0] | | | | |
| 6 | NON_REMOVABLE[1][14] | NON_REMOVABLE[1:0] =<br>b'00: DS1, DS2, DS3, DS4 removable<br>b'01: DS1, DS2, DS3 removable<br>b'10: DS1, DS2 removable<br>b'11: DS1 removable | | | |
| 5 | NON_REMOVABLE[0][14] | | | | |
| 85 | VID[2] | Reserved. If PIN_STRAP is enabled and CY VID is required, strap VID[2:0] to '1'. | | | |
| 64 | VID[1] | | | | |
| 43 | VID[0] | | | | |
| 38 | DS1_CDP_EN[15] | strapped '0' | strapped '1' | strapped '0' | strapped '1' |
| | | DS1 CDP enabled | DS1 CDP disabled | DS1 CDP disabled | DS1 CDP enabled |
| 86 | DS2_CDP_EN[15] | DS2 CDP enabled | DS2 CDP disabled | DS2 CDP disabled | DS2 CDP enabled |
| 87 | DS3_CDP_EN[15] | DS3 CDP enabled | DS3 CDP disabled | DS3 CDP disabled | DS3 CDP enabled |
| 35 | DS4_CDP_EN[15] | DS4 CDP enabled | DS4 CDP disabled | DS4 CDP disabled | DS4 CDP enabled |

**Notes**
11. See Figure 16 and Figure 17.
12. I2C_DEV_ID is valid only when HX3 is in I²C slave mode.
13. VID, PORT_DISABLE, NON_REMOVABLE are group straps. If one of the pins in a group strap is floating (INVALID), that group input will be INVALID and the default will not be overwritten.
14. These DS ports are exposed ports and the connected devices can be removed.
15. DSx_CDP_EN will be active LOW input when PWR_SW_POL is set to active LOW; similarly DSx_CDP_EN will be active HIGH input when PWR_SW_POL is set to active HIGH.

### *I²C Configuration*

When enabled for I²C configuration through the MODE_SEL pins (See Table 5 on page 24), HX3 can be configured as an I²C master or as an I²C slave. HX3's configuration data is a maximum of 197 bytes and HX3's firmware is 10 KB. Note that HX3's firmware also includes configuration settings.

### *HX3 as I²C Master*

HX3 reads configurations from an external I²C EEPROM with sizes ranging from 16 to 64 KB. An example of a supported EEPROM is 24LC128. Based on the contents of the bSignature and bImageType fields in Table 7 on page 26, HX3 performs one of the following actions:

- Loads custom configuration settings from the EEPROM when bSignature is "CY" and bImageType is 0xD4.
- Loads the Cypress-provided firmware from the EEPROM when bSignature is "CY" and bImageType is 0xB0. This firmware also includes configuration settings.
- If bSignature ≠ "CY", HX3 enumerates in the vendor-specific mode.

The contents of the EEPROM can be updated with the easy-to-use Cypress Blaster Plus tool. Blaster Plus is a GUI-based tool to configure HX3. This tool allows to do the following:

- Download the Cypress-provided firmware from a PC via HX3's US port and store it on an EEPROM connected to HX3's I²C port.
- Read the configuration settings from the EEPROM. These settings are displayed in the Blaster Plus GUI. Modify settings as required.
- Write back the updated settings on to the EEPROM. In addition, an image file can be created for external use.

The Blaster Plus tool, user guide, and the Cypress-provided firmware are available at www.cypress.com/hx3.

### *HX3 as I²C Slave*

An external I²C master can program the configuration settings into HX3 according to the EEPROM map in Table 7 on page 26. Alternatively, the HX3 firmware (<10 KB), which includes configuration settings, can also be programmed. It is recommended to use the Blaster Plus tool to create the HX3 firmware or configuration image file. HX3's I²C slave address needs to be provided while creating the image file. Refer to Table 6 for HX3's I²C slave address.

**Table 7. EEPROM Map**

| I²C Offset | Bits | Name | Default | Description |
|---|---|---|---|---|
| 0 | 7:0 | bSignature LSB ("C") | 0x43 | The first byte of the 2-byte signature initialized with "CY" ASCII text.<br>When the signature is not valid, the hub enumerates as a vendor-specific device. |
| 1 | 7:0 | bSignature MSB ("Y") | 0x59 | The second byte of the 2-byte signature initialized with "CY" ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device. |
| 2 | 7:6 | bImageCTL | b'00 | Reserved |
| | 5:4 | I²C Speed | b'11 | b'01: 400 kHz<br>b'11: 100 kHz |
| | 3:1 | bImageCTL | b'000 | Reserved |
| | 0 | bImageCTL | 0 | 0: Execution binary file<br>1: Data file |
| 3 | 7:0 | bImageType | 0xD4 | 0xD4: Load only configuration<br>0xB0: Load firmware boot image<br>All other bImageType will return an error code. |
| 4 | 7:0 | bD4Length | 40 | bD4Length is defined in bytes as the length from offset 5.<br>I²C offset bytes 0–4 are the header bytes.<br>bD4Length = 6: Only update VID, PID, and DID<br>bD4Length = 18: Configuration options (no PHY trim)<br>bD4Length = 40: Configuration options with PHY trim options<br>bD4Length > 40: User must provide valid string descriptors<br>bD4Length > 192: Error |
| 5 | 7:0 | VID [7:0] | 0xB4 | Custom Vendor ID - LSB |
| 6 | 7:0 | VID [15:8] | 0x04 | Custom Vendor ID - MSB |
| 7 | 7:0 | PID [7:0] | 0x04 | Custom Product ID (PID)<br>Default: 0x6504<br>If separate PID is used for USB 2.0, the USB 2.0 PID will be read from offset 35 and 36.<br>Else, USB 2.0 PID = PID+2; Default: 0x6506 |
| 8 | 7:0 | PID [15:8] | 0x65 | |

**Table 7. EEPROM Map** *(continued)*

| I²C Offset | Bits | Name | Default | Description |
|---|---|---|---|---|
| 9 | 7:0 | DID [7:0] | 00 - 88-pin QFN, 10 - 68-pin QFN | Custom Device ID - revision - LSB |
| 10 | 7:0 | DID [15:8] | 50 | Custom Device ID - revision - MSB |
| 11 | 7:0 | Reserved | 0 | Reserved |
| 12 | 7:4 | SHARED_LINK_EN | b'0000 | Enable Shared Link on DS port<br>bit[7:4]=DS4, DS3, DS2, DS1<br>0: Shared Link not enabled<br>1: Shared Link enabled |
| | 3:0 | SHC_ACTIVE_PORTS [3:0] | b'1111 | Indicates if a SuperSpeed port is active.<br>bit[3:0] = DS4, DS3, DS2, DS1<br>0: Not active<br>1: Active |
| 13 | 7:0 | POWER_ON_TIME | 0x32 | Time (in 2-ms intervals) from the time the power-on sequence begins on a port until power is good on that port (bPwron2PwrGood) |
| 14 | 7:4 | REMOVABLE_PORTS [3:0] | b'1111 | Indicates if the port is removable.<br>bit[7:4]=DS4, DS3, DS2, DS1<br>0: Non-removable<br>1: Removable |
| | 3:0 | UHC_ACTIVE_PORTS [3:0] | b'1111 | Indicates if a USB 2.0 port is active.<br>bit[3:0]=DS4, DS3, DS2, DS1<br>0: Not active<br>1: Active |
| 15 | 7 | SS_LED_PIN_CONTROL | 0 | Port 1–4: SS LED disable<br>0: DS[1:4]_LED_SS are LEDs. The LED glows when the SS port is active and not in disabled state.<br>1: DS[1:4]_LED_SS are not LEDs |
| | 6 | GREEN_LED_PIN_CONTROL | 0 | Port 1–4: USB 2.0 Green LED disable<br>0: DS[1:4]_GREEN are LEDs<br>1: DS[1:4]_GREEN are not LEDs |
| | 5 | AMBER_LED_PIN_CONTROL | 0 | Port 1–4: USB 2.0 Amber LED disable<br>0: DS[1:4]_AMBER are LEDs<br>1: DS[1:4]_AMBER are not LEDs |
| | 4 | PORT_INDICATORS | 1 | Port indicators supported<br>0: Port indicators are not supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request has no effect.<br>1: Port indicators are supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request controls the indicators. |
| | 3 | COMPOUND_HUB | 0 | Identifies a compound device.<br>0: Hub is not part of a compound device.<br>1: Hub is part of a compound device. |
| | 2:1 | Reserved | 0 | Reserved |
| | 0 | GANG | 0 | 1: Ganged power switch enable for all DS ports<br>0: Individual port power switch enable for each DS port |

**Table 7. EEPROM Map** *(continued)*

| I²C Offset | Bits | Name | Default | Description |
|---|---|---|---|---|
| 51 + X | 7:0 | bString: Product | 'C', 0, 'Y', 0, '-', 0, 'H', 0, 'X', 0, '3', 0, ' ', 0, 'H', 0, 'U', 0, 'B', 0 | Product string: UNICODE UTF-16LE per USB 2.0 specification: "CY-HX3 HUB" |
| 49 + X + Y | 7:0 | bLength: Serial Number (Z) | 22 | Serial number string length ("bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number" should be less than or equal to 152 bytes). Z ≤ 66. |
| 50 + X + Y | 7:0 | DescType | 3 | String descriptor type (constant value) |
| 51 + X + Y | 7:0 | bString: Serial Number | '1', 0, '2', 0, '3', 0, '4', 0, '5', 0, '6', 0, '7', 0, '8', 0, '9', 0, 'A', 0 | Serial number string: UNICODE UTF-16LE per USB 2.0 specification: "123456789A" |

## EMI

HX3 meets the EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. HX3 tolerates EMI conducted by aggressors outlined by the above specifications and continues to function as expected.

## ESD

HX3 has a built-in ESD protection on all pins. The ESD protection level provided on these ports is 2.2 kV Human Body Model (HBM) based on the JESD22-A114 specification.

## Packaging

**Table 12. Package Characteristics**

| Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_A$ | Operating ambient temperature | –40 | – | 85 | °C |
| $T_J$ | Operating junction temperature | –40 | – | 125 | °C |
| $T_{JA}$ | Package $J_A$ (68-pin QFN) | – | 16.2 | – | °C/W |
| $T_{JA}$ | Package $J_A$ (88-pin QFN) | – | 15.7 | – | °C/W |
| $T_{JA}$ | Package $J_A$ (100-ball BGA) | – | 35 | – | °C/W |
| $T_{JC}$ | Package $J_C$ (68-pin QFN) | – | 23.8 | – | °C/W |
| $T_{JC}$ | Package $J_C$ (88-pin QFN) | – | 18.9 | – | °C/W |
| $T_{JC}$ | Package $J_C$ (100-ball BGA) | – | 12 | – | °C/W |

**Table 13. Solder Reflow Peak Temperature**

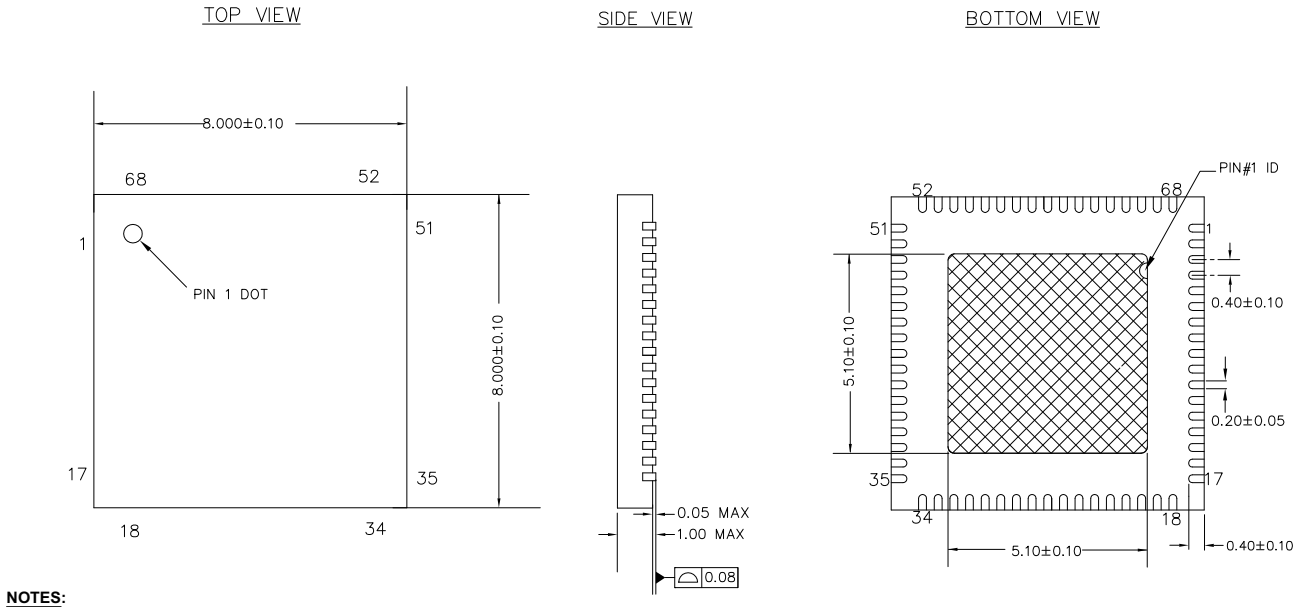
| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---|---|---|
| 68-pin QFN | 260 °C | 30 seconds |
| 88-pin QFN | 260 °C | 30 seconds |
| 100-ball BGA | 260 °C | 30 seconds |

**Table 14. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Package | MSL |
|---|---|
| 68-pin QFN | MSL 3 |
| 88-pin QFN | MSL 3 |
| 100-ball BGA | MSL 3 |

## Package Diagrams

**Figure 18. 68-pin QFN (8 × 8 × 1.0 mm) LT68B 5.1 × 5.1 mm EPAD (Sawn) Package Outline**

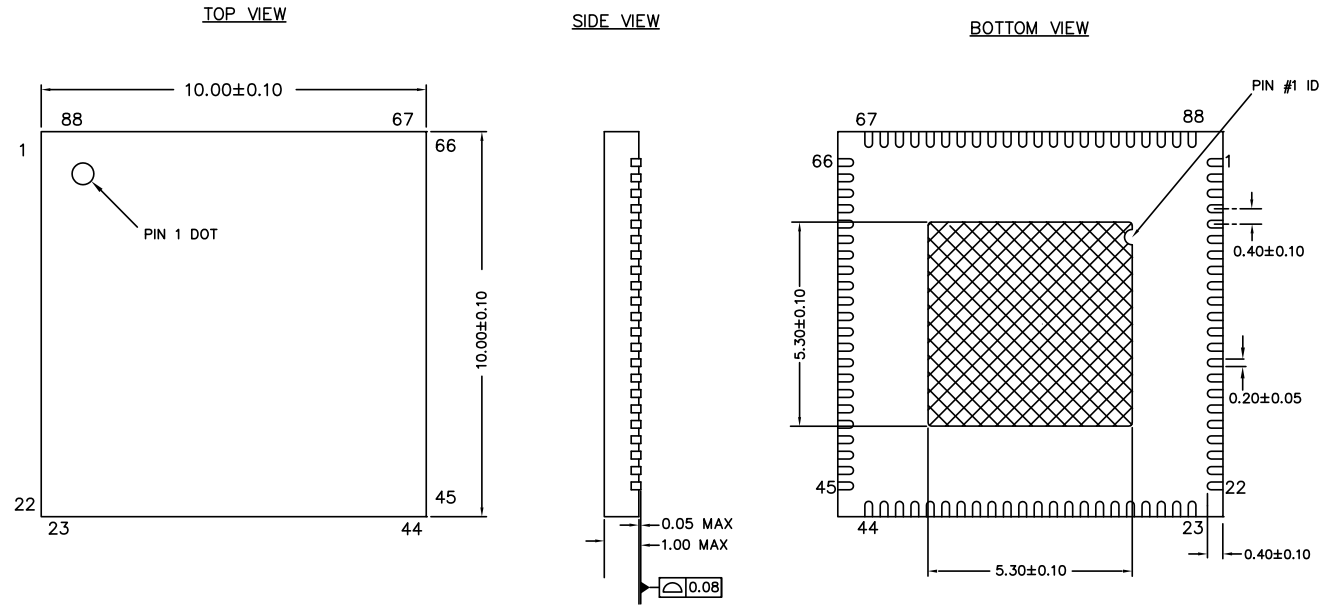



**NOTES:**

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC#: MO-220
3. ALL DIMENSIONS ARE IN MILLIMETERS

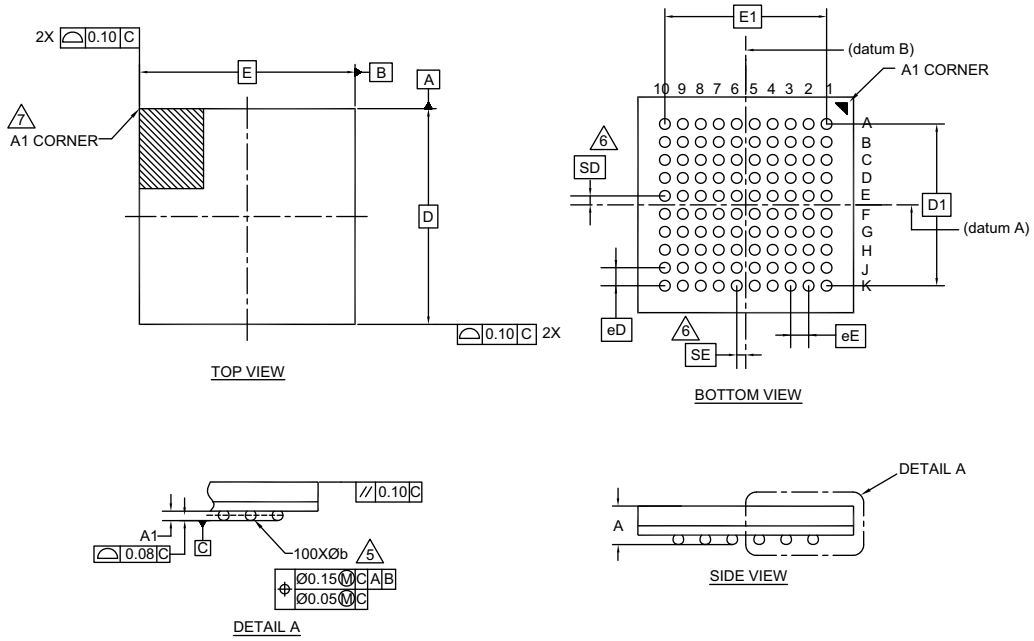
001-78925 *B

**Figure 19. 88-pin QFN (10 × 10 × 1.0 mm) LT88B 5.3 × 5.3 EPAD (Sawn) Package Outline**




001-76569 *B

**Figure 20. 100-Ball BGA (6.0 × 6.0 × 1.0 mm) BZ100 Package Outline**




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.00 |
| A1 | 0.16 | - | - |
| D | 6.00 BSC | | |
| E | 6.00 BSC | | |
| D1 | 4.50 BSC | | |
| E1 | 4.50 BSC | | |
| MD | 10 | | |
| ME | 10 | | |
| N | 100 | | |
| ∅ b | 0.25 | 0.30 | 0.35 |
| eD | 0.50 BSC | | |
| eE | 0.50 BSC | | |
| SD | 0.25 BSC | | |
| SE | 0.25 BSC | | |

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-195C.

51-85209 *F

## Acronyms

**Table 15. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| ACA | Accessory Charging Adapter |
| ASSP | Application-Specific Standard Product |
| BC | Battery Charging |
| CDP | Charging Downstream Port |
| DS | DownStream |
| DCP | Dedicated Charging Port |
| DNU | Do Not Use |
| DWG | Device Working Group |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| FS | Full-Speed |
| FW | FirmWare |
| GND | GrouND |
| GPIO | General-Purpose Input/Output |
| HS | Hi-Speed |
| ISP | In-System Programming |
| I/O | Input/Output |
| LS | Low-Speed |
| NC | No Connect |
| OTG | On-The-Go |
| PID | Product ID |
| POR | Power-On Reset |
| ROM | Read-Only Memory |
| SCL | Serial CLock |
| SDA | Serial DAta |
| SS | SuperSpeed |
| TT | Transaction Translator |
| US | UpStream |
| VID | Vendor ID |

## Reference Documents

*USB 2.0 Specification*

*USB 3.0 Specification*

*Battery Charging Specification*

## Document Conventions

### Units of Measure

**Table 16. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degree celsius |
| Ω | ohm |
| Gbps | gigabit per second |
| KB | kilobyte |
| kHz | kilohertz |
| kΩ | kiloohm |
| Mbps | megabit per second |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| ms | millisecond |
| mW | milliwatt |
| ns | nanosecond |
| ppm | parts per million |
| V | volt |

## Document History Page

| Document Title: CYUSB330x/CYUSB331x/CYUSB332x/CYUSB230x, HX3 USB 3.0 Hub<br>Document Number: 001-73643 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *E | 4271496 | MURT | 02/21/2014 | Changed status from Preliminary to Final. |
| *F | 4291210 | MURT | 02/25/2014 | Post to external web. |
| *G | 4308926 | MURT | 03/14/2014 | Updated System Interfaces:<br>Updated Configuration Options:<br>Updated HX3 as I2C Slave:<br>Updated Table 7. |
| *H | 4463533 | MURT | 08/01/2014 | Updated Features:<br>Updated TID#.<br>Updated Electrical Specifications:<br>Updated Power Consumption:<br>Updated Table 9:<br>Updated details corresponding to suspend power.<br>Removed Errata. |
| *I | 4483117 | RAJM | 08/22/2014 | Added Silicon Revision History. |
| *J | 4499514 | RAJM | 09/15/2014 | Added BGA package information. |
| *K | 4582512 | PRJI | 11/28/2014 | Updated HX3 Product Options:<br>Updated Table 1.<br>Updated Pin Information:<br>Updated Table 4. |
| *L | 4632890 | HBM | 01/20/2015 | Updated Pin Information:<br>Updated Figure 12.<br>Updated Figure 13.<br>Updated Table 4.<br>Added Packaging.<br>Updated Package Diagrams:<br>spec 51-85209 – Changed revision from *D to *E. |
| *M | 4669639 | HBM | 02/24/2015 | No technical updates.<br>Completing Sunset Review. |
| *N | 4764583 | HBM | 05/13/2015 | Updated Package Diagrams:<br>spec 001-76569 – Changed revision from *A to *B.<br>Updated Silicon Revision History.<br>Updated Method of Identification. |
| *O | 4941772 | HBM | 11/25/2015 | Updated HX3 Product Options:<br>Updated Table 1:<br>Included CYUSB2302-68LTXI and CYUSB2304-68LTXI part numbers related information.<br>Updated Ordering Information:<br>Updated Table 11:<br>Updated part numbers. |
| *P | 5466603 | HBM | 10/20/2016 | Updated Features:<br>Replaced “USB 3.0-Certified Hub, TID# 330000060” with “USB-IF Certified Hub, TID# 330000060, 30000074”.<br>Updated Package Diagrams:<br>spec 51-85209 – Changed revision from *E to *F.<br>Updated to new template.<br>Completing Sunset Review. |

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