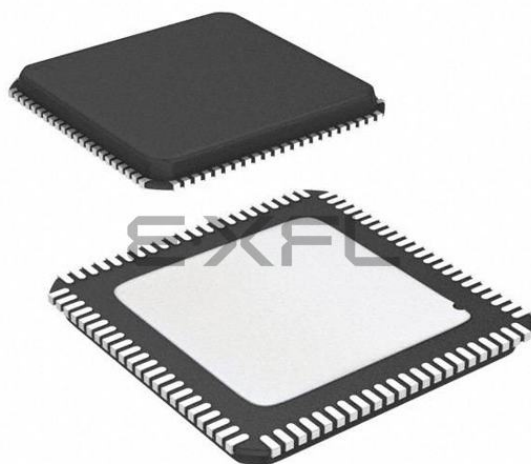




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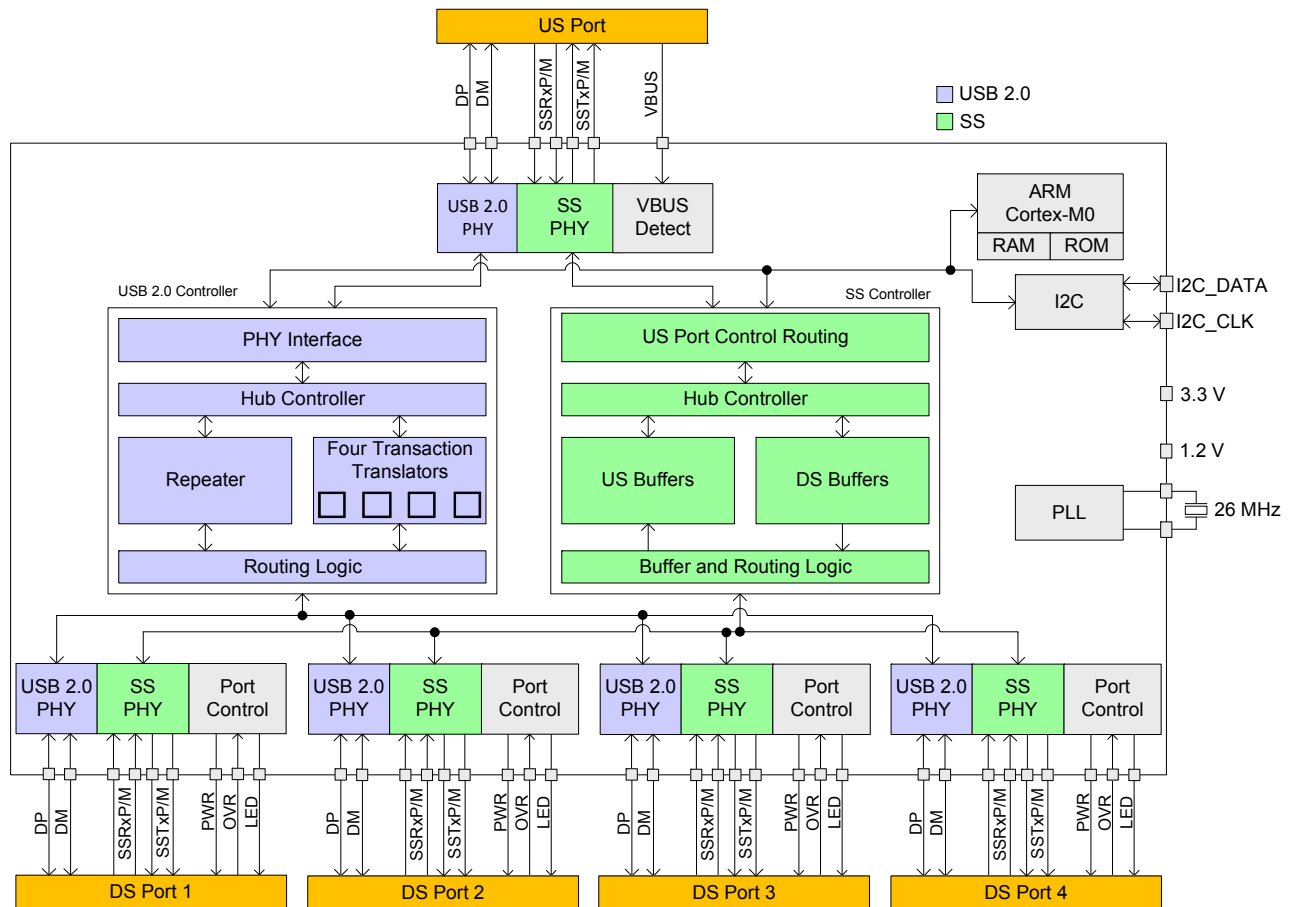
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Application specific microcontrollers are engineered to

Details

Product Status	Active
Applications	USB 3.0 Hub Controller
Core Processor	ARM® Cortex®-M0
Program Memory Type	ROM (32kB)
Controller Series	CYUSB
RAM Size	16K x 8
Interface	I ² C
Number of I/O	10
Voltage - Supply	1.14V ~ 1.26V, 2.5V ~ 2.7V, 3V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad
Supplier Device Package	88-QFN (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3314-88ltxct

Block Diagram



Contents

Architecture Overview	4	EMI	31
SS Hub Controller	4	ESD	31
USB 2.0 Hub Controller	4	Absolute Maximum Ratings	32
CPU	4	Electrical Specifications	32
I2C Interface	4	DC Electrical Characteristics	32
Port Controller	4	Power Consumption	33
Applications	4	Ordering Information	34
HX3 Product Options	5	Ordering Code Definitions	35
Product Features	6	Packaging	36
Shared Link	6	Package Diagrams	37
Ghost Charge	6	Acronyms	39
Vendor-Command Support	7	Reference Documents	39
ACA-Dock Support	7	Document Conventions	39
Pin Information	8	Units of Measure	39
System Interfaces	24	Silicon Revision History	40
Upstream Port (US)	24	Method of Identification	40
Downstream Ports (DS1, 2, 3, 4)	24	Document History Page	41
Communication Interfaces (I2C)	24	Sales, Solutions, and Legal Information	42
Oscillator	24	Worldwide Sales and Design Support	42
GPIOs	24	Products	42
Power Control	24	PSoC@Solutions	42
Reset	24	Cypress Developer Community	42
Configuration Mode Select	24	Technical Support	42
Configuration Options	24		

HX3 Product Options

Table 1. HX3 Product Options

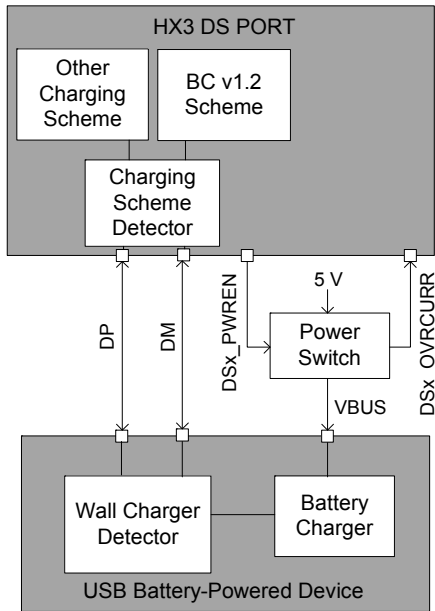
Features	CYUSB3302	CYUSB3304	CYUSB3312	CYUSB3314	CYUSB3324	CYUSB3326	CYUSB3328	CYUSB2302-68LTXI	CYUSB2304-68LTXI
Number of DS ports	2 (USB 3.0)	4 (USB 3.0)	2 (USB 3.0)	4 (USB 3.0)	4 (USB 3.0)	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	8 (4 SS, 4 USB 2.0)	2 (USB 2.0)	4 (USB 2.0)
Number of Shared Link ports	0	0	0	0	0	2 ^[1]	4	0	0
BC v1.2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACA-Dock	No	No	No	No	Yes	No	Yes	No	No
External Power Switch Control	Ganged	Ganged	Individual and Ganged	Individual and Ganged	Individual and Ganged	Individual	Individual	Ganged	Ganged
Pin-Strap support	No	No	Yes	Yes	Yes	Yes	Yes	No	No
I ² C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Vendor command	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Port indicators	No	No	Yes	Yes	Yes	No	No	No	No
Packages ^[2]	68-QFN, 100-ball BGA	68-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	88-QFN, 100-ball BGA	68-QFN, 100-ball BGA	68-QFN, 100-ball BGA
Temperature range	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial and Commercial	Industrial (88-QFN only) and Commercial	Industrial and Commercial	Industrial and Commercial

Notes

- DS1 and DS2 are Shared link Ports.
- BGA Industrial Grade packages are limited to 1 W of active power. For power calculations refer to [Table 10](#) on page 33.

When the US port is disconnected from the host, HX3 detects if any of the DS ports are connected to a device requesting charging. It determines the charging method and then switches to the appropriate signaling based on the detected charging specification as shown in [Figure 4](#). The hub either emulates a USB-compliant dedicated charging port by connecting DP and DM (see the BC v1.2 specification) or other supported proprietary charging schemes.

Figure 4. Ghost Charge Implementation in HX3



Ghost Charge is enabled by default and can be disabled through configuration. Refer to [Configuration Options on page 24](#).

Vendor-Command Support

HX3 supports vendor-specific requests and can also enumerate as a vendor-specific device. The vendor-specific request can be used to (a) bridge USB and I²C and (b) configure HX3. This feature can be used for the following applications:

- Firmware upgrade of an external ASSP connected to HX3 through USB
- In-System programming (ISP) of an EEPROM connected to HX3 through USB

Note

3. 124 kΩ is the recommended RID_A value as per BC v1.2 specification, but some portable devices use custom RID_A values.

ACA-Dock Support

In traditional USB topologies, the host provides VBUS to enable and charge the connected devices. For OTG hosts, however, an ACA-Dock provides VBUS and a method to charge the host. HX3 supports the ACA-Dock standard (see BC v1.2 specification) by integrating the functions of the adapter controller.

[Figure 5](#) shows the ACA-Dock system. If the ACA-Dock feature is enabled, HX3 turns on the external power switch to drive VBUS on the US port. To inform the OTG host that it is connected to an ACA-Dock, the ID pin is tied to ground using a resistor RID_A,³ as shown in [Figure 5](#). The ACA-Dock feature can be disabled using the [Configuration Options on page 24](#).

For example, a BC v1.2 compliant phone such as a Sony Xperia (neo V) can be docked to a HX3-based ACA-Dock system. The phone acts as an OTG host and the ACA-Dock charges the phone connected to the US port while also powering the four DS ports.

Figure 5. ACA-Dock Support

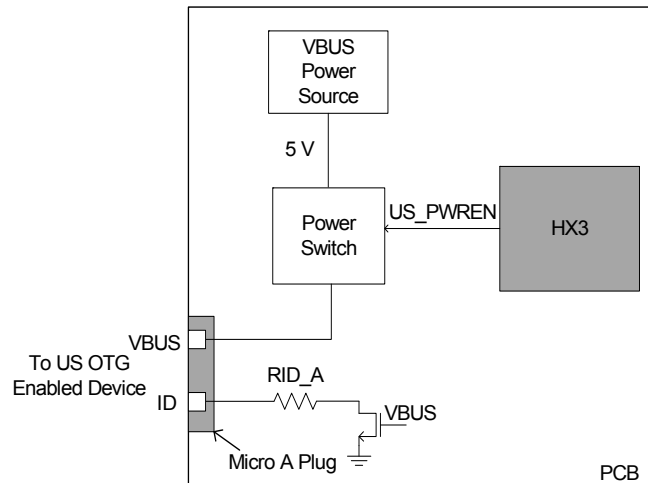


Figure 7. HX3 68-Pin QFN 4-Port Pinout

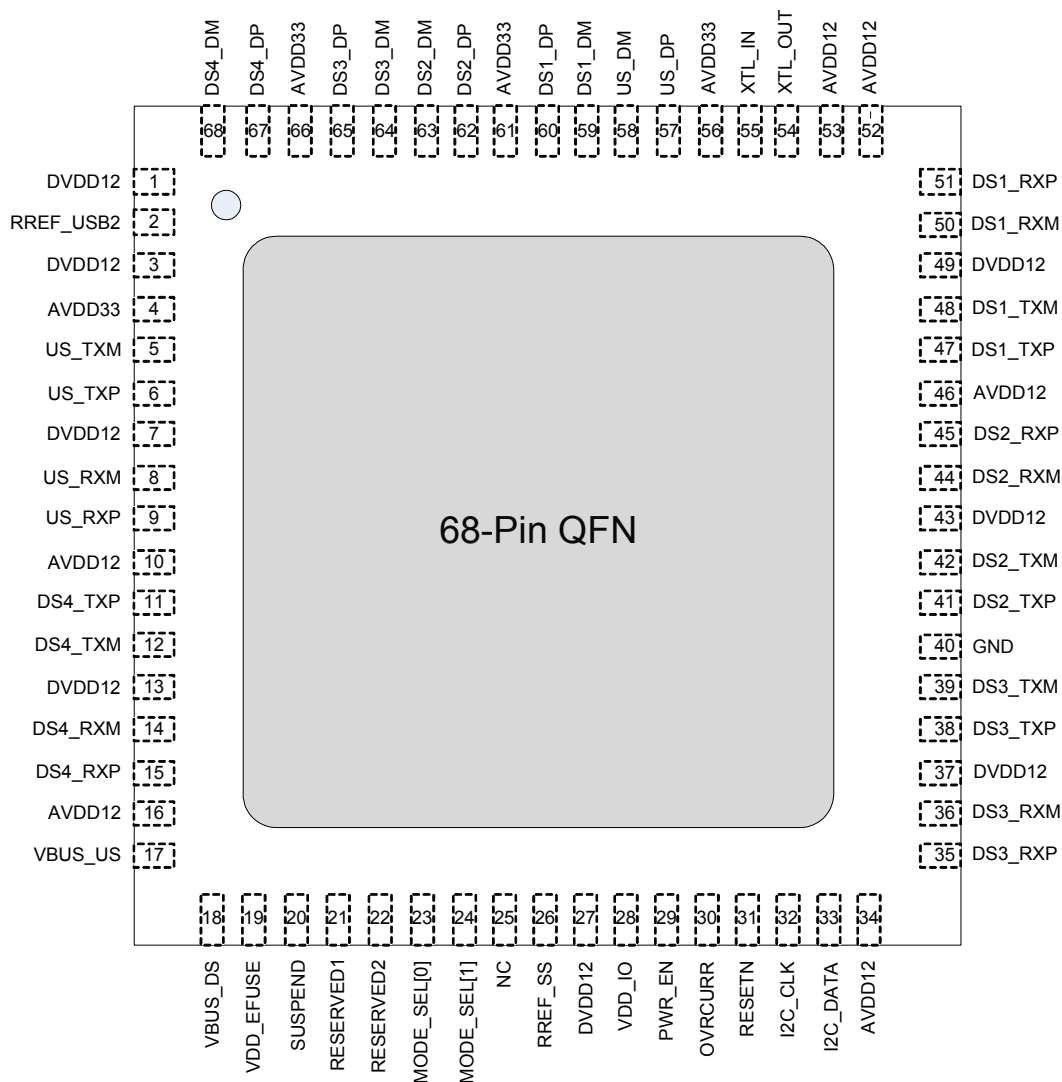


Figure 8. HX3 100-Ball BGA Pinout for CYUSB3302

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
NC	NC	NC	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
NC	NC	NC	VDD_IO	VSS	AVDD33	NC	NC	NC	DVDD12
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
US_TXM	NC	NC	NC	NC	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
US_TXP	NC	NC	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
DVDD12	RREF_US B2	NC	NC	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
US_RXM	VSS	AVDD33	MODE_SE L[1]	DVDD12	OVRCUR R	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
US_RXP	VBUS_DS	SUSPEND	RESERVE D1	MODE_SE L[0]	VDD_IO	PWR_EN	I2C_DATA	VSS	DS2_RXM
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
AVDD12	VBUS_US	VDD_EFUS SE	RESERVE D2	RREF_SS	VSS	DS2_TXM	DS2_TXP	NC	AVDD12
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
VSS	AVDD12	VSS	GPIO	NC	I2C_CLK	NC	NC	VSS	NC
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
NC	NC	DVDD12	NC	NC	NC	NC	NC	DVDD12	NC

Table 2. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB3302 and CYUSB3304

Pin Name		Type	68-QFN Pin#	100-BGA Ball #	Description
CYUSB3302	CYUSB3304				
US Port					
US_RXP		I	9	G1	SuperSpeed receive plus
US_RXM		I	8	F1	SuperSpeed receive minus
US_TXP		O	6	D1	SuperSpeed transmit plus
US_TXM		O	5	C1	SuperSpeed transmit minus
US_DP		I/O	57	A9	USB 2.0 data plus
US_DM		I/O	58	A8	USB 2.0 data minus
DS1 Port					
DS1_RXP		I	51	D10	SuperSpeed receive plus
DS1_RXM		I	50	C10	SuperSpeed receive minus
DS1_TXP		O	47	F8	SuperSpeed transmit plus
DS1_TXM		O	48	E8	SuperSpeed transmit minus
DS1_DP		I/O	60	C7	USB 2.0 data plus
DS1_DM		I/O	59	C8	USB 2.0 data minus
DS2 Port					
DS2_RXP		I	45	F10	SuperSpeed receive plus
DS2_RXM		I	44	G10	SuperSpeed receive minus
DS2_TXP		O	41	H8	SuperSpeed transmit plus
DS2_TXM		O	42	H7	SuperSpeed transmit minus
DS2_DP		I/O	62	A6	USB 2.0 data plus
DS2_DM		I/O	63	A5	USB 2.0 data minus
DS3 Port					
NC	DS3_RXP	I	35	K10	SuperSpeed receive plus
NC	DS3_RXM	I	36	J10	SuperSpeed receive minus
NC	DS3_TXP	O	38	K7	SuperSpeed transmit plus
NC	DS3_TXM	O	39	K8	SuperSpeed transmit minus
NC	DS3_DP	I/O	65	C4	USB 2.0 data plus
NC	DS3_DM	I/O	64	C5	USB 2.0 data minus
DS4 Port					
NC	DS4_RXP	I	15	K4	SuperSpeed receive plus
NC	DS4_RXM	I	14	K5	SuperSpeed receive minus
NC	DS4_TXP	O	11	K1	SuperSpeed transmit plus
NC	DS4_TXM	O	12	K2	SuperSpeed transmit minus
NC	DS4_DP	I/O	67	A3	USB 2.0 data plus
NC	DS4_DM	I/O	68	A2	USB 2.0 data minus
OVRCURR		I	30	F6	Ganged overcurrent input
PWR_EN		I/O	29	G7	Ganged power enable output
NC		I/O	25	NA	NC

Figure 12. HX3 100-Ball BGA Pinout for CYUSB3312

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
DS3_PWR EN	NC	NC	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
DS2_OVR CURR	DS2_PWR EN	DS3_AMBE R	VDD_IO	VSS	AVDD33	DS3_OVR CURR	DS3_GREE N	DS3_LED_ SS	DVDD12
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
US_TXM	DS1_AMBE R	DS2_LED_ SS	NC	NC	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
US_TXP	DS1_LED_ SS	DS1_GREE N	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
DVDD12	RREF_USB 2	DS2_GREE N	DS2_AMBE R	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
US_RXM	VSS	AVDD33	MODE_SE L[1]	DVDD12	DS4_OVR CURR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
US_RXP	VBUS_DS	SUSPEND	RESERVE D1	MODE_SE L[0]	VDD_IO	DS4_PWR EN	I2C_DATA	VSS	DS2_RXM
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
AVDD12	VBUS_US	VDD_EFUS E	DS4_LED_ SS	RREF_SS	VSS	DS2_TXM	DS2_TXP	DS4_GREE N	AVDD12
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
VSS	AVDD12	VSS	DS4_AMBE R	US_PWRE N	I2C_CLK	DS1_PWR EN	DS1_OVR CURR	VSS	NC
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
NC	NC	DVDD12	NC	NC	US_OVRC URR	NC	NC	DVDD12	NC

Figure 13. HX3 100-Ball BGA Pinout for CYUSB3314, CYUSB332x

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
DS3_PWR EN	DS4_DM	DS4_DP	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
DS2_OVR CURR	DS2_PWR EN	DS3_AMB ER	VDD_IO	VSS	AVDD33	DS3_OVR CURR	DS3_GRE EN	DS3_LED _SS	DVDD12
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
US_TXM	DS1_AMB ER	DS2_LED _SS	DS3_DP	DS3_DM	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
US_TXP	DS1_LED _SS	DS1_GRE EN	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
DVDD12	RREF_US B2	DS2_GRE EN	DS2_AMB ER	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
US_RXM	VSS	AVDD33	MODE_SE L[1]	DVDD12	DS4_OVR CURR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
US_RXP	VBUS_DS	SUSPEND	RESERVE D1	MODE_SE L[0]	VDD_IO	DS4_PWR EN	I2C_DATA	VSS	DS2_RXM
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
AVDD12	VBUS_US	VDD_EFU SE	DS4_LED _SS	RREF_SS	VSS	DS2_TXM	DS2_TXP	DS4_GRE EN	AVDD12
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
VSS	AVDD12	VSS	DS4_AMB ER	US_PWR EN	I2C_CLK	DS1_PWR EN	DS1_OVR CURR	VSS	DS3_RXM
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
DS4_TXP	DS4_TXM	DVDD12	DS4_RXP	DS4_RXM	US_OVRC URR	DS3_TXP	DS3_TXM	DVDD12	DS3_RXP

Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314				
	CYUSB3324				
	CYUSB3326				
	CYUSB3328				
US Port					
US_RXP	I	14	G1	SuperSpeed receive plus	
US_RXM	I	13	F1	SuperSpeed receive minus	
US_TXP	O	11	D1	SuperSpeed transmit plus	
US_TXM	O	10	C1	SuperSpeed transmit minus	
US_DP	I/O	71	A9	USB 2.0 data plus	
US_DM	I/O	72	A8	USB 2.0 data minus	
US_OVRCURR	I	39	K6	CYUSB3324/3328: Overcurrent detect input for US port in ACA-Dock mode. If ACA-Dock mode is disabled using Configuration Options on page 24 , this pin must be pulled HIGH using a 10 kΩ to VDD_IO. Other part numbers: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.	
US_PWREN ^[5]	I/O	31	J5	CYUSB3324/3328: VBUS power enable output for US port in ACA-Dock mode. If ACA-Dock mode is disabled using Configuration Options on page 24 , this pin can be left floating if Pin-Strap is not enabled. Other part numbers: This pin can be left floating if Pin-Strap (Pin# 63) is not enabled.	
PWR_SW_POL ^[6]				This pin is called PWR_SW_POL in pin-strap configuration mode.	
DS1 Port					
DS1_RXP	I	61	D10	SuperSpeed receive plus	
DS1_RXM	I	60	C10	SuperSpeed receive minus	
DS1_TXP	O	57	F8	SuperSpeed transmit plus	
DS1_TXM	O	58	E8	SuperSpeed transmit minus	
DS1_DP	I/O	74	C7	USB 2.0 data plus	
DS1_DM	I/O	73	C8	USB 2.0 data minus	
DS1_OVRCURR	I	42	J8	Overcurrent detect input for DS1 port	
DS1_PWREN ^[5]	I/O	38	J7	VBUS power enable output for DS1 port. When the port is disabled, this pin is in tristate.	
DS1_CDP_EN ^[6]				This pin is called DS1_CDP_EN in pin-strap configuration mode.	
DS1_AMBER ^[5]	I/O	2	C2	LED_AMBER output for DS1 port	
ACA_DOCK ^[6]				This pin is called ACA-DOCK in pin-strap configuration mode.	
DS1_GREEN ^[5]	I/O	3	D3	CYUSB3312/3314/3324: LED_GREEN output for DS1 port	
DS1_VBUSEN_SL ^[5]				CYUSB3326/3328: VBUS power enable output for SS port 1	
PORT_DISABLE[0] ^[6]				This pin is called PORT_DISABLE[0] in pin-strap configuration mode.	
DS1_LED_SS ^[5]	I/O	4	D2	LED_SS output for DS1 port	
PORT_DISABLE[1] ^[6]				This pin is called PORT_DISABLE[1] in pin-strap configuration mode.	

Notes

5. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
6. For pin-strap configuration details, refer to [Table 6](#) on page 25.

Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X (continued)

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314				
	CYUSB3324				
	CYUSB3326				
	CYUSB3328				
DS2 Port					
DS2_RXP		I	55	F10	SuperSpeed receive plus
DS2_RXM		I	54	G10	SuperSpeed receive minus
DS2_TXP		O	51	H8	SuperSpeed transmit plus
DS2_TXM		O	52	H7	SuperSpeed transmit minus
DS2_DP		I/O	76	A6	USB 2.0 data plus
DS2_DM		I/O	77	A5	USB 2.0 data minus
DS2_OVRCURR		I	1	B1	Overcurrent detect input for DS2 port
DS2_PWREN ^[7]		I/O	86	B2	VBUS power enable output for DS2 port. When the port is disabled, this pin is in tristate.
DS2_CDP_EN ^[8]					This pin is called DS2_CDP_EN in the pin-strap configuration mode.
DS2_AMBER ^[7]		I/O	5	E4	LED_AMBER output for DS2 port
NON_REMOVABLE[0] ^[8]					This pin is called NON_REMOVABLE[0] in the pin-strap configuration mode.
DS2_GREEN ^[7]		I/O	6	E3	CYUSB3312/3314/3324: LED_GREEN output for DS2 port
DS2_VBUSEN_SL ^[7]					CYUSB3326/3328: VBUS power enable output for SS port 2
NON_REMOVABLE[1] ^[8]					This pin is called NON_REMOVABLE[1] in the pin-strap configuration mode.
DS2_LED_SS ^[7]		I/O	84	C3	LED_SS output for DS2 port
PWR_EN_SEL ^[8]					This pin is called PWR_EN_SEL in the pin-strap configuration mode.
DS3 Port					
NC	DS3_RXP	I	45	K10	SuperSpeed receive plus
NC	DS3_RXM	I	46	J10	SuperSpeed receive minus
NC	DS3_TXP	O	48	K7	SuperSpeed transmit plus
NC	DS3_TXM	O	49	K8	SuperSpeed transmit minus
NC	DS3_DP	I/O	79	C4	USB 2.0 data plus
NC	DS3_DM	I/O	78	C5	USB 2.0 data minus
DS3_OVRCURR		I	65	B7	CYUSB3314/3324/3326/3328: Overcurrent detect input for DS3 port CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
DS3_PWREN ^[7]		I/O	87	A1	VBUS power enable output for DS3 port. When the port is disabled, this pin is in tristate.
DS3_CDP_EN ^[8]					This pin is called DS3_CDP_EN in the pin-strap configuration mode.
DS3_AMBER ^[7]		I/O	85	B3	LED_AMBER output for DS3 port
VID_SEL[2] ^[8]					This pin is called VID_SEL[2] in the pin-strap configuration mode.

Notes

7. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
8. For pin-strap configuration details, refer to [Table 6](#) on page 25.

Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X (continued)

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314				
	CYUSB3324				
	CYUSB3326				
	CYUSB3328				
SUSPEND		I/O	25	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and Ground					
VDD_EFUSE		PWR	24	H3	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V
AVDD12		PWR	15, 21, 44, 56, 62, 67	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND		PWR	50	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12		PWR	8, 12, 18, 33, 47, 53, 59, 83	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS_US		PWR	22	H2	CYUSB3324/3328: Connect the VBUS_US pin to the local 5 V supply. If ACA-Dock mode is disabled using Configuration Options on page 24 , this pin must be connected to VBUS from US port. Other part numbers: This pin must be connected to VBUS from US port.
VBUS_DS		PWR	23	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	9, 70, 75, 80	A4, A7, B6, F3	3.3 V analog supply
VDD_IO		PWR	34, 66, 88	B4, E7, G6	3.3 V I/O supply
USB Precision Resistors					
RREF_USB2		A	7	E2	Connect pin to a precision resistor (6.04 k Ω $\pm$ 1%) to generate a current reference for USB 2.0 PHY.
RREF_SS		A	32	H5	Connect pin to a precision resistor (200 Ω $\pm$ 1%) for SS PHY termination impedance calibration.

System Interfaces

Upstream Port (US)

This port is compliant with the USB 3.0 specification and includes an integrated 1.5 k Ω pull-up and termination resistors. It also supports ACA-Dock to enable charging an OTG host connected on the US port.

Downstream Ports (DS1, 2, 3, 4)

DS ports are compliant with the USB 3.0 specification and integrate 15 k Ω pull-down and termination resistors. Ports can be disabled or enabled, and can be set to removable or non-removable options. BC v1.2 charging is enabled by default and can be disabled on each DS port using the configuration options (see [Configuration Options](#)).

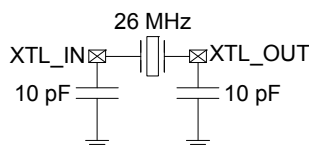
Communication Interfaces (I²C)

The interface follows the Inter-IC Bus specification, version 3.0, with support for the standard mode (100 kHz) and the fast mode (400 kHz) frequencies. HX3 supports I²C in the slave and master modes. The I²C interface supports the multi-master mode of operation. Both the SCL and SDA signals require external pull-up resistors based on the specification. VDD_IO for HX3 is 3.3 V and it is expected that the I²C pull-up resistors will be connected to the same supply.

Oscillator

HX3 requires an external crystal with a frequency of 26 MHz and an accuracy of ± 150 ppm in parallel resonant, fundamental mode. The crystal drive circuit is capable of a low-power drive level (<200 μ W). The crystal connection to the XTL_OUT and XTL_IN pins is shown in [Figure 14](#).

Figure 14. Crystal Connection



GPIOs

HX3 GPIOs are used for overcurrent sensing, controlling external power switches, and driving LEDs. These pins can sink up to 4 mA current each. GPIOs also enable pin-straps for input configuration. Refer to [Table 6](#) for more details.

Power Control

The PWR_EN[1-4] and OV_CURR[1-4] pins interface HX3 to external power switches. These pins are used to control power switches for DS port power and monitor overcurrent conditions. The power switch polarity and the power control mode (individual and ganged) can be changed using the configuration options.

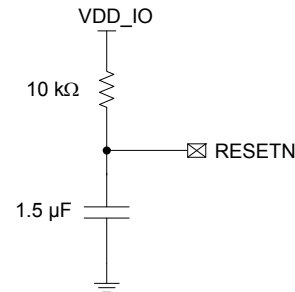
Reset

HX3 operates with two external power supplies, 3.3 V and 1.2 V. There is no power sequencing requirement between these two supplies. However, the RESETN pin should be held LOW until both these supplies become stable.

The RESETN pin can be tied to VDD_IO through an external resistor and to ground (GND) through an external capacitor (minimum 5 ms time constant), as shown in [Figure 15](#). This creates a clean reset signal for power-on reset (POR).

HX3 does not support internal brown-out detection. If the system requires this feature, an external reset should be provided on the RESETN pin when supplies are below their valid operating ranges.

Figure 15. Reset Connection



Configuration Mode Select

Configuration options are selected through the MODE_SEL pins and the pin-strap enable pin (PIN_STRAP). After power-up, these pins are sampled by an on-chip bootloader to determine the configuration options (see [Table 5](#)).

Table 5. HX3 Boot Sequence

MODE_SEL[1]	MODE_SEL[0]	HX3 Configuration Modes
0	0	Reserved. Do not use this mode.
1	1	Internal ROM configuration
0	1	I ² C Master, read configuration from I ² C EEPROM*
1	0	I ² C Slave, configure from an external I ² C Master

* Download Cypress-provided firmware from www.cypress.com/hx3.

Configuration Options

HX3 can be configured by using one of the following:

- eFuse (one-time programmable memory)
- Pin-Strap (read configuration from dedicated pins at power on)
- External I²C slave such as an EEPROM
- External I²C master

The I²C master/slave configuration overrides the pin-strap configuration. Pin-straps override the eFuse configuration, and the eFuse configuration overrides the internal ROM configuration.

eFuse Configuration

HX3 contains eFuses, which are OTP elements on the chip that can be electrically blown. The eFuses are read by the bootloader to determine the customer-specific configurations. eFuse programming is supported only at factory and distributor locations where programming conditions can be controlled. eFuse programming is supported under the following conditions:

Table 7. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
23	7:6	HS_AMPLITUDE_DS4	b'00	HS driver amplitude control; HS driver current: +0% to +7.5% b'00: Default b'01: +2.5% b'10: +5% b'11: +7.5%
	5:4	HS_AMPLITUDE_DS3	b'00	
	3:2	HS_AMPLITUDE_DS2	b'00	
	1:0	HS_AMPLITUDE_DS2	b'00	
24	7:6	HS_AMPLITUDE_US	b'00	HS driver slope control for all ports b'0000: +15% b'0001: +5% b'0100: Default b'0101: -5% b'1111: -7.5%
	5:2	HS_SLOPE	b'0100	
	1:0	HS_TX_VREF	b'10	
25	7:3	HS_PREEMP_EN[4:0]	b'00000	HS driver pre-emphasis enable – for ports DS4, DS3, DS2, DS1, and US 0: pre-emphasis is disabled 1: pre-emphasis is enabled HS driver pre-emphasis depth 0: +10% 1: +20%
	2	HS_PREEMP_DEPTH_DS4 ^[17]	0	
	1	HS_PREEMP_DEPTH_DS3 ^[17]	0	
	0	HS_PREEMP_DEPTH_DS2 ^[17]	0	
	7	HS_PREEMP_DEPTH_DS1 ^[17]	0	
26	6	HS_PREEMP_DEPTH_US ^[17]	0	Reserved
	5	Reserved	1	
	4:1	PCS_TX_DEEMPH_DS4	0x6	
	0	Reserved	0	
	7:4	PCS_TX_DEEMPH_DS3	0x6	
27	3:0	PCS_TX_DEEMPH_DS2	0x6	USB 3.0 Tx driver de-emphasis value 0x3: -2.75 dB 0x6: -3.4 dB (Default) 0x9: -4.0 dB
	7:4	PCS_TX_DEEMPH_DS1	0x6	
28	3:0	PCS_TX_DEEMPH_US	0x6	Reserved
	7	Reserved	0	
29	6	Reserved	1	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
	5:0	PCS_TX_SWING_FULL_DS4	0x29	
30	7:6	Reserved	0	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
	5:0	PCS_TX_SWING_FULL_DS3	0x29	

Note

17. HS_PREEMP_DEPTH is valid only when corresponding HS_PREEMP_EN is set for that port.

Table 7. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
51 + X	7:0	bString: Product	'C', 0, 'Y', 0, '-', 0, 'H', 0, 'X', 0, '3', 0, '-', 0, 'H', 0, 'U', 0, 'B', 0	Product string: UNICODE UTF-16LE per USB 2.0 specification: "CY-HX3 HUB"
49 + X + Y	7:0	bLength: Serial Number (Z)	22	Serial number string length ("bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number" should be less than or equal to 152 bytes). Z ≤ 66.
50 + X + Y	7:0	DescType	3	String descriptor type (constant value)
51 + X + Y	7:0	bString: Serial Number	'1', 0, '2', 0, '3', 0, '4', 0, '5', 0, '6', 0, '7', 0, '8', 0, '9', 0, 'A', 0	Serial number string: UNICODE UTF-16LE per USB 2.0 specification: "123456789A"

EMI

HX3 meets the EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. HX3 tolerates EMI conducted by aggressors outlined by the above specifications and continues to function as expected.

ESD

HX3 has a built-in ESD protection on all pins. The ESD protection level provided on these ports is 2.2 kV Human Body Model (HBM) based on the JESD22-A114 specification.

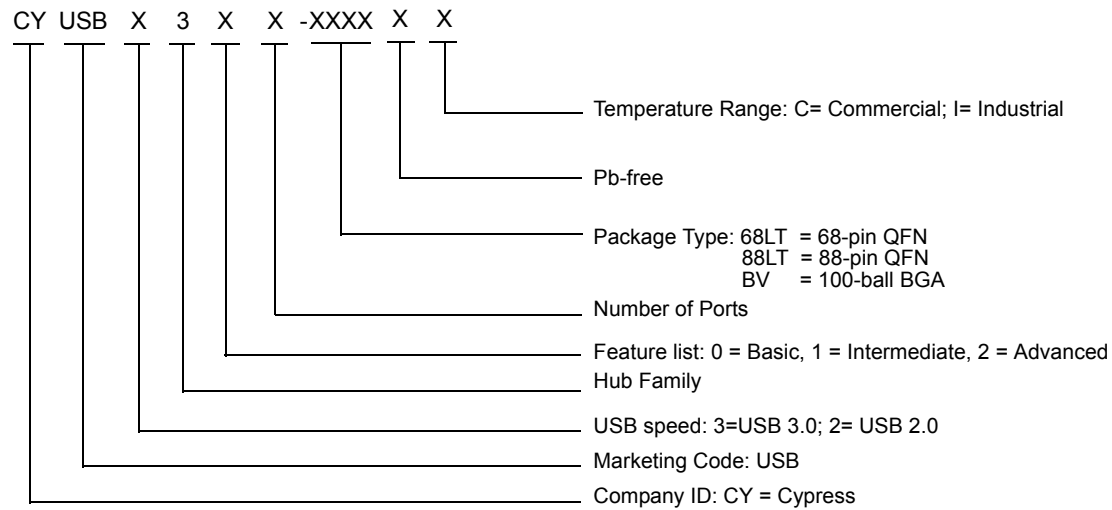
Ordering Information

Table 11 lists HX3's ordering information. The table contains only the part numbers that are currently available for order. Additional part numbers for industrial temperature range can be made available on request. For more information, visit the Cypress [website](#) or contact the local sales representative.

Table 11. Ordering Information

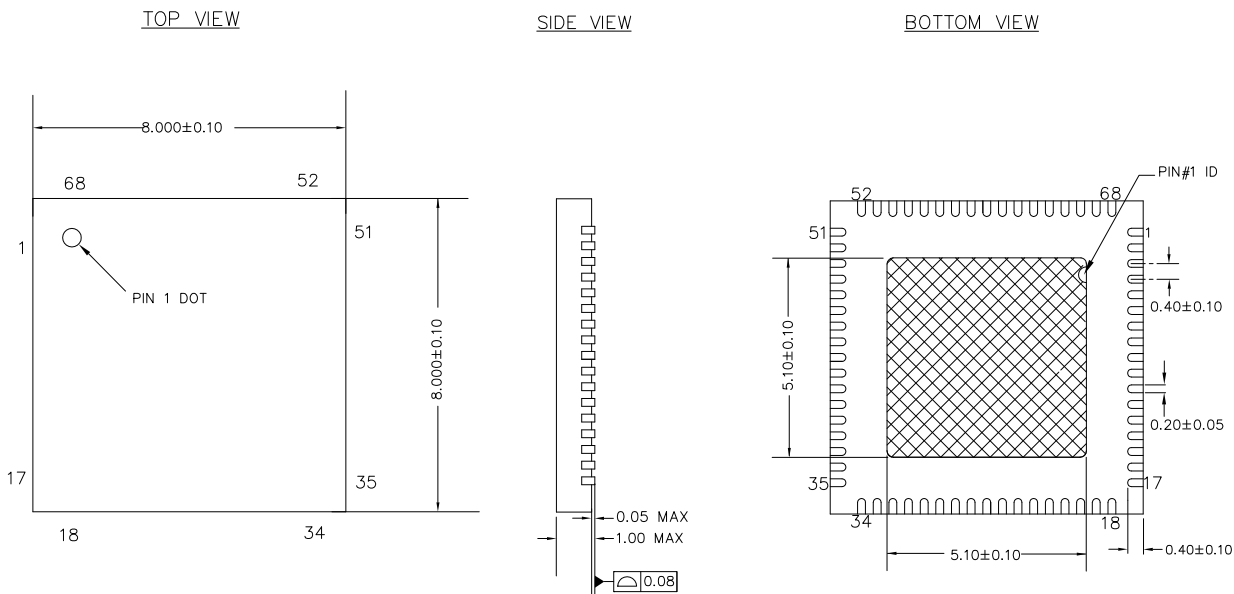
Serial No.	Ordering Part Number	Number of DS Ports	Number of Shared Link Ports	Ghost Charge	ACA-Dock	Temperature	Package
1.	CYUSB3302-68LTXC	2 (USB 3.0)	0	Yes	No	0-70 °C	68-QFN
2.	CYUSB3302-68LTXI	2 (USB 3.0)	0	Yes	No	-40-85 °C	68-QFN
3.	CYUSB3304-68LTXC	4 (USB 3.0)	0	Yes	No	0-70 °C	68-QFN
4.	CYUSB3304-68LTXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	68-QFN
5.	CYUSB3312-88LTXC	2 (USB 3.0)	0	Yes	No	0-70 °C	88-QFN
6.	CYUSB3312-88LTXI	2 (USB 3.0)	0	Yes	No	-40-85 °C	88-QFN
7.	CYUSB3314-88LTXC	4 (USB 3.0)	0	Yes	No	0-70 °C	88-QFN
8.	CYUSB3314-88LTXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	88-QFN
9.	CYUSB3324-88LTXC	4 (USB 3.0)	0	Yes	Yes	0-70 °C	88-QFN
10.	CYUSB3324-88LTXI	4 (USB 3.0)	0	Yes	Yes	-40-85 °C	88-QFN
11.	CYUSB3326-88LTXC	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	0-70 °C	88-QFN
12.	CYUSB3326-88LTXI	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	-40-85 °C	88-QFN
13.	CYUSB3328-88LTXC	8 (4 SS, 4 USB 2.0)	4	Yes	Yes	0-70 °C	88-QFN
14.	CYUSB3328-88LTXI	8 (4 SS, 4 USB 2.0)	4	Yes	Yes	-40-85 °C	88-QFN
15.	CYUSB3302-BVXC	2 (USB 3.0)	0	Yes	No	0-70 °C	100-BGA
16.	CYUSB3302-BVXI	2 (USB 3.0)	0	Yes	No	-40-85 °C	100-BGA
17.	CYUSB3304-BVXC	4 (USB 3.0)	0	Yes	No	0-70 °C	100-BGA
18.	CYUSB3304-BVXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	100-BGA
19.	CYUSB3312-BVXC	2 (USB 3.0)	0	Yes	No	0-70 °C	100-BGA
20.	CYUSB3312-BVXI	2 (USB 3.0)	0	Yes	No	-40-85 °C	100-BGA
21.	CYUSB3314-BVXC	4 (USB 3.0)	0	Yes	No	0-70 °C	100-BGA
22.	CYUSB3314-BVXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	100-BGA
23.	CYUSB3324-BVXC	4 (USB 3.0)	0	Yes	Yes	0-70 °C	100-BGA
24.	CYUSB3324-BVXI	4 (USB 3.0)	0	Yes	Yes	-40-85 °C	100-BGA
25.	CYUSB3326-BVXC	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	0-70 °C	100-BGA
26.	CYUSB3326-BVXI	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	-40-85 °C	100-BGA
27.	CYUSB3328-BVXC	8 (4 SS, 4 USB 2.0)	4	Yes	Yes	0-70 °C	100-BGA
28.	CYUSB2302-68LTXI	2 (USB 2.0)	0	Yes	No	-40-85 °C	68-QFN
29.	CYUSB2304-68LTXI	4 (USB 2.0)	0	Yes	No	-40-85 °C	68-QFN

Ordering Code Definitions



Package Diagrams

Figure 18. 68-pin QFN (8 × 8 × 1.0 mm) LT68B 5.1 × 5.1 mm EPAD (Sawn) Package Outline

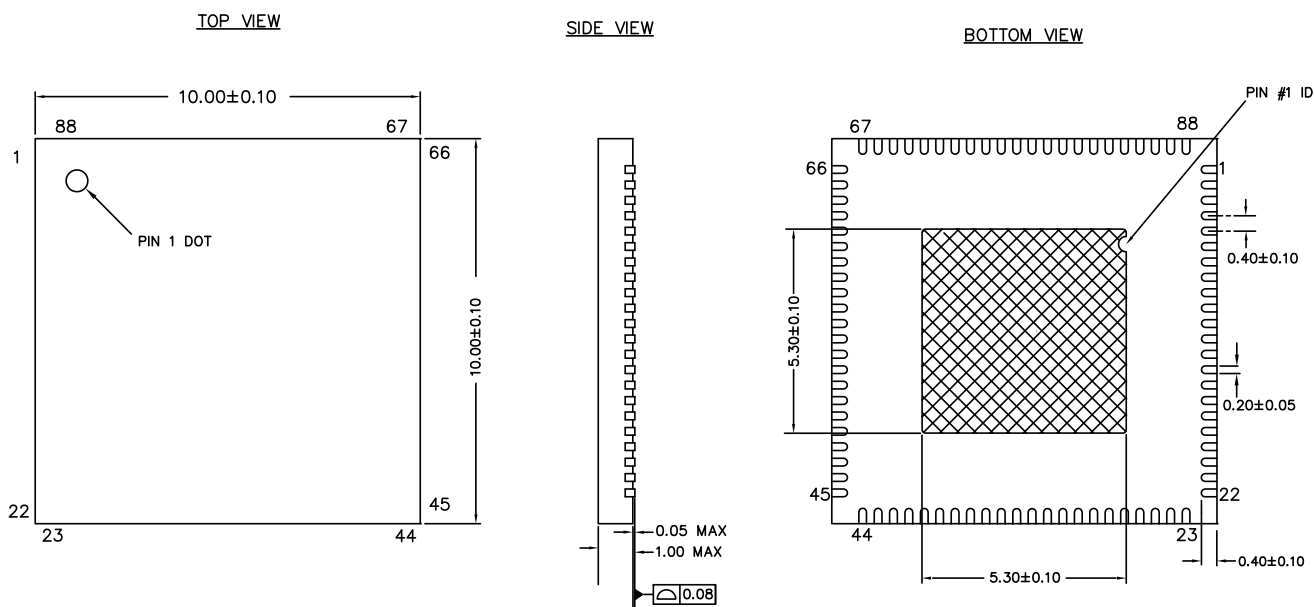


NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC#: MO-220
3. ALL DIMENSIONS ARE IN MILLIMETERS

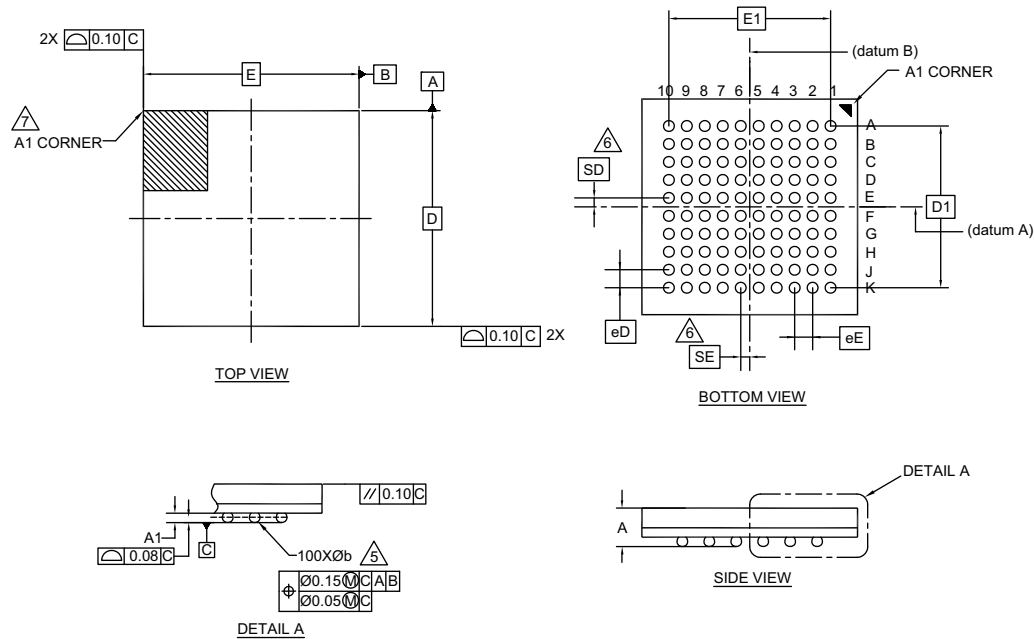
001-78925 *B

Figure 19. 88-pin QFN (10 × 10 × 1.0 mm) LT88B 5.3 × 5.3 EPAD (Sawn) Package Outline



001-76569 *B

Figure 20. 100-Ball BGA (6.0 × 6.0 × 1.0 mm) BZ100 Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	6.00 BSC		
E	6.00 BSC		
D1	4.50 BSC		
E1	4.50 BSC		
MD	10		
ME	10		
N	100		
Ø b	0.25	0.30	0.35
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.25 BSC		
SE	0.25 BSC		

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
- JEDEC SPECIFICATION NO. REF. : MO-195C.

51-85209 *F

Silicon Revision History

This datasheet is applicable for the USB-IF certified (TID# 330000060) HX3 Rev. *D and Rev. *C Silicon.

Rev. *D: This Silicon revision improves the yield of HX3, and is drop-in compatible for all the part numbers. There is no need to change the board design or layout to use the HX3 Rev. *D Silicon. Products are completely compatible with the HX3 Rev. *C Silicon.

Rev. *C: This Silicon revision fixes the errata applicable to the Rev. *A Silicon.

The following table defines the changes between Rev. *A, Rev. *C, and Rev. *D Silicon.

No.	Items	Part Numbers	Rev. *A	Rev. *C	Rev. *D
1	USB-IF Compliance	All	Requires firmware on external EEPROM	No external EEPROM required	No external EEPROM required
2	FS-only hub or host connected to HX3 Upstream Port	All	Not supported	Supported	Supported
3	Suspend Power	All	90 mW	37.8 mW	37.8 mW

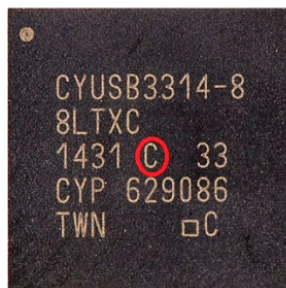
Method of Identification

Markings on row 3 of the HX3 package differentiate Rev. *D Silicon from Rev. *C Silicon and Rev. *A Silicon as indicated in the example below. Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

HX3 REV *A SILICON



HX3 REV *C SILICON



HX3 REV *D SILICON

