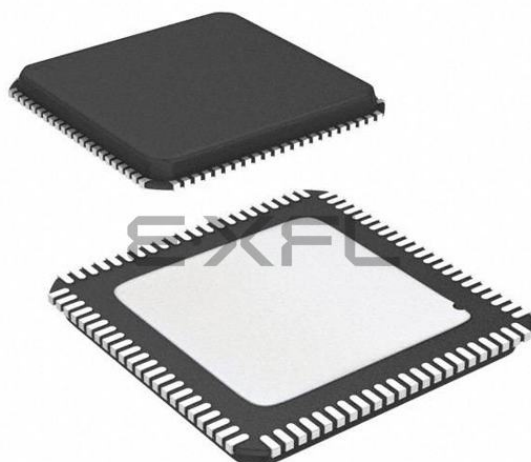




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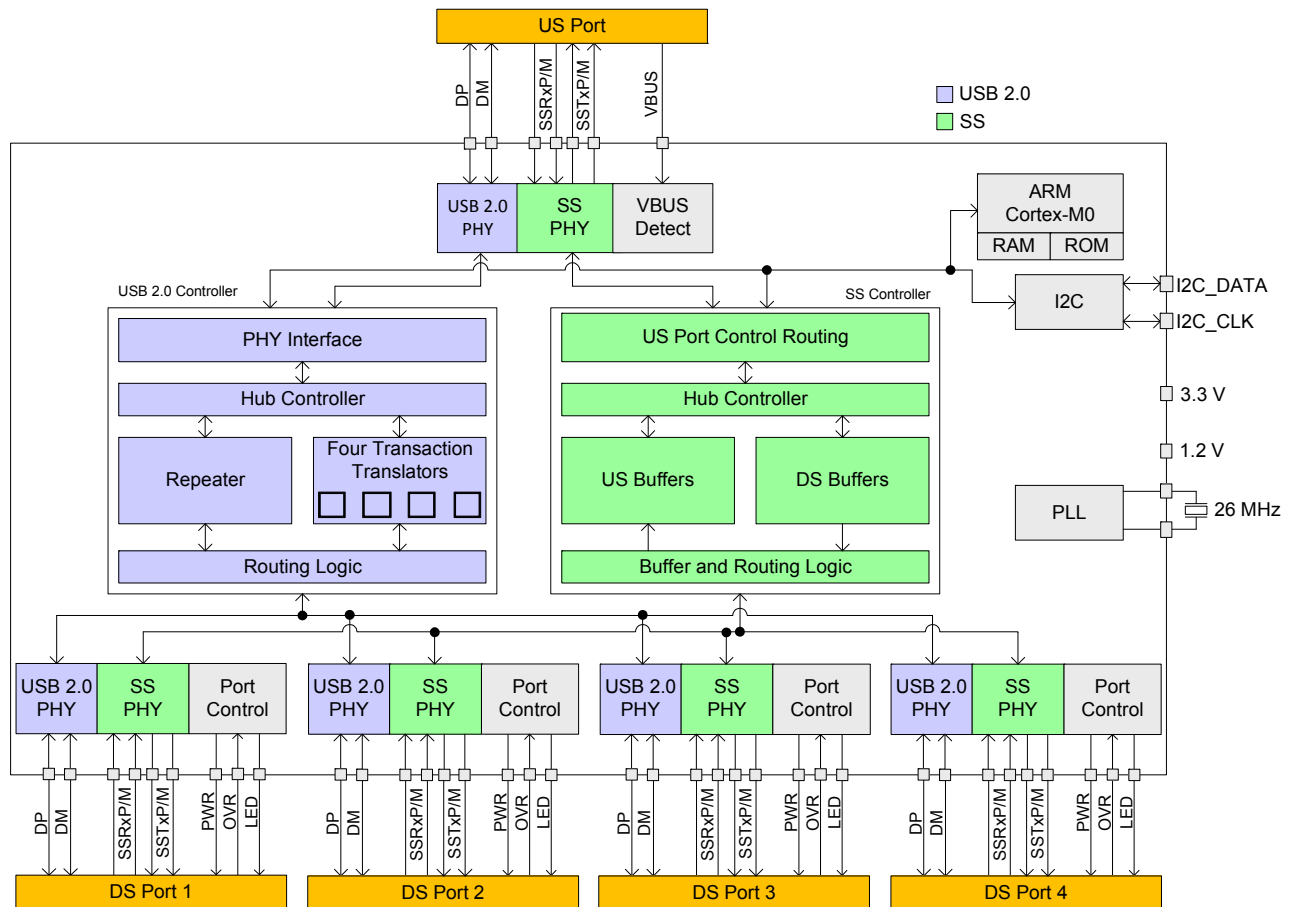
What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details

Product Status	Active
Applications	USB 3.0 Hub Controller
Core Processor	ARM® Cortex®-M0
Program Memory Type	ROM (32kB)
Controller Series	CYUSB
RAM Size	16K x 8
Interface	I ² C
Number of I/O	10
Voltage - Supply	1.14V ~ 1.26V, 2.5V ~ 2.7V, 3V ~ 3.6V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad
Supplier Device Package	88-QFN (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3314-88ltxit

Block Diagram

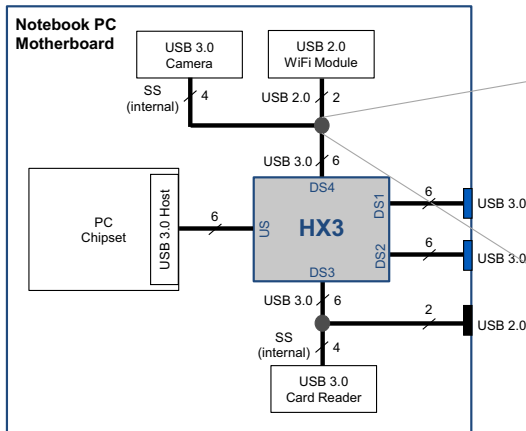


Product Features

Shared Link

Figure 1. Application of Shared Link in a Notebook

Example: Shared Link Provides Six USB Ports in a Notebook

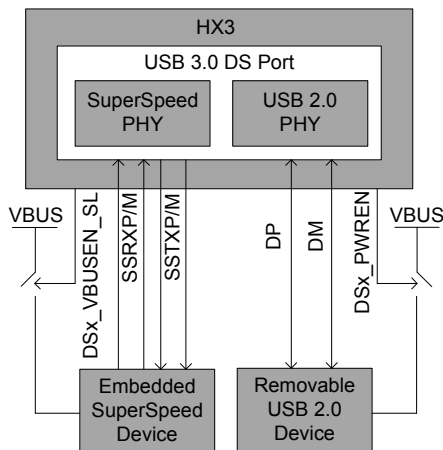


USB 3.0 Port Split Into SS Port and Standard USB 2.0 Port

Shared Link is a Cypress-proprietary feature that enables a USB 3.0 port to be split into an embedded SS port and a standard USB 2.0 port. Shared Link enables a maximum of eight DS ports from a four-port USB 3.0 hub.

For example, if one of the DS ports is connected to an embedded SS device, such as a USB 3.0 camera, HX3 enables the system designer to reuse the USB 2.0 signals of that specific port to connect to a standard USB 2.0 port. Figure 1 shows how Shared Link can be used in an application.

Figure 2. DS Port VBUS Control in Shared Link



The Shared Link mode requires a separate VBUS control for the removable USB 2.0 device and the embedded SS device. Figure 2 shows the VBUS control implementation.

To ensure that the embedded SS device does not fall back to USB 2.0 operation, an external power switch is required. This switch is controlled by HX3, which generates an output signal called DSx_VBUSEN_SL. This signal controls the VBUS for the embedded device.

DSx_PWREN is another output signal generated by HX3 and controls VBUS for the removable USB 2.0 device. For example, when an overcurrent condition occurs, DSx_PWREN turns off the port power.

Ghost Charge

Ghost Charge is a Cypress-proprietary feature for charging USB devices on the DS port when the US port is not connected to a host. For example, in a docking station with HX3 as shown in Figure 3, when the laptop is undocked, HX3 will emulate a dedicated charging port (DCP) to provide charge to a phone connected on a DS port.

Figure 3. Ghost Charge



Charge a smartphone without docking the notebook

Figure 7. HX3 68-Pin QFN 4-Port Pinout

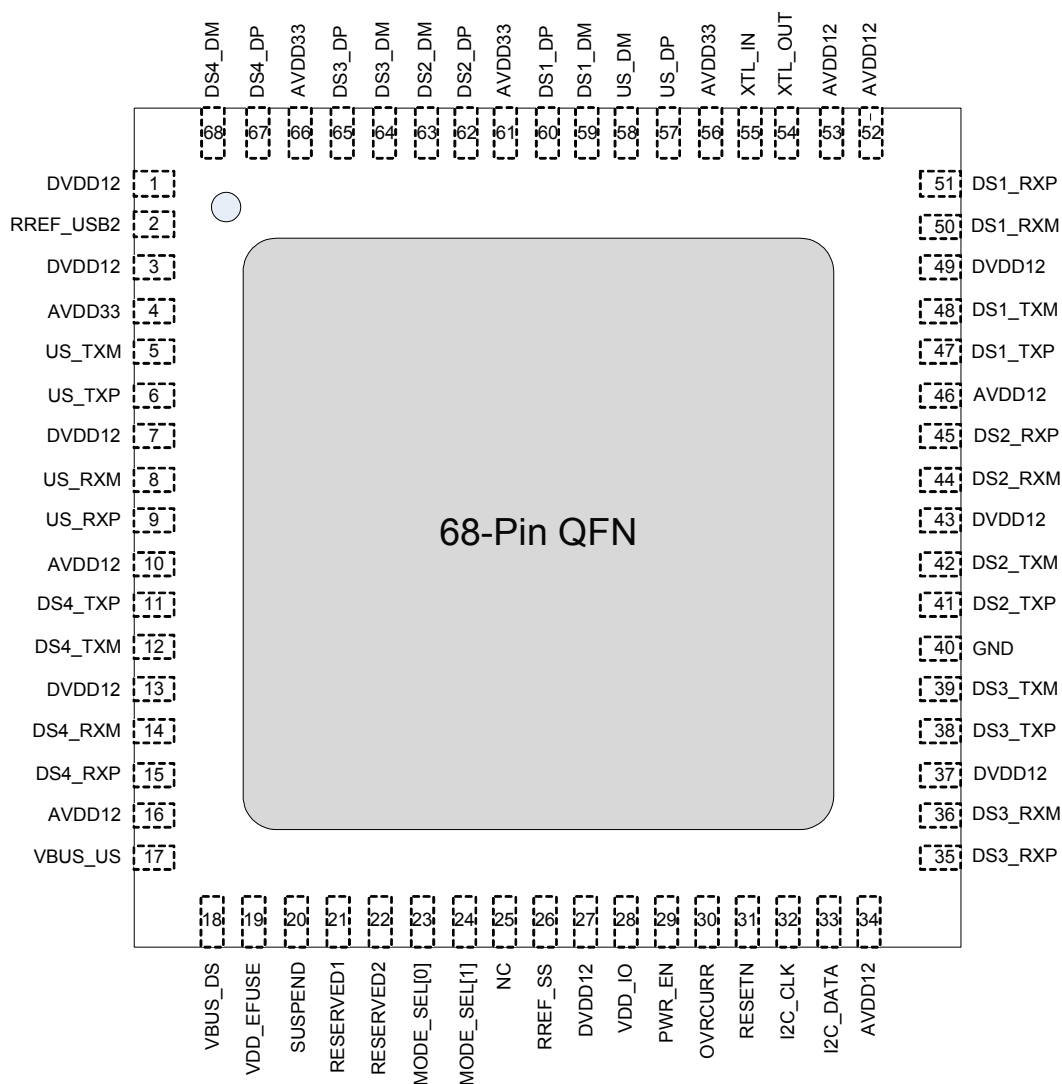


Figure 8. HX3 100-Ball BGA Pinout for CYUSB3302

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
NC	NC	NC	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
NC	NC	NC	VDD_IO	VSS	AVDD33	NC	NC	NC	DVDD12
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
US_TXM	NC	NC	NC	NC	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
US_TXP	NC	NC	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
DVDD12	RREF_US B2	NC	NC	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
US_RXM	VSS	AVDD33	MODE_SE L[1]	DVDD12	OVRCUR R	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
US_RXP	VBUS_DS	SUSPEND	RESERVE D1	MODE_SE L[0]	VDD_IO	PWR_EN	I2C_DATA	VSS	DS2_RXM
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
AVDD12	VBUS_US	VDD_EFUS SE	RESERVE D2	RREF_SS	VSS	DS2_TXM	DS2_TXP	NC	AVDD12
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
VSS	AVDD12	VSS	GPIO	NC	I2C_CLK	NC	NC	VSS	NC
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
NC	NC	DVDD12	NC	NC	NC	NC	NC	DVDD12	NC

Figure 9. HX3 100-Ball BGA Pinout for CYUSB3304

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
NC	DS4_DM	DS4_DP	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
NC	NC	NC	VDD_IO	VSS	AVDD33	NC	NC	NC	DVDD12
C1	C2	C3	C4	C5	C6	C7	C8	C9	10
US_TXM	NC	NC	DS3_DP	DS3_DM	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
US_TXP	NC	NC	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
DVDD12	RREF_US B2	NC	NC	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
US_RXM	VSS	AVDD33	MODE_SE L[1]	DVDD12	OVRCUR R	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
US_RXP	VBUS_DS	SUSPEND	RESERVE D1	MODE_SE L[0]	VDD_IO	PWR_EN	I2C_DATA	VSS	DS2_RXM
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
AVDD12	VBUS_US	VDD_EFUS SE	RESERVE D2	RREF_SS	VSS	DS2_TXM	DS2_TXP	NC	AVDD12
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
VSS	AVDD12	VSS	GPIO	NC	I2C_CLK	NC	NC	VSS	DS3_RXM
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
DS4_TXP	DS4_TXM	DVDD12	DS4_RXP	DS4_RXM	NC	DS3_TXP	DS3_TXM	DVDD12	DS3_RXP

Table 2. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB3302 and CYUSB3304

Pin Name		Type	68-QFN Pin#	100-BGA Ball #	Description
CYUSB3302	CYUSB3304				
US Port					
US_RXP		I	9	G1	SuperSpeed receive plus
US_RXM		I	8	F1	SuperSpeed receive minus
US_TXP		O	6	D1	SuperSpeed transmit plus
US_TXM		O	5	C1	SuperSpeed transmit minus
US_DP		I/O	57	A9	USB 2.0 data plus
US_DM		I/O	58	A8	USB 2.0 data minus
DS1 Port					
DS1_RXP		I	51	D10	SuperSpeed receive plus
DS1_RXM		I	50	C10	SuperSpeed receive minus
DS1_TXP		O	47	F8	SuperSpeed transmit plus
DS1_TXM		O	48	E8	SuperSpeed transmit minus
DS1_DP		I/O	60	C7	USB 2.0 data plus
DS1_DM		I/O	59	C8	USB 2.0 data minus
DS2 Port					
DS2_RXP		I	45	F10	SuperSpeed receive plus
DS2_RXM		I	44	G10	SuperSpeed receive minus
DS2_TXP		O	41	H8	SuperSpeed transmit plus
DS2_TXM		O	42	H7	SuperSpeed transmit minus
DS2_DP		I/O	62	A6	USB 2.0 data plus
DS2_DM		I/O	63	A5	USB 2.0 data minus
DS3 Port					
NC	DS3_RXP	I	35	K10	SuperSpeed receive plus
NC	DS3_RXM	I	36	J10	SuperSpeed receive minus
NC	DS3_TXP	O	38	K7	SuperSpeed transmit plus
NC	DS3_TXM	O	39	K8	SuperSpeed transmit minus
NC	DS3_DP	I/O	65	C4	USB 2.0 data plus
NC	DS3_DM	I/O	64	C5	USB 2.0 data minus
DS4 Port					
NC	DS4_RXP	I	15	K4	SuperSpeed receive plus
NC	DS4_RXM	I	14	K5	SuperSpeed receive minus
NC	DS4_TXP	O	11	K1	SuperSpeed transmit plus
NC	DS4_TXM	O	12	K2	SuperSpeed transmit minus
NC	DS4_DP	I/O	67	A3	USB 2.0 data plus
NC	DS4_DM	I/O	68	A2	USB 2.0 data minus
OVRCURR		I	30	F6	Ganged overcurrent input
PWR_EN		I/O	29	G7	Ganged power enable output
NC		I/O	25	NA	NC

Table 2. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB3302 and CYUSB3304 (continued)

Pin Name		Type	68-QFN Pin#	100-BGA Ball #	Description
CYUSB3302	CYUSB3304				
RESERVED1		I/O	21	G4	This pin must be pulled HIGH using a 10 k Ω to VDD_IO.
RESERVED2		I	22	H4	This pin must be pulled HIGH using a 10 k Ω to VDD_IO.
Mode Select, Clock, and Reset					
MODE_SEL[0]		I	23	G5	Device operation mode select bit 0; refer to Table 5 on page 24
MODE_SEL[1]		I	24	F4	Device operation mode select bit 1; refer to Table 5 on page 24
XTL_OUT		A	54	E6	Crystal out
XTL_IN		A	55	E5	Crystal in
RESETN		I	31	F7	Active LOW reset input
I2C_CLK		I/O	32	J6	I ² C clock
I2C_DATA		I/O	33	G8	I ² C data
SUSPEND		I/O	20	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and Ground					
VDD_EFUSE		PWR	19	H3	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V.
AVDD12		PWR	10, 16, 34, 46, 52, 53	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND		PWR	40	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12		PWR	1, 3, 7, 13, 27, 37, 43, 49,	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS_US		PWR	17	H2	This pin must be connected to VBUS from US port
VBUS_DS		PWR	18	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	4, 56, 61, 66	A4, A7, B6, F3	3.3 V analog supply
VDD_IO		PWR	28	B4, E7, G6	3.3 V I/O supply
USB Precision Resistors					
RREF_USB2		A	2	E2	Connect pin to a precision resistor (6.04 k Ω $\pm$ 1%) to generate a current reference for USB 2.0 PHY.
RREF_SS		A	26	H5	Connect pin to a precision resistor (200 Ω $\pm$ 1%) for SS PHY termination impedance calibration.

Note

4. These pins are Do Not Use (DNU); they must be left floating.

Table 3. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB2302 and CYUSB2304

Pin Name		Type	68-QFN Pin#	100-BGA Ball #	Description
CYUSB2302	CYUSB2304				
US Port					
NC		I	9	G1	SuperSpeed receive plus
NC		I	8	F1	SuperSpeed receive minus
NC		O	6	D1	SuperSpeed transmit plus
NC		O	5	C1	SuperSpeed transmit minus
US_DP		I/O	57	A9	USB 2.0 data plus
US_DM		I/O	58	A8	USB 2.0 data minus
DS1 Port					
NC		I	51	D10	SuperSpeed receive plus
NC		I	50	C10	SuperSpeed receive minus
NC		O	47	F8	SuperSpeed transmit plus
NC		O	48	E8	SuperSpeed transmit minus
DS1_DP		I/O	60	C7	USB 2.0 data plus
DS1_DM		I/O	59	C8	USB 2.0 data minus
DS2 Port					
NC		I	45	F10	SuperSpeed receive plus
NC		I	44	G10	SuperSpeed receive minus
NC		O	41	H8	SuperSpeed transmit plus
NC		O	42	H7	SuperSpeed transmit minus
DS2_DP		I/O	62	A6	USB 2.0 data plus
DS2_DM		I/O	63	A5	USB 2.0 data minus
DS3 Port					
NC	NC	I	35	K10	SuperSpeed receive plus
NC	NC	I	36	J10	SuperSpeed receive minus
NC	NC	O	38	K7	SuperSpeed transmit plus
NC	NC	O	39	K8	SuperSpeed transmit minus
NC	DS3_DP	I/O	65	C4	USB 2.0 data plus
NC	DS3_DM	I/O	64	C5	USB 2.0 data minus
DS4 Port					
NC	NC	I	15	K4	SuperSpeed receive plus
NC	NC	I	14	K5	SuperSpeed receive minus
NC	NC	O	11	K1	SuperSpeed transmit plus
NC	NC	O	12	K2	SuperSpeed transmit minus
NC	DS4_DP	I/O	67	A3	USB 2.0 data plus
NC	DS4_DM	I/O	68	A2	USB 2.0 data minus
OVRCURR		I	30	F6	Ganged overcurrent input
PWR_EN		I/O	29	G7	Ganged power enable output
NC		I/O	25	NA	NC

Figure 13. HX3 100-Ball BGA Pinout for CYUSB3314, CYUSB332x

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
DS3_PWR EN	DS4_DM	DS4_DP	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
DS2_OVR CURR	DS2_PWR EN	DS3_AMB ER	VDD_IO	VSS	AVDD33	DS3_OVR CURR	DS3_GRE EN	DS3_LED _SS	DVDD12
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
US_TXM	DS1_AMB ER	DS2_LED _SS	DS3_DP	DS3_DM	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
US_TXP	DS1_LED _SS	DS1_GRE EN	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
DVDD12	RREF_US B2	DS2_GRE EN	DS2_AMB ER	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
US_RXM	VSS	AVDD33	MODE_SE L[1]	DVDD12	DS4_OVR CURR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
US_RXP	VBUS_DS	SUSPEND	RESERVE D1	MODE_SE L[0]	VDD_IO	DS4_PWR EN	I2C_DATA	VSS	DS2_RXM
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
AVDD12	VBUS_US	VDD_EFU SE	DS4_LED _SS	RREF_SS	VSS	DS2_TXM	DS2_TXP	DS4_GRE EN	AVDD12
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
VSS	AVDD12	VSS	DS4_AMB ER	US_PWR EN	I2C_CLK	DS1_PWR EN	DS1_OVR CURR	VSS	DS3_RXM
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
DS4_TXP	DS4_TXM	DVDD12	DS4_RXP	DS4_RXM	US_OVRC URR	DS3_TXP	DS3_TXM	DVDD12	DS3_RXP

Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314				
	CYUSB3324				
	CYUSB3326				
	CYUSB3328				
US Port					
US_RXP	I	14	G1	SuperSpeed receive plus	
US_RXM	I	13	F1	SuperSpeed receive minus	
US_TXP	O	11	D1	SuperSpeed transmit plus	
US_TXM	O	10	C1	SuperSpeed transmit minus	
US_DP	I/O	71	A9	USB 2.0 data plus	
US_DM	I/O	72	A8	USB 2.0 data minus	
US_OVRCURR	I	39	K6	CYUSB3324/3328: Overcurrent detect input for US port in ACA-Dock mode. If ACA-Dock mode is disabled using Configuration Options on page 24 , this pin must be pulled HIGH using a 10 kΩ to VDD_IO. Other part numbers: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.	
US_PWREN ^[5]	I/O	31	J5	CYUSB3324/3328: VBUS power enable output for US port in ACA-Dock mode. If ACA-Dock mode is disabled using Configuration Options on page 24 , this pin can be left floating if Pin-Strap is not enabled. Other part numbers: This pin can be left floating if Pin-Strap (Pin# 63) is not enabled.	
PWR_SW_POL ^[6]				This pin is called PWR_SW_POL in pin-strap configuration mode.	
DS1 Port					
DS1_RXP	I	61	D10	SuperSpeed receive plus	
DS1_RXM	I	60	C10	SuperSpeed receive minus	
DS1_TXP	O	57	F8	SuperSpeed transmit plus	
DS1_TXM	O	58	E8	SuperSpeed transmit minus	
DS1_DP	I/O	74	C7	USB 2.0 data plus	
DS1_DM	I/O	73	C8	USB 2.0 data minus	
DS1_OVRCURR	I	42	J8	Overcurrent detect input for DS1 port	
DS1_PWREN ^[5]	I/O	38	J7	VBUS power enable output for DS1 port. When the port is disabled, this pin is in tristate.	
DS1_CDP_EN ^[6]				This pin is called DS1_CDP_EN in pin-strap configuration mode.	
DS1_AMBER ^[5]	I/O	2	C2	LED_AMBER output for DS1 port	
ACA_DOCK ^[6]				This pin is called ACA-DOCK in pin-strap configuration mode.	
DS1_GREEN ^[5]	I/O	3	D3	CYUSB3312/3314/3324: LED_GREEN output for DS1 port	
DS1_VBUSEN_SL ^[5]				CYUSB3326/3328: VBUS power enable output for SS port 1	
PORT_DISABLE[0] ^[6]				This pin is called PORT_DISABLE[0] in pin-strap configuration mode.	
DS1_LED_SS ^[5]	I/O	4	D2	LED_SS output for DS1 port	
PORT_DISABLE[1] ^[6]				This pin is called PORT_DISABLE[1] in pin-strap configuration mode.	

Notes

5. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
6. For pin-strap configuration details, refer to [Table 6](#) on page 25.

Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X (continued)

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314				
	CYUSB3324				
	CYUSB3326				
	CYUSB3328				
SUSPEND		I/O	25	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and Ground					
VDD_EFUSE		PWR	24	H3	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V
AVDD12		PWR	15, 21, 44, 56, 62, 67	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND		PWR	50	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12		PWR	8, 12, 18, 33, 47, 53, 59, 83	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS_US		PWR	22	H2	CYUSB3324/3328: Connect the VBUS_US pin to the local 5 V supply. If ACA-Dock mode is disabled using Configuration Options on page 24 , this pin must be connected to VBUS from US port. Other part numbers: This pin must be connected to VBUS from US port.
VBUS_DS		PWR	23	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	9, 70, 75, 80	A4, A7, B6, F3	3.3 V analog supply
VDD_IO		PWR	34, 66, 88	B4, E7, G6	3.3 V I/O supply
USB Precision Resistors					
RREF_USB2		A	7	E2	Connect pin to a precision resistor (6.04 k Ω $\pm$ 1%) to generate a current reference for USB 2.0 PHY.
RREF_SS		A	32	H5	Connect pin to a precision resistor (200 Ω $\pm$ 1%) for SS PHY termination impedance calibration.

System Interfaces

Upstream Port (US)

This port is compliant with the USB 3.0 specification and includes an integrated 1.5 k Ω pull-up and termination resistors. It also supports ACA-Dock to enable charging an OTG host connected on the US port.

Downstream Ports (DS1, 2, 3, 4)

DS ports are compliant with the USB 3.0 specification and integrate 15 k Ω pull-down and termination resistors. Ports can be disabled or enabled, and can be set to removable or non-removable options. BC v1.2 charging is enabled by default and can be disabled on each DS port using the configuration options (see [Configuration Options](#)).

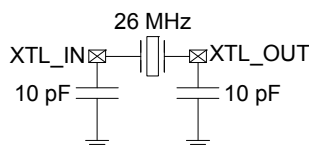
Communication Interfaces (I²C)

The interface follows the Inter-IC Bus specification, version 3.0, with support for the standard mode (100 kHz) and the fast mode (400 kHz) frequencies. HX3 supports I²C in the slave and master modes. The I²C interface supports the multi-master mode of operation. Both the SCL and SDA signals require external pull-up resistors based on the specification. VDD_IO for HX3 is 3.3 V and it is expected that the I²C pull-up resistors will be connected to the same supply.

Oscillator

HX3 requires an external crystal with a frequency of 26 MHz and an accuracy of ± 150 ppm in parallel resonant, fundamental mode. The crystal drive circuit is capable of a low-power drive level (<200 μ W). The crystal connection to the XTL_OUT and XTL_IN pins is shown in [Figure 14](#).

Figure 14. Crystal Connection



GPIOs

HX3 GPIOs are used for overcurrent sensing, controlling external power switches, and driving LEDs. These pins can sink up to 4 mA current each. GPIOs also enable pin-straps for input configuration. Refer to [Table 6](#) for more details.

Power Control

The PWR_EN[1-4] and OV_CURR[1-4] pins interface HX3 to external power switches. These pins are used to control power switches for DS port power and monitor overcurrent conditions. The power switch polarity and the power control mode (individual and ganged) can be changed using the configuration options.

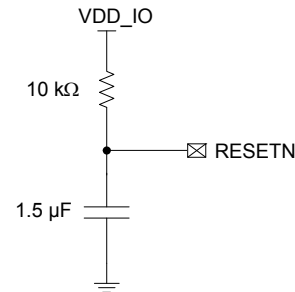
Reset

HX3 operates with two external power supplies, 3.3 V and 1.2 V. There is no power sequencing requirement between these two supplies. However, the RESETN pin should be held LOW until both these supplies become stable.

The RESETN pin can be tied to VDD_IO through an external resistor and to ground (GND) through an external capacitor (minimum 5 ms time constant), as shown in [Figure 15](#). This creates a clean reset signal for power-on reset (POR).

HX3 does not support internal brown-out detection. If the system requires this feature, an external reset should be provided on the RESETN pin when supplies are below their valid operating ranges.

Figure 15. Reset Connection



Configuration Mode Select

Configuration options are selected through the MODE_SEL pins and the pin-strap enable pin (PIN_STRAP). After power-up, these pins are sampled by an on-chip bootloader to determine the configuration options (see [Table 5](#)).

Table 5. HX3 Boot Sequence

MODE SEL[1]	MODE SEL[0]	HX3 Configuration Modes
0	0	Reserved. Do not use this mode.
1	1	Internal ROM configuration
0	1	I ² C Master, read configuration from I ² C EEPROM*
1	0	I ² C Slave, configure from an external I ² C Master

* Download Cypress-provided firmware from www.cypress.com/hx3.

Configuration Options

HX3 can be configured by using one of the following:

- eFuse (one-time programmable memory)
- Pin-Strap (read configuration from dedicated pins at power on)
- External I²C slave such as an EEPROM
- External I²C master

The I²C master/slave configuration overrides the pin-strap configuration. Pin-straps override the eFuse configuration, and the eFuse configuration overrides the internal ROM configuration.

eFuse Configuration

HX3 contains eFuses, which are OTP elements on the chip that can be electrically blown. The eFuses are read by the bootloader to determine the customer-specific configurations. eFuse programming is supported only at factory and distributor locations where programming conditions can be controlled. eFuse programming is supported under the following conditions:

Table 7. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
9	7:0	DID [7:0]	00 - 88-pin QFN, 10 - 68-pin QFN	Custom Device ID - revision - LSB
10	7:0	DID [15:8]	50	Custom Device ID - revision - MSB
11	7:0	Reserved	0	Reserved
12	7:4	SHARED_LINK_EN	b'0000	Enable Shared Link on DS port bit[7:4]=DS4, DS3, DS2, DS1 0: Shared Link not enabled 1: Shared Link enabled
	3:0	SHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a SuperSpeed port is active. bit[3:0] = DS4, DS3, DS2, DS1 0: Not active 1: Active
13	7:0	POWER_ON_TIME	0x32	Time (in 2-ms intervals) from the time the power-on sequence begins on a port until power is good on that port (bPwron2PwrGood)
14	7:4	REMOVABLE_PORTS [3:0]	b'1111	Indicates if the port is removable. bit[7:4]=DS4, DS3, DS2, DS1 0: Non-removable 1: Removable
	3:0	UHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a USB 2.0 port is active. bit[3:0]=DS4, DS3, DS2, DS1 0: Not active 1: Active
15	7	SS_LED_PIN_CONTROL	0	Port 1–4: SS LED disable 0: DS[1:4]_LED_SS are LEDs. The LED glows when the SS port is active and not in disabled state. 1: DS[1:4]_LED_SS are not LEDs
	6	GREEN_LED_PIN_CONTROL	0	Port 1–4: USB 2.0 Green LED disable 0: DS[1:4]_GREEN are LEDs 1: DS[1:4]_GREEN are not LEDs
	5	AMBER_LED_PIN_CONTROL	0	Port 1–4: USB 2.0 Amber LED disable 0: DS[1:4]_AMBER are LEDs 1: DS[1:4]_AMBER are not LEDs
	4	PORT_INDICATORS	1	Port indicators supported 0: Port indicators are not supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request has no effect. 1: Port indicators are supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request controls the indicators.
	3	COMPOUND_HUB	0	Identifies a compound device. 0: Hub is not part of a compound device. 1: Hub is part of a compound device.
	2:1	Reserved	0	Reserved
	0	GANG	0	1: Ganged power switch enable for all DS ports 0: Individual port power switch enable for each DS port

Table 7. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
16	7	SUSPEND_INDICATOR_DISABLE	0	0: Suspend indicator enabled 1: Suspend indicator disabled
	6	SS_US_DISABLE	0	Hub mode of operation (USB 3.0 or USB 2.0) 0: USB 3.0 hub and USB 2.0 hub enabled 1: USB 3.0 hub disabled and USB 2.0 hub enabled
	5	PWR_EN_POLARITY	0	Power switch control output polarity 0: Active LOW 1: Active HIGH
	4:0	PORT_POLARITY	b'00000	USB 2.0 DP and DM swapped bit[4:0]=DS4, DS3, DS2, DS1, US 1: Port polarity swapped 0: Port polarity not swapped
17	7:5	Reserved	0	Reserved
	4	BC_ENABLE	1	0: BC v1.2 disabled 1: BC v1.2 enabled
	3	ACA_DOCK	0	If this bit is set, enable ACA-Dock on the US port
	2	APPLE_XA	0	0: Max limit for Apple charging 2.1 A 1: Max limit for Apple charging 1 A
	1	Reserved	0	Reserved
	0	GHOST_CHARGE_EN	1	0: Ghost Charging disabled 1: Ghost Charging enabled
18	7:4	CDP_EN[3:0]	b'1111	Per-port charging setting bit[7:4]=DS4, DS3, DS2, DS1 0: CDP disabled 1: CDP enabled
	3:0	DCP_EN[3:0]	b'0000	Per-port charging setting bit[3:0]=DS4, DS3, DS2, DS1 0: DCP disabled 1: DCP enabled
19	7	EMBEDDED_HUB	0	If this bit is set, the US is as an embedded port and VBUS connected to VBUS_US pin is ignored.
	6	ILLEGAL_DESCRIPTOR	1	If this bit is set, the USB 2.0 hub controller will accept both 0x00 and 0x29 as valid descriptor types. If '0', only 0x29 will be accepted as a valid descriptor type.
	5	Reserved	1	Reserved
	4	OC_POLARITY	0	Overcurrent input polarity 0: Active LOW 1: Active HIGH
	3:0	OC_TIMER	b'1000	Time in milliseconds for which the overcurrent inputs will be filtered
20	7:0	Reserved	0	Reserved
21	7:4	Reserved	0	Reserved
	3	STRING_DESCRIPTOR_ENABLE ^[16]	0	0: String descriptor support is disabled 1: String descriptor support is enabled When string descriptors are not supported, the hub controller returns a non-zero index (compile-time programmable) for each string which is supported, and 0x00 for each string not supported, as indicated by this field.
	2:0	Reserved	0	Reserved
22	7:0	Reserved	0	Reserved

Note

16. When the string descriptor supports LangID, Manufacturer, Product and Serial Number, the serial number must be unique for each device.

Table 7. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
23	7:6	HS_AMPLITUDE_DS4	b'00	HS driver amplitude control; HS driver current: +0% to +7.5% b'00: Default b'01: +2.5% b'10: +5% b'11: +7.5%
	5:4	HS_AMPLITUDE_DS3	b'00	
	3:2	HS_AMPLITUDE_DS2	b'00	
	1:0	HS_AMPLITUDE_DS2	b'00	
24	7:6	HS_AMPLITUDE_US	b'00	HS driver slope control for all ports b'0000: +15% b'0001: +5% b'0100: Default b'0101: -5% b'1111: -7.5%
	5:2	HS_SLOPE	b'0100	
	1:0	HS_TX_VREF	b'10	
25	7:3	HS_PREEMP_EN[4:0]	b'00000	HS driver pre-emphasis enable – for ports DS4, DS3, DS2, DS1, and US 0: pre-emphasis is disabled 1: pre-emphasis is enabled HS driver pre-emphasis depth 0: +10% 1: +20%
	2	HS_PREEMP_DEPTH_DS4 ^[17]	0	
	1	HS_PREEMP_DEPTH_DS3 ^[17]	0	
	0	HS_PREEMP_DEPTH_DS2 ^[17]	0	
	7	HS_PREEMP_DEPTH_DS1 ^[17]	0	
26	6	HS_PREEMP_DEPTH_US ^[17]	0	Reserved
	5	Reserved	1	
	4:1	PCS_TX_DEEMPH_DS4	0x6	
	0	Reserved	0	
	7:4	PCS_TX_DEEMPH_DS3	0x6	
27	3:0	PCS_TX_DEEMPH_DS2	0x6	USB 3.0 Tx driver de-emphasis value 0x3: -2.75 dB 0x6: -3.4 dB (Default) 0x9: -4.0 dB
	7:4	PCS_TX_DEEMPH_DS1	0x6	
28	3:0	PCS_TX_DEEMPH_US	0x6	Reserved
	7	Reserved	0	
29	6	Reserved	1	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
	5:0	PCS_TX_SWING_FULL_DS4	0x29	
30	7:6	Reserved	0	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
	5:0	PCS_TX_SWING_FULL_DS3	0x29	

Note

17. HS_PREEMP_DEPTH is valid only when corresponding HS_PREEMP_EN is set for that port.

Table 7. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
31	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_DS2	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
32	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_DS1	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
33	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_US	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
34	7:0	Reserved	0	Reserved
35	7:0	UHC_PID [7:0]_LSB	0x06	USB 2.0 PID. If bD4Length ≥ 40, USB 2.0 PID will be read from this location.
36	7:0	UHC_PID [15:8]_MSB	0x65	
37–44	7:0	Reserved	0	Eight bytes reserved for future expansion
45	7:0	bLength: LangID	4	Size of LangID (defined by spec as N+2)
46	7:0	DescType	3	String descriptor type (constant value)
47	7:0	LangID - MSB	9	String language ID - MSB of wLangID
48	7:0	LangID - LSB	4	String language ID - MSB of wLangID
49	7:0	bLength: Manufacturer (X)	54	Manufacturer string length ("bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number" should be less than or equal to 152 bytes). X ≤ 66.
50	7:0	DescType	3	String descriptor type (constant value)
51	7:0	bString: Manufacturer	'2', 0, '0', 0, '1', 0, '4', 0, ' ', 0, 'C', 0, 'y', 0, 'p', 0, 'r', 0, 'e', 0, 's', 0, 's', 0, ' ', 0, 'S', 0, 'e', 0, 'm', 0, 'i', 0, 'c', 0, 'o', 0, 'n', 0, 'd', 0, 'u', 0, 'c', 0, 't', 0, 'o', 0, 'r', 0	Manufacturer string: UNICODE UTF-16LE per USB 2.0 specification: "2014 Cypress Semiconductor"
49 + X	7:0	bLength: Product (Y)	22	Product string length ("bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number" should be less than or equal to 152 bytes). Y ≤ 66.
50 + X	7:0	DescType	3	String descriptor type (constant value)

Table 7. EEPROM Map (continued)

I ² C Offset	Bits	Name	Default	Description
51 + X	7:0	bString: Product	'C', 0, 'Y', 0, '-', 0, 'H', 0, 'X', 0, '3', 0, '-', 0, 'H', 0, 'U', 0, 'B', 0	Product string: UNICODE UTF-16LE per USB 2.0 specification: "CY-HX3 HUB"
49 + X + Y	7:0	bLength: Serial Number (Z)	22	Serial number string length ("bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number" should be less than or equal to 152 bytes). Z ≤ 66.
50 + X + Y	7:0	DescType	3	String descriptor type (constant value)
51 + X + Y	7:0	bString: Serial Number	'1', 0, '2', 0, '3', 0, '4', 0, '5', 0, '6', 0, '7', 0, '8', 0, '9', 0, 'A', 0	Serial number string: UNICODE UTF-16LE per USB 2.0 specification: "123456789A"

EMI

HX3 meets the EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. HX3 tolerates EMI conducted by aggressors outlined by the above specifications and continues to function as expected.

ESD

HX3 has a built-in ESD protection on all pins. The ESD protection level provided on these ports is 2.2 kV Human Body Model (HBM) based on the JESD22-A114 specification.

Power Consumption

Table 9 provides the power consumption estimates for HX3 under different conditions. Table 10 summarizes the power consumption for various combinations of devices connected to DS ports.

For example, to calculate the HX3 power consumption for three SS devices connected to DS ports (and no device connected to one DS port), and a US port connected to a USB 3.0 host:

$$\text{Power consumption} = [a] + 2*[g] = 492.5 + 2*76 = 644 \text{ mW}$$

[a] is the active power consumption for the US port connected to a USB 3.0 host and the SS device connected to the DS port.

[g] is the incremental power consumption for an additional SS device connected to the DS port.

Table 9. Power Consumption Estimates for Various Usage Scenarios

Device Condition	Number and Speed of DS Ports Connected	Typical Consumption			Comments
		Supply Current (mA)		Power (mW)	
		1.2 V	3.3 V		
Suspend ^[18]	NA	12.0	7.1	37.8	–
Active power with USB 3.0 host ^[19]	1 SS	204.1	75.0	492.5	[a]
	1 HS	51.2	45.2	210.7	[b]
	1 FS	51.2	34.0	173.7	[c]
	1 SS + 1 HS	218.0	103.4	602.9	[d]
Active power with USB 2.0 host ^[19, 20]	1 HS	51.2	45.2	210.7	[e]
	1 FS	51.2	34.0	173.7	[f]
Incremental active power for additional DS port	SS	39.4	8.7	76.0	[g]
	HS	7.0	19.8	73.7	[h]
	FS	7.0	14.2	55.2	[i]
Active power saving per disabled DS port ^[21]	–	10.6	9.6	44.4	[j]

Table 10. Power Consumption Under Various Configurations

Configuration	Number of DS Devices Connected With Data Transfer	Typical Consumption			Comments
		Supply Current (mA)		Power (mW)	
		1.2 V	3.3 V		
USB 3.0 4-Port Hub (USB 3.0 host)	4 SS devices	322	101	720	[a] + 3*[g]
	3 SS + 1 HS devices	297	121	755	[d] + 2*[g]
	3 SS devices	283	92	644	[a] + 2*[g]
USB 3.0 4-Port Hub with one port disabled (USB 3.0 host)	3 SS devices	272	83	600	[a] + 2*[g] - [j]
	2 SS + 1 HS devices	247	103	634	[d] + [g] - [j]
Shared Link with eight DS ports	4 SS + 4 HS devices	357	189	1052	[d] + 3*([g] + [h])
USB 2.0 4-Port Hub (USB 2.0 host)	4 HS devices	72	105	432	[e] + 3*[h]
	3 HS + 1 FS devices	72	99	413	[e] + 2*[h] + [i]

Notes

18. US port in low-power state (SS in U3 and USB 2.0 in L2).

19. All four DS ports are enabled.

20. US SS disabled using configuration options. Refer to Table 7 on page 26 for I²C configuration options.

21. Power saving applicable only with a USB 3.0 host. DS ports can be disabled through configuration options. Refer to Table 6 on page 25 for pin-strapping and Table 7 on page 26 for I²C configuration options.

Ordering Information

Table 11 lists HX3's ordering information. The table contains only the part numbers that are currently available for order. Additional part numbers for industrial temperature range can be made available on request. For more information, visit the Cypress [website](#) or contact the local sales representative.

Table 11. Ordering Information

Serial No.	Ordering Part Number	Number of DS Ports	Number of Shared Link Ports	Ghost Charge	ACA-Dock	Temperature	Package
1.	CYUSB3302-68LTXC	2 (USB 3.0)	0	Yes	No	0-70 °C	68-QFN
2.	CYUSB3302-68LTXI	2 (USB 3.0)	0	Yes	No	-40-85 °C	68-QFN
3.	CYUSB3304-68LTXC	4 (USB 3.0)	0	Yes	No	0-70 °C	68-QFN
4.	CYUSB3304-68LTXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	68-QFN
5.	CYUSB3312-88LTXC	2 (USB 3.0)	0	Yes	No	0-70 °C	88-QFN
6.	CYUSB3312-88LTXI	2 (USB 3.0)	0	Yes	No	-40-85 °C	88-QFN
7.	CYUSB3314-88LTXC	4 (USB 3.0)	0	Yes	No	0-70 °C	88-QFN
8.	CYUSB3314-88LTXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	88-QFN
9.	CYUSB3324-88LTXC	4 (USB 3.0)	0	Yes	Yes	0-70 °C	88-QFN
10.	CYUSB3324-88LTXI	4 (USB 3.0)	0	Yes	Yes	-40-85 °C	88-QFN
11.	CYUSB3326-88LTXC	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	0-70 °C	88-QFN
12.	CYUSB3326-88LTXI	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	-40-85 °C	88-QFN
13.	CYUSB3328-88LTXC	8 (4 SS, 4 USB 2.0)	4	Yes	Yes	0-70 °C	88-QFN
14.	CYUSB3328-88LTXI	8 (4 SS, 4 USB 2.0)	4	Yes	Yes	-40-85 °C	88-QFN
15.	CYUSB3302-BVXC	2 (USB 3.0)	0	Yes	No	0-70 °C	100-BGA
16.	CYUSB3302-BVXI	2 (USB 3.0)	0	Yes	No	-40-85 °C	100-BGA
17.	CYUSB3304-BVXC	4 (USB 3.0)	0	Yes	No	0-70 °C	100-BGA
18.	CYUSB3304-BVXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	100-BGA
19.	CYUSB3312-BVXC	2 (USB 3.0)	0	Yes	No	0-70 °C	100-BGA
20.	CYUSB3312-BVXI	2 (USB 3.0)	0	Yes	No	-40-85 °C	100-BGA
21.	CYUSB3314-BVXC	4 (USB 3.0)	0	Yes	No	0-70 °C	100-BGA
22.	CYUSB3314-BVXI	4 (USB 3.0)	0	Yes	No	-40-85 °C	100-BGA
23.	CYUSB3324-BVXC	4 (USB 3.0)	0	Yes	Yes	0-70 °C	100-BGA
24.	CYUSB3324-BVXI	4 (USB 3.0)	0	Yes	Yes	-40-85 °C	100-BGA
25.	CYUSB3326-BVXC	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	0-70 °C	100-BGA
26.	CYUSB3326-BVXI	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2	Yes	No	-40-85 °C	100-BGA
27.	CYUSB3328-BVXC	8 (4 SS, 4 USB 2.0)	4	Yes	Yes	0-70 °C	100-BGA
28.	CYUSB2302-68LTXI	2 (USB 2.0)	0	Yes	No	-40-85 °C	68-QFN
29.	CYUSB2304-68LTXI	4 (USB 2.0)	0	Yes	No	-40-85 °C	68-QFN

Ordering Code Definitions

