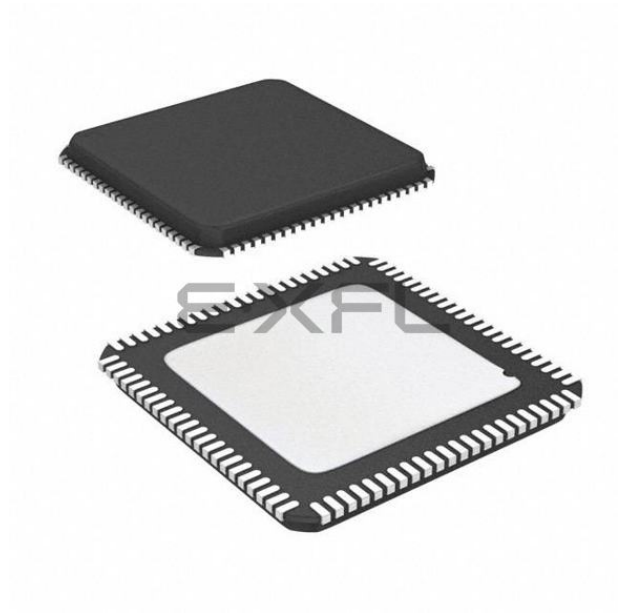

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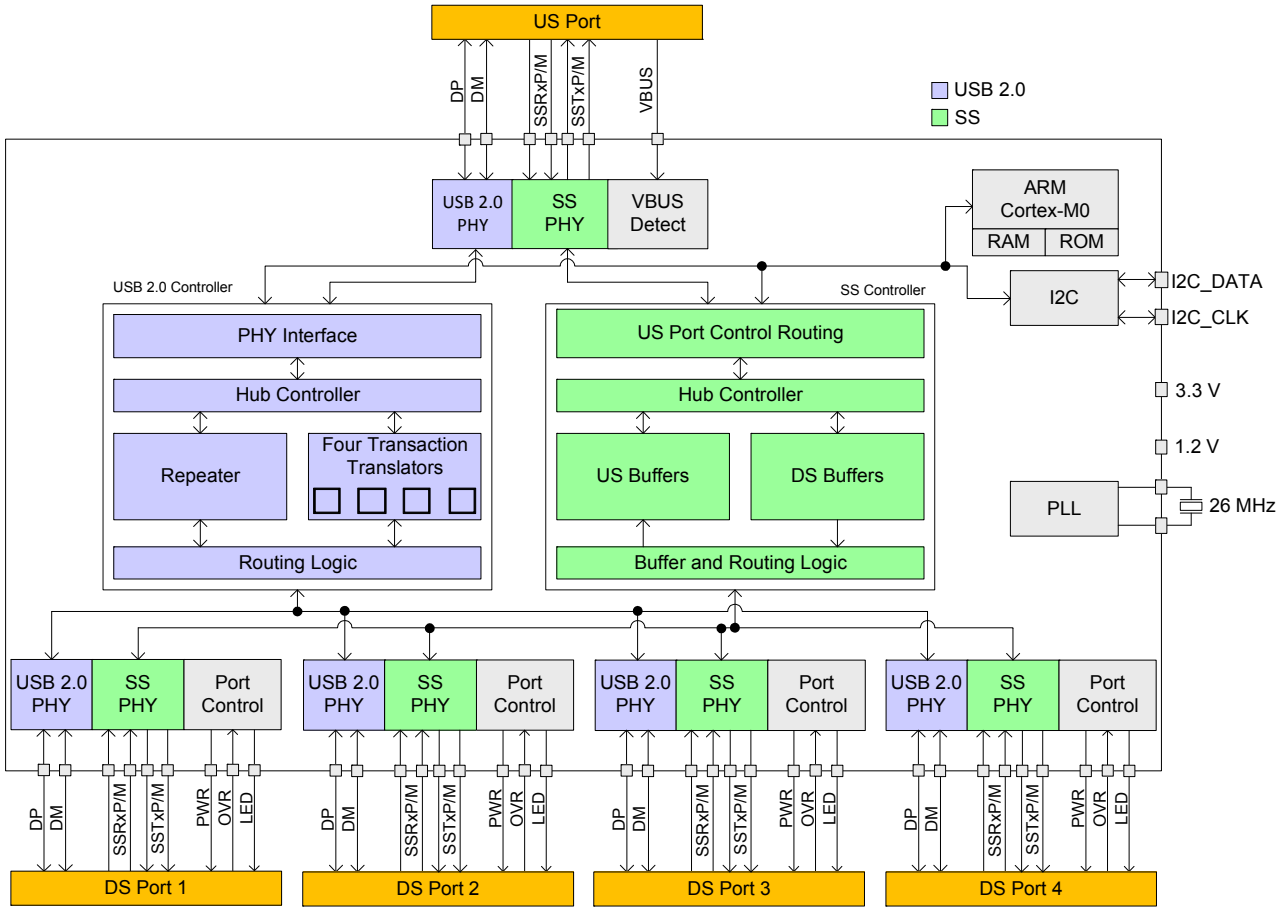
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB 3.0 Hub Controller
Core Processor	ARM® Cortex®-M0
Program Memory Type	ROM (32kB)
Controller Series	CYUSB
RAM Size	16K x 8
Interface	I²C
Number of I/O	10
Voltage - Supply	1.14V ~ 1.26V, 2.5V ~ 2.7V, 3V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad
Supplier Device Package	88-QFN (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3324-88ltxc

Block Diagram



Pin Information

Figure 6. HX3 68-Pin QFN 2-Port Pinout

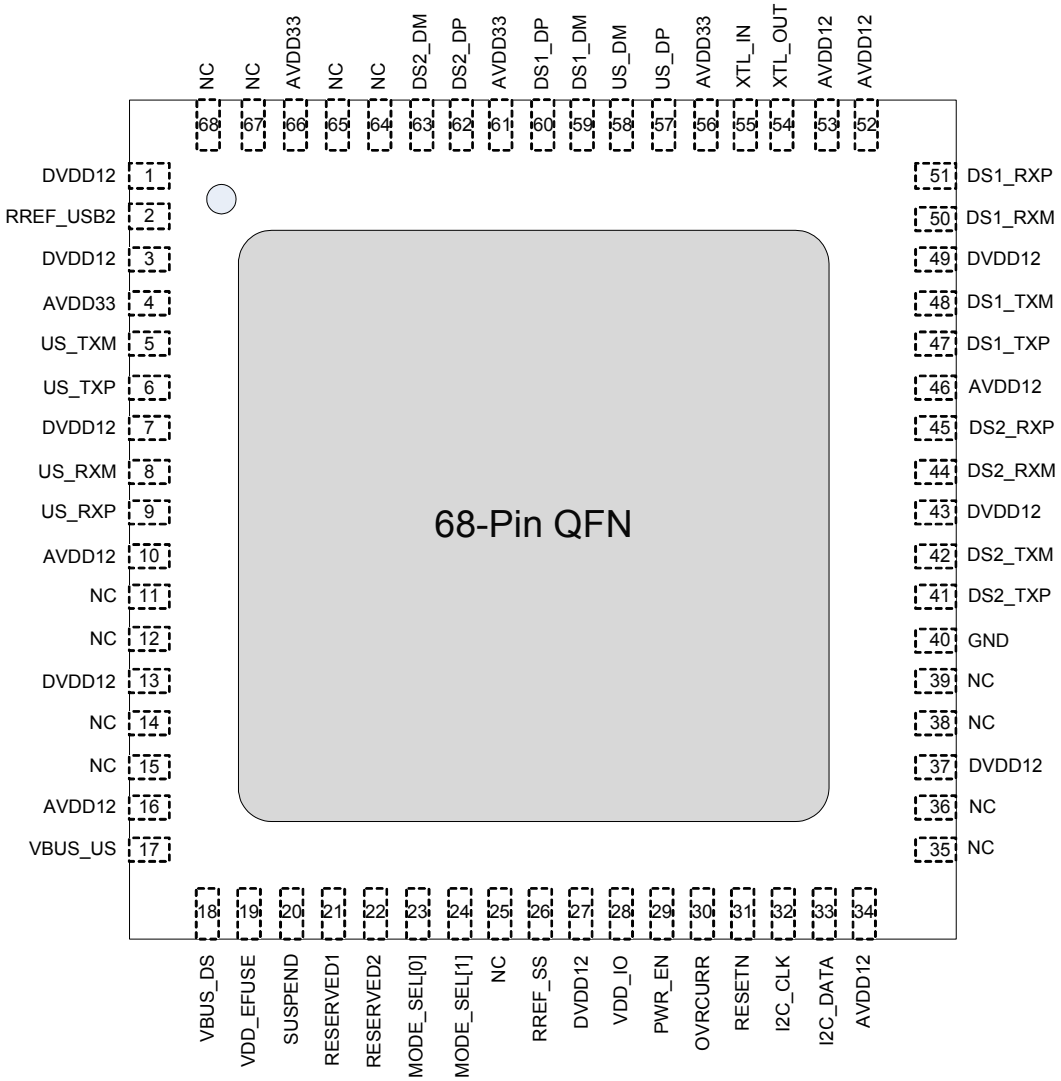


Figure 7. HX3 68-Pin QFN 4-Port Pinout

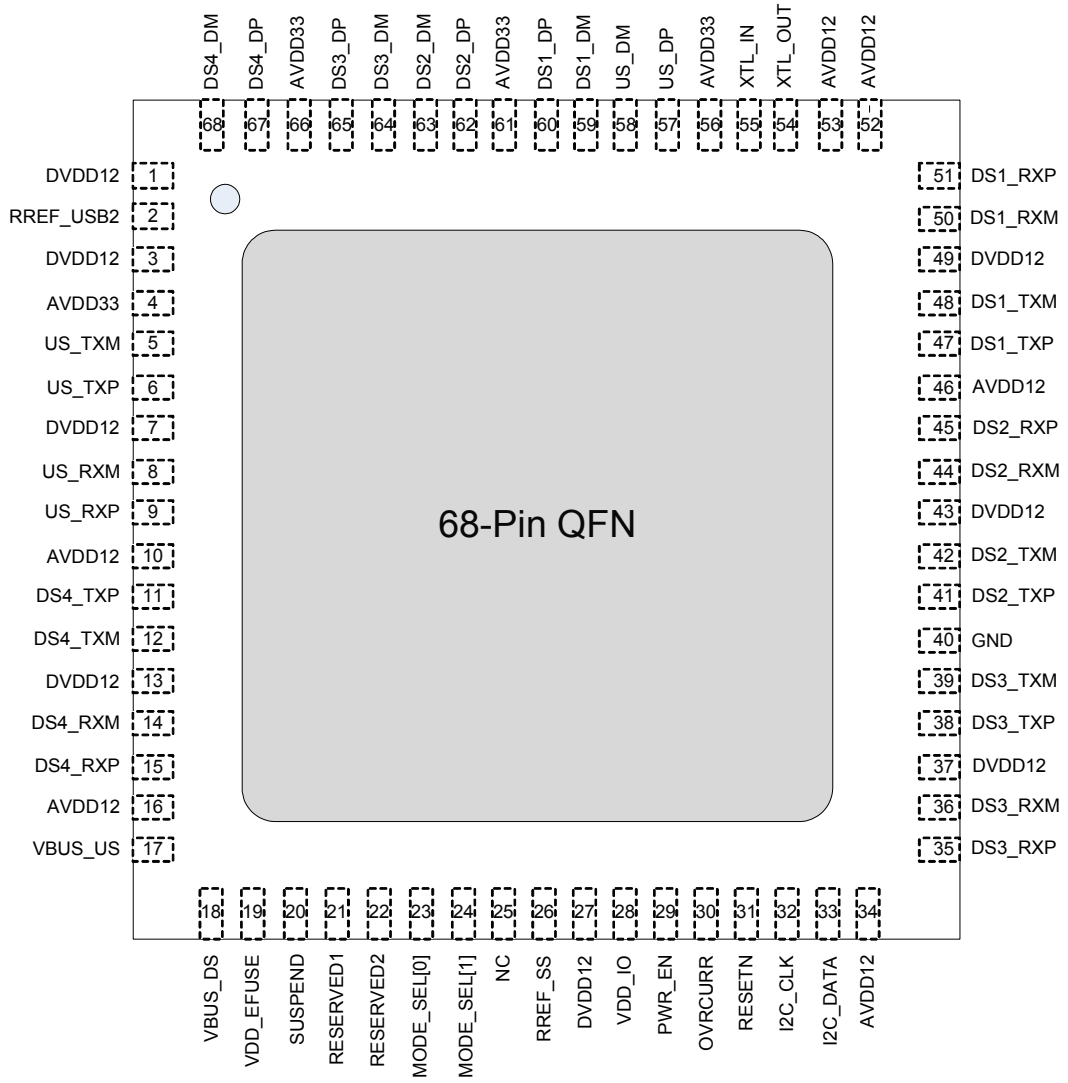


Figure 8. HX3 100-Ball BGA Pinout for CYUSB3302

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
NC	NC	NC	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**	**B9**	**B10**
NC	NC	NC	VDD_IO	VSS	AVDD33	NC	NC	NC	DVDD12
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**
US_TXM	NC	NC	NC	NC	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**	**D9**	**D10**
US_TXP	NC	NC	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**	**E8**	**E9**	**E10**
DVDD12	RREF_USB2	NC	NC	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**	**F9**	**F10**
US_RXM	VSS	AVDD33	MODE_SEL[1]	DVDD12	OVRCURR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**	**G9**	**G10**
US_RXP	VBUS_DS	SUSPEND	RESERVED1	MODE_SEL[0]	VDD_IO	PWR_EN	I2C_DATA	VSS	DS2_RXM
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**	**H9**	**H10**
AVDD12	VBUS_US	VDD_EFUSE	RESERVED2	RREF_SS	VSS	DS2_TXM	DS2_TXP	NC	AVDD12
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**	**J10**
VSS	AVDD12	VSS	GPIO	NC	I2C_CLK	NC	NC	VSS	NC
K1	**K2**	**K3**	**K4**	**K5**	**K6**	**K7**	**K8**	**K9**	**K10**
NC	NC	DVDD12	NC	NC	NC	NC	NC	DVDD12	NC

Table 3. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB2302 and CYUSB2304

Pin Name		Type	68-QFN Pin#	100-BGA Ball #	Description
CYUSB2302	CYUSB2304				
US Port					
NC		I	9	G1	SuperSpeed receive plus
NC		I	8	F1	SuperSpeed receive minus
NC		O	6	D1	SuperSpeed transmit plus
NC		O	5	C1	SuperSpeed transmit minus
US_DP		I/O	57	A9	USB 2.0 data plus
US_DM		I/O	58	A8	USB 2.0 data minus
DS1 Port					
NC		I	51	D10	SuperSpeed receive plus
NC		I	50	C10	SuperSpeed receive minus
NC		O	47	F8	SuperSpeed transmit plus
NC		O	48	E8	SuperSpeed transmit minus
DS1_DP		I/O	60	C7	USB 2.0 data plus
DS1_DM		I/O	59	C8	USB 2.0 data minus
DS2 Port					
NC		I	45	F10	SuperSpeed receive plus
NC		I	44	G10	SuperSpeed receive minus
NC		O	41	H8	SuperSpeed transmit plus
NC		O	42	H7	SuperSpeed transmit minus
DS2_DP		I/O	62	A6	USB 2.0 data plus
DS2_DM		I/O	63	A5	USB 2.0 data minus
DS3 Port					
NC	NC	I	35	K10	SuperSpeed receive plus
NC	NC	I	36	J10	SuperSpeed receive minus
NC	NC	O	38	K7	SuperSpeed transmit plus
NC	NC	O	39	K8	SuperSpeed transmit minus
NC	DS3_DP	I/O	65	C4	USB 2.0 data plus
NC	DS3_DM	I/O	64	C5	USB 2.0 data minus
DS4 Port					
NC	NC	I	15	K4	SuperSpeed receive plus
NC	NC	I	14	K5	SuperSpeed receive minus
NC	NC	O	11	K1	SuperSpeed transmit plus
NC	NC	O	12	K2	SuperSpeed transmit minus
NC	DS4_DP	I/O	67	A3	USB 2.0 data plus
NC	DS4_DM	I/O	68	A2	USB 2.0 data minus
OVRCURR		I	30	F6	Ganged overcurrent input
PWR_EN		I/O	29	G7	Ganged power enable output
NC		I/O	25	NA	NC

Table 3. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB2302 and CYUSB2304 *(continued)*

Pin Name		Type	68-QFN Pin#	100-BGA Ball #	Description
CYUSB2302	CYUSB2304				
RESERVED1		I/O	21	G4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
RESERVED2		I	22	H4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
Mode Select, Clock, and Reset					
MODE_SEL[0]		I	23	G5	Device operation mode select bit 0; refer to Table 5 on page 24
MODE_SEL[1]		I	24	F4	Device operation mode select bit 1; refer to Table 5 on page 24
XTL_OUT		A	54	E6	Crystal out
XTL_IN		A	55	E5	Crystal in
RESETN		I	31	F7	Active LOW reset input
I2C_CLK		I/O	32	J6	I^2C clock
I2C_DATA		I/O	33	G8	I^2C data
SUSPEND		I/O	20	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and Ground					
VDD_EFUSE		PWR	19	H3	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V.
AVDD12		PWR	10, 16, 34, 46, 52, 53	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND		PWR	40	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12		PWR	1, 3, 7, 13, 27, 37, 43, 49,	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS _US		PWR	17	H2	This pin must be connected to VBUS from US port
VBUS_DS		PWR	18	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	4, 56, 61, 66	A4, A7, B6, F3	3.3 V analog supply
VDD_IO		PWR	28	B4, E7, G6	3.3 V I/O supply
USB Precision Resistors					
RREF_USB2		A	2	E2	Connect pin to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY.
RREF_SS		A	26	H5	Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration.

Figure 10. HX3 88-Pin QFN 2-Port Pinout

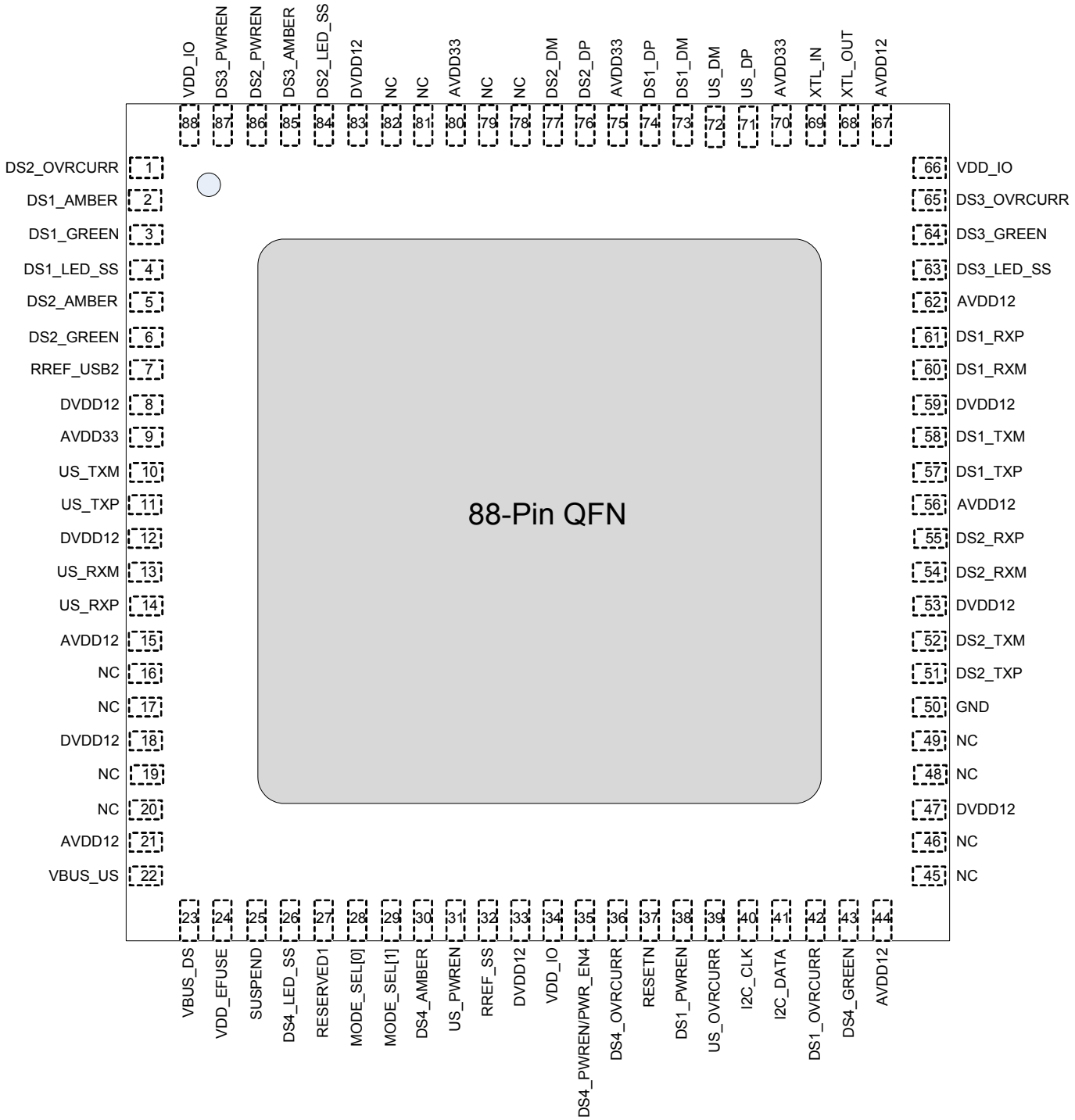


Figure 11. HX3 88-Pin QFN 4-Port Pinout

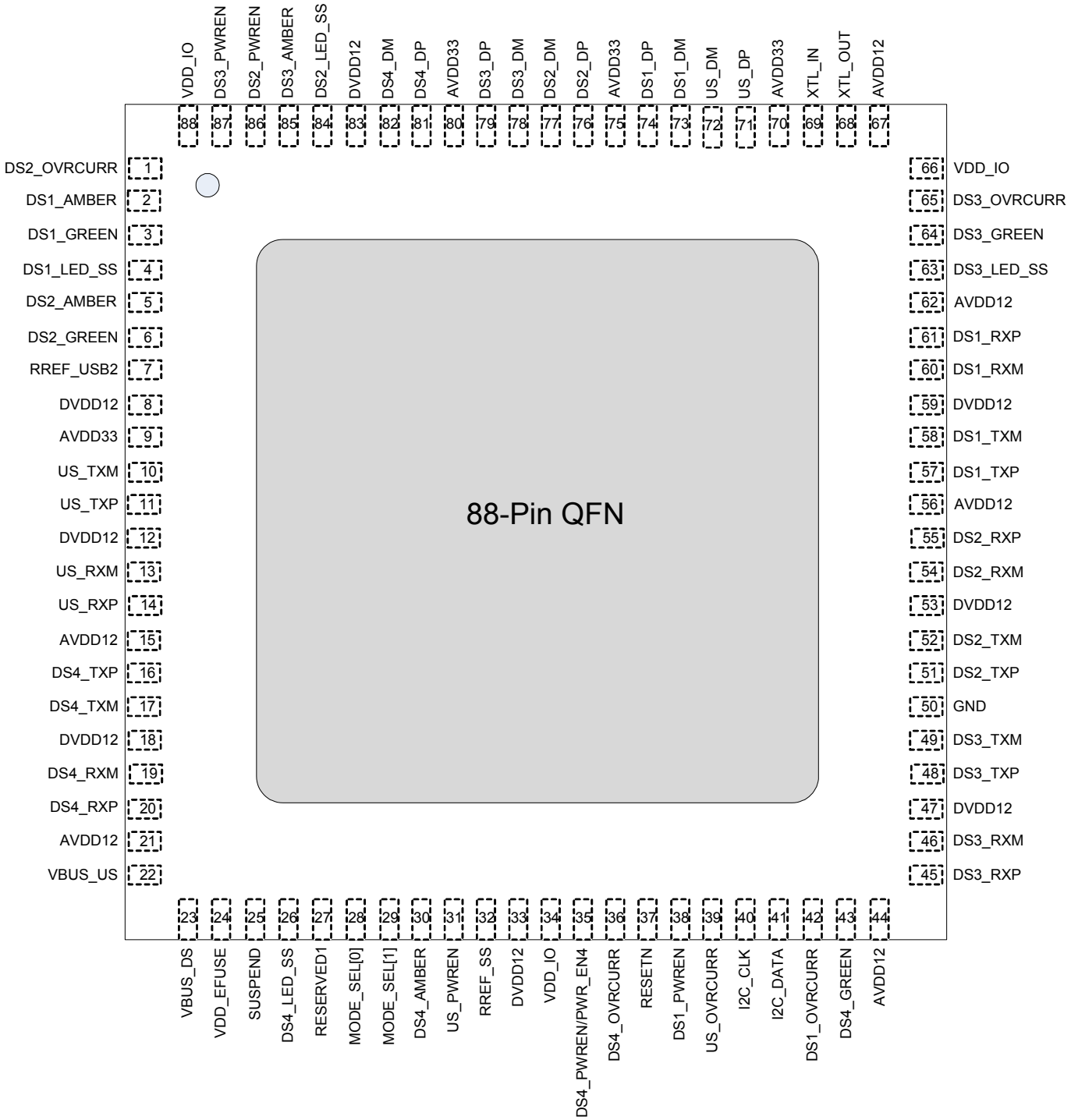


Figure 12. HX3 100-Ball BGA Pinout for CYUSB3312

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
DS3_PWREN	NC	NC	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**	**B9**	**B10**
DS2_OVRCURR	DS2_PWREN	DS3_AMBER	VDD_IO	VSS	AVDD33	DS3_OVRCURR	DS3_GREEN	DS3_LED_SS	DVDD12
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**
US_TXM	DS1_AMBER	DS2_LED_SS	NC	NC	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**	**D9**	**D10**
US_TXP	DS1_LED_SS	DS1_GREEN	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**	**E8**	**E9**	**E10**
DVDD12	RREF_USB2	DS2_GREEN	DS2_AMBER	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**	**F9**	**F10**
US_RXM	VSS	AVDD33	MODE_SEL[1]	DVDD12	DS4_OVRCURR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**	**G9**	**G10**
US_RXP	VBUS_DS	SUSPEND	RESERVED1	MODE_SEL[0]	VDD_IO	DS4_PWREN	I2C_DATA	VSS	DS2_RXM
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**	**H9**	**H10**
AVDD12	VBUS_US	VDD_EFUSE	DS4_LED_SS	RREF_SS	VSS	DS2_TXM	DS2_TXP	DS4_GREEN	AVDD12
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**	**J10**
VSS	AVDD12	VSS	DS4_AMBER	US_PWREN	I2C_CLK	DS1_PWREN	DS1_OVRCURR	VSS	NC
K1	**K2**	**K3**	**K4**	**K5**	**K6**	**K7**	**K8**	**K9**	**K10**
NC	NC	DVDD12	NC	NC	US_OVRCURR	NC	NC	DVDD12	NC

Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314 CYUSB3324 CYUSB3326 CYUSB3328				
US Port					
US_RXP		I	14	G1	SuperSpeed receive plus
US_RXM		I	13	F1	SuperSpeed receive minus
US_TXP		O	11	D1	SuperSpeed transmit plus
US_TXM		O	10	C1	SuperSpeed transmit minus
US_DP		I/O	71	A9	USB 2.0 data plus
US_DM		I/O	72	A8	USB 2.0 data minus
US_OVRCURR		I	39	K6	CYUSB3324/3328: Overcurrent detect input for US port in ACA-Dock mode. If ACA-Dock mode is disabled using Configuration Options on page 24, this pin must be pulled HIGH using a 10 kΩ to VDD_IO. Other part numbers: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
US_PWREN[5]		I/O	31	J5	CYUSB3324/3328: VBUS power enable output for US port in ACA-Dock mode. If ACA-Dock mode is disabled using Configuration Options on page 24, this pin can be left floating if Pin-Strap is not enabled. Other part numbers: This pin can be left floating if Pin-Strap (Pin# 63) is not enabled.
PWR_SW_POL[6]					This pin is called PWR_SW_POL in pin-strap configuration mode.
DS1 Port					
DS1_RXP		I	61	D10	SuperSpeed receive plus
DS1_RXM		I	60	C10	SuperSpeed receive minus
DS1_TXP		O	57	F8	SuperSpeed transmit plus
DS1_TXM		O	58	E8	SuperSpeed transmit minus
DS1_DP		I/O	74	C7	USB 2.0 data plus
DS1_DM		I/O	73	C8	USB 2.0 data minus
DS1_OVRCURR		I	42	J8	Overcurrent detect input for DS1 port
DS1_PWREN[5]		I/O	38	J7	VBUS power enable output for DS1 port. When the port is disabled, this pin is in tristate.
DS1_CDP_EN[6]					This pin is called DS1_CDP_EN in pin-strap configuration mode.
DS1_AMBER[5]		I/O	2	C2	LED_AMBER output for DS1 port
ACA_DOCK[6]					This pin is called ACA-DOCK in pin-strap configuration mode.
DS1_GREEN[5]		I/O	3	D3	CYUSB3312/3314/3324: LED_GREEN output for DS1 port
DS1_VBUSEN_SL[5]					CYUSB3326/3328: VBUS power enable output for SS port 1
PORT_DISABLE[0][6]					This pin is called PORT_DISABLE[0] in pin-strap configuration mode.
DS1_LED_SS[5]		I/O	4	D2	LED_SS output for DS1 port
PORT_DISABLE[1][6]					This pin is called PORT_DISABLE[1] in pin-strap configuration mode.

Notes
5. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
6. For pin-strap configuration details, refer to Table 6 on page 25.

Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X *(continued)*

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314 CYUSB3324 CYUSB3326 CYUSB3328				
SUSPEND		I/O	25	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and Ground					
VDD_EFUSE		PWR	24	H3	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V
AVDD12		PWR	15, 21, 44, 56, 62, 67	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND		PWR	50	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12		PWR	8, 12, 18, 33, 47, 53, 59, 83	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS _US		PWR	22	H2	CYUSB3324/3328: Connect the VBUS_US pin to the local 5 V supply. If ACA-Dock mode is disabled using Configuration Options on page 24, this pin must be connected to VBUS from US port. Other part numbers: This pin must be connected to VBUS from US port.
VBUS_DS		PWR	23	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	9, 70, 75, 80	A4, A7, B6, F3	3.3 V analog supply
VDD_IO		PWR	34, 66, 88	B4, E7, G6	3.3 V I/O supply
USB Precision Resistors					
RREF_USB2		A	7	E2	Connect pin to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY.
RREF_SS		A	32	H5	Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration.

Temperature range of 25 °C–70 °C and programming voltage of 2.5 V–2.7 V.

Pin-Strap Configuration

Pin-straps are supported for select product options (see Table 1 on page 5) to provide reconfigurability without an additional EEPROM. The pin-strap configuration is enabled by pulling the Pin #63 of 88-pin QFN HIGH. Table 6 on page 25 shows the configuration options supported through pin-straps and the GPIOs used for this purpose. Figure 16 and Figure 17 show how the GPIOs need to be connected if pin-strap and LED connection are required or only pin-strap is required.

HX3 samples pin-strap GPIOs at power-up. Floating straps are considered as invalid and the default configuration is used. If PIN_STRAP (Pin #63 of 88-pin QFN) is floating, all strap inputs are considered invalid. A GPIO is considered strapped "1" or "0" when connected with a weak pull-up (10 kΩ) or pull-down (10 kΩ) respectively. After the initial sampling at power-up and reset, the GPIOs are used in their normal functions.

Figure 16. Pin-Strap With LED or LED-Only Connection

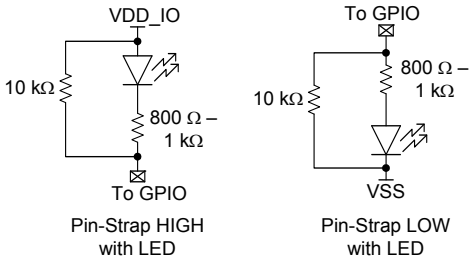


Figure 17. Pin-Strap Connection

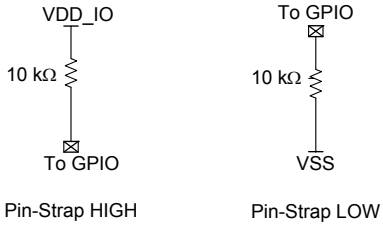


Table 6. Pin-Strap Configuration

88-QFN Pin #	Pin-Strap Name	Strapped '0'[11]		Strapped '1'[11]	
30	I2C_DEV_ID[12]	ID 0: HX3 I²C slave address (7 bits) is 0x60. This is also the default I²C slave address for the 68-pin QFN package.		ID 1: HX3 I²C slave address (7 bits) is 0x58	
31	PWR_SW_POL	Power enable and overcurrent will be active LOW		Power enable and overcurrent will be active HIGH	
2	ACA_DOCK	Disabled		Enabled	
84	PWR_EN_SEL	Individual		Gang	
63	PIN_STRAP[13]	No pin-strapping		Pin-strapping configuration enabled	
4	PORT_DISABLE[1]	PORT_DISABLE[1:0] = b'00: DS1, DS2, DS3, DS4 active b'01: DS1, DS2, DS3 active b'10: DS1, DS2 active b'11: DS1 active Pin-straps cannot enable ports disabled by factory setting.			
3	PORT_DISABLE[0]				
6	NON_REMOVABLE[1][14]	NON_REMOVABLE[1:0] = b'00: DS1, DS2, DS3, DS4 removable b'01: DS1, DS2, DS3 removable b'10: DS1, DS2 removable b'11: DS1 removable			
5	NON_REMOVABLE[0][14]				
85	VID[2]	Reserved. If PIN_STRAP is enabled and CY VID is required, strap VID[2:0] to '1'.			
64	VID[1]				
43	VID[0]				
38	DS1_CDP_EN[15]	strapped '0'	strapped '1'	strapped '0'	strapped '1'
		DS1 CDP enabled	DS1 CDP disabled	DS1 CDP disabled	DS1 CDP enabled
86	DS2_CDP_EN[15]	DS2 CDP enabled	DS2 CDP disabled	DS2 CDP disabled	DS2 CDP enabled
87	DS3_CDP_EN[15]	DS3 CDP enabled	DS3 CDP disabled	DS3 CDP disabled	DS3 CDP enabled
35	DS4_CDP_EN[15]	DS4 CDP enabled	DS4 CDP disabled	DS4 CDP disabled	DS4 CDP enabled

Notes
11. See Figure 16 and Figure 17.
12. I2C_DEV_ID is valid only when HX3 is in I²C slave mode.
13. VID, PORT_DISABLE, NON_REMOVABLE are group straps. If one of the pins in a group strap is floating (INVALID), that group input will be INVALID and the default will not be overwritten.
14. These DS ports are exposed ports and the connected devices can be removed.
15. DSx_CDP_EN will be active LOW input when PWR_SW_POL is set to active LOW; similarly DSx_CDP_EN will be active HIGH input when PWR_SW_POL is set to active HIGH.

I²C Configuration

When enabled for I²C configuration through the MODE_SEL pins (See Table 5 on page 24), HX3 can be configured as an I²C master or as an I²C slave. HX3's configuration data is a maximum of 197 bytes and HX3's firmware is 10 KB. Note that HX3's firmware also includes configuration settings.

HX3 as I²C Master

HX3 reads configurations from an external I²C EEPROM with sizes ranging from 16 to 64 KB. An example of a supported EEPROM is 24LC128. Based on the contents of the bSignature and bImageType fields in Table 7 on page 26, HX3 performs one of the following actions:

- Loads custom configuration settings from the EEPROM when bSignature is "CY" and bImageType is 0xD4.
- Loads the Cypress-provided firmware from the EEPROM when bSignature is "CY" and bImageType is 0xB0. This firmware also includes configuration settings.
- If bSignature ≠ "CY", HX3 enumerates in the vendor-specific mode.

The contents of the EEPROM can be updated with the easy-to-use Cypress Blaster Plus tool. Blaster Plus is a GUI-based tool to configure HX3. This tool allows to do the following:

- Download the Cypress-provided firmware from a PC via HX3's US port and store it on an EEPROM connected to HX3's I²C port.
- Read the configuration settings from the EEPROM. These settings are displayed in the Blaster Plus GUI. Modify settings as required.
- Write back the updated settings on to the EEPROM. In addition, an image file can be created for external use.

The Blaster Plus tool, user guide, and the Cypress-provided firmware are available at www.cypress.com/hx3.

HX3 as I²C Slave

An external I²C master can program the configuration settings into HX3 according to the EEPROM map in Table 7 on page 26. Alternatively, the HX3 firmware (<10 KB), which includes configuration settings, can also be programmed. It is recommended to use the Blaster Plus tool to create the HX3 firmware or configuration image file. HX3's I²C slave address needs to be provided while creating the image file. Refer to Table 6 for HX3's I²C slave address.

Table 7. EEPROM Map

I²C Offset	Bits	Name	Default	Description
0	7:0	bSignature LSB ("C")	0x43	The first byte of the 2-byte signature initialized with "CY" ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device.
1	7:0	bSignature MSB ("Y")	0x59	The second byte of the 2-byte signature initialized with "CY" ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device.
2	7:6	bImageCTL	b'00	Reserved
	5:4	I²C Speed	b'11	b'01: 400 kHz b'11: 100 kHz
	3:1	bImageCTL	b'000	Reserved
	0	bImageCTL	0	0: Execution binary file 1: Data file
3	7:0	bImageType	0xD4	0xD4: Load only configuration 0xB0: Load firmware boot image All other bImageType will return an error code.
4	7:0	bD4Length	40	bD4Length is defined in bytes as the length from offset 5. I²C offset bytes 0–4 are the header bytes. bD4Length = 6: Only update VID, PID, and DID bD4Length = 18: Configuration options (no PHY trim) bD4Length = 40: Configuration options with PHY trim options bD4Length > 40: User must provide valid string descriptors bD4Length > 192: Error
5	7:0	VID [7:0]	0xB4	Custom Vendor ID - LSB
6	7:0	VID [15:8]	0x04	Custom Vendor ID - MSB
7	7:0	PID [7:0]	0x04	Custom Product ID (PID) Default: 0x6504 If separate PID is used for USB 2.0, the USB 2.0 PID will be read from offset 35 and 36. Else, USB 2.0 PID = PID+2; Default: 0x6506
8	7:0	PID [15:8]	0x65	

Table 7. EEPROM Map *(continued)*

I²C Offset	Bits	Name	Default	Description
51 + X	7:0	bString: Product	'C', 0, 'Y', 0, '-', 0, 'H', 0, 'X', 0, '3', 0, ' ', 0, 'H', 0, 'U', 0, 'B', 0	Product string: UNICODE UTF-16LE per USB 2.0 specification: "CY-HX3 HUB"
49 + X + Y	7:0	bLength: Serial Number (Z)	22	Serial number string length ("bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number" should be less than or equal to 152 bytes). Z ≤ 66.
50 + X + Y	7:0	DescType	3	String descriptor type (constant value)
51 + X + Y	7:0	bString: Serial Number	'1', 0, '2', 0, '3', 0, '4', 0, '5', 0, '6', 0, '7', 0, '8', 0, '9', 0, 'A', 0	Serial number string: UNICODE UTF-16LE per USB 2.0 specification: "123456789A"

EMI

HX3 meets the EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. HX3 tolerates EMI conducted by aggressors outlined by the above specifications and continues to function as expected.

ESD

HX3 has a built-in ESD protection on all pins. The ESD protection level provided on these ports is 2.2 kV Human Body Model (HBM) based on the JESD22-A114 specification.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature..... –65 °C to +150 °C

Operating temperature ..... –40 °C to +85 °C

Electrostatic discharge voltage ..... 2200 V

Oscillator or crystal frequency ..... 26 MHz ±150 ppm

I/O voltage supply .....3 V to 3.6 V

Maximum input sink current per I/O ..... 4 mA

Electrical Specifications

HX3 meets all USB-IF Electrical Compliance specifications.

DC Electrical Characteristics

Table 8. DC Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
DVDD12	1.2 V core supply	–	1.14	1.2	1.26	V
VDD_EFUSE	eFuse supply	Normal operation	1.14	1.2	1.26	V
		Programming	2.5	2.6	2.7	V
AVDD12	1.2 V analog supply	–	1.14	1.2	1.26	V
VDD_IO	3.3 V I/O supply	–	3	3.3	3.6	V
AVDD33	3.3 V analog supply	–	3	3.3	3.6	V
V_{IH}	Input HIGH voltage	–	0.7 × VDD_IO	–	VDD_IO	V
V_{IL}	Input LOW voltage	–	0	–	0.3 × VDD_IO	V
V_{OH}	Output HIGH voltage	Output HIGH voltage at $I_{OH} \leq +4$ mA	2.4	–	–	V
V_{OL}	Output LOW voltage	Output LOW voltage at $I_{OL} \geq -4$ mA	–	–	0.4	V
I_{OS}	Input sink current	LED GPIO usage	–	–	4	mA
I_{IX}	Input leakage current	All I/O signals held at VDD_IO or GND	–1	–	1	µA
I_{OZ}	Output HI-Z leakage current	–	–	–	10	µA
I_{CC}	1.2 V supplies combined operating current	–	–	410	526	mA
I_{CC}	3.3 V supplies combined operating current	–	–	260	286	mA
V_{RAMP}	Voltage ramp rate on core and I/O supplies	Voltage ramp must be monotonic	0.2	–	50	V/ms
V_N	Noise level permitted on core and I/O supplies	Max p-p noise level permitted on all supplies except AVDD	–	–	100	mV
V_{N_USB}	Noise level permitted on AVDD12 and AVDD33 supply	Max p-p noise level permitted USB supply	–	–	20	mV

Power Consumption

Table 9 provides the power consumption estimates for HX3 under different conditions. Table 10 summarizes the power consumption for various combinations of devices connected to DS ports.

For example, to calculate the HX3 power consumption for three SS devices connected to DS ports (and no device connected to one DS port), and a US port connected to a USB 3.0 host:

Power consumption = [a] + 2*[g] = 492.5 + 2*76 = 644 mW

[a] is the active power consumption for the US port connected to a USB 3.0 host and the SS device connected to the DS port.

[g] is the incremental power consumption for an additional SS device connected to the DS port.

Table 9. Power Consumption Estimates for Various Usage Scenarios

Device Condition	Number and Speed of DS Ports Connected	Typical Consumption			Comments
		Supply Current (mA)		Power (mW)	
		1.2 V	3.3 V		
Suspend [18]	NA	12.0	7.1	37.8	–
Active power with USB 3.0 host [19]	1 SS	204.1	75.0	492.5	[a]
	1 HS	51.2	45.2	210.7	[b]
	1 FS	51.2	34.0	173.7	[c]
	1 SS + 1 HS	218.0	103.4	602.9	[d]
Active power with USB 2.0 host [19, 20]	1 HS	51.2	45.2	210.7	[e]
	1 FS	51.2	34.0	173.7	[f]
Incremental active power for additional DS port	SS	39.4	8.7	76.0	[g]
	HS	7.0	19.8	73.7	[h]
	FS	7.0	14.2	55.2	[i]
Active power saving per disabled DS port[21]	–	10.6	9.6	44.4	[j]

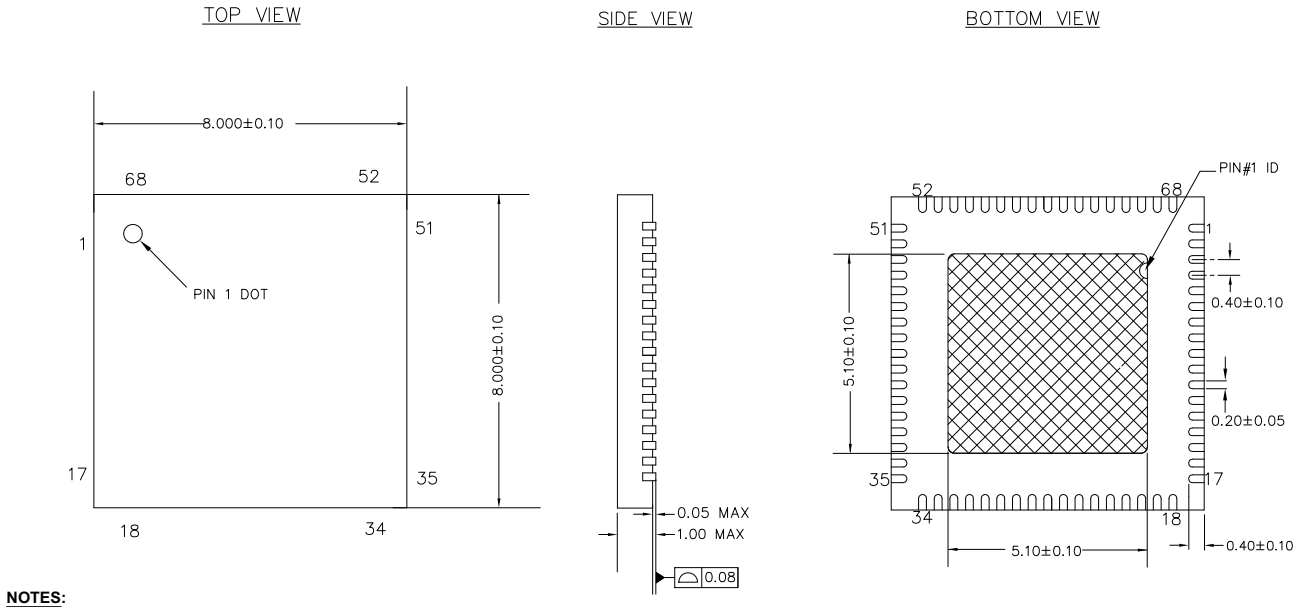
Table 10. Power Consumption Under Various Configurations

Configuration	Number of DS Devices Connected With Data Transfer	Typical Consumption			Comments
		Supply Current (mA)		Power (mW)	
		1.2 V	3.3 V		
USB 3.0 4-Port Hub (USB 3.0 host)	4 SS devices	322	101	720	[a] + 3*[g]
	3 SS + 1 HS devices	297	121	755	[d] + 2*[g]
	3 SS devices	283	92	644	[a] + 2*[g]
USB 3.0 4-Port Hub with one port disabled (USB 3.0 host)	3 SS devices	272	83	600	[a] + 2*[g] - [j]
	2 SS + 1 HS devices	247	103	634	[d] + [g] - [j]
Shared Link with eight DS ports	4 SS + 4 HS devices	357	189	1052	[d] + 3*([g] + [h])
USB 2.0 4-Port Hub (USB 2.0 host)	4 HS devices	72	105	432	[e] + 3*[h]
	3 HS + 1 FS devices	72	99	413	[e] + 2*[h] + [i]

Notes
18. US port in low-power state (SS in U3 and USB 2.0 in L2).
19. All four DS ports are enabled.
20. US SS disabled using configuration options. Refer to Table 7 on page 26 for I^2C configuration options.
21. Power saving applicable only with a USB 3.0 host. DS ports can be disabled through configuration options. Refer to Table 6 on page 25 for pin-strapping and Table 7 on page 26 for I^2C configuration options.

Package Diagrams

Figure 18. 68-pin QFN (8 × 8 × 1.0 mm) LT68B 5.1 × 5.1 mm EPAD (Sawn) Package Outline

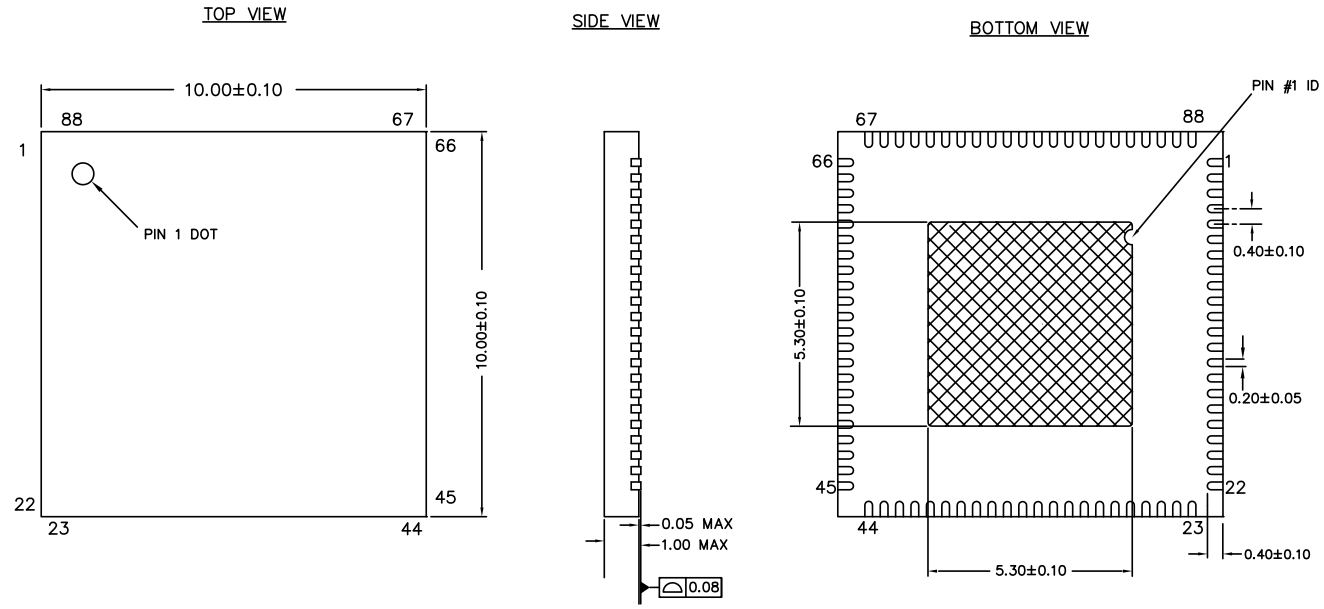


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC#: MO-220
3. ALL DIMENSIONS ARE IN MILLIMETERS

001-78925 *B

Figure 19. 88-pin QFN (10 × 10 × 1.0 mm) LT88B 5.3 × 5.3 EPAD (Sawn) Package Outline



001-76569 *B

Acronyms

Table 15. Acronyms Used in this Document

Acronym	Description
ACA	Accessory Charging Adapter
ASSP	Application-Specific Standard Product
BC	Battery Charging
CDP	Charging Downstream Port
DS	DownStream
DCP	Dedicated Charging Port
DNU	Do Not Use
DWG	Device Working Group
EEPROM	Electrically Erasable Programmable Read-Only Memory
FS	Full-Speed
FW	FirmWare
GND	GrouND
GPIO	General-Purpose Input/Output
HS	Hi-Speed
ISP	In-System Programming
I/O	Input/Output
LS	Low-Speed
NC	No Connect
OTG	On-The-Go
PID	Product ID
POR	Power-On Reset
ROM	Read-Only Memory
SCL	Serial CLock
SDA	Serial DAta
SS	SuperSpeed
TT	Transaction Translator
US	UpStream
VID	Vendor ID

Reference Documents

USB 2.0 Specification

USB 3.0 Specification

Battery Charging Specification

Document Conventions

Units of Measure

Table 16. Units of Measure

Symbol	Unit of Measure
°C	degree celsius
Ω	ohm
Gbps	gigabit per second
KB	kilobyte
kHz	kilohertz
kΩ	kiloohm
Mbps	megabit per second
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
ppm	parts per million
V	volt

Silicon Revision History

This datasheet is applicable for the USB-IF certified (TID# 330000060) HX3 Rev. *D and Rev. *C Silicon.

Rev. *D: This Silicon revision improves the yield of HX3, and is drop-in compatible for all the part numbers. There is no need to change the board design or layout to use the HX3 Rev. *D Silicon. Products are completely compatible with the HX3 Rev. *C Silicon.

Rev. *C: This Silicon revision fixes the errata applicable to the Rev. *A Silicon.

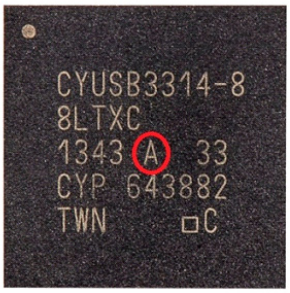
The following table defines the changes between Rev. *A, Rev. *C, and Rev. *D Silicon.

No.	Items	Part Numbers	Rev. *A	Rev. *C	Rev. *D
1	USB-IF Compliance	All	Requires firmware on external EEPROM	No external EEPROM required	No external EEPROM required
2	FS-only hub or host connected to HX3 Upstream Port	All	Not supported	Supported	Supported
3	Suspend Power	All	90 mW	37.8 mW	37.8 mW

Method of Identification

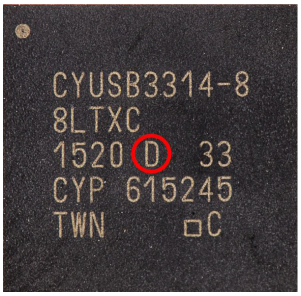
Markings on row 3 of the HX3 package differentiate Rev. *D Silicon from Rev. *C Silicon and Rev. *A Silicon as indicated in the example below. Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

HX3 REV *A SILICON



HX3 REV *C SILICON

HX3 REV *D SILICON



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