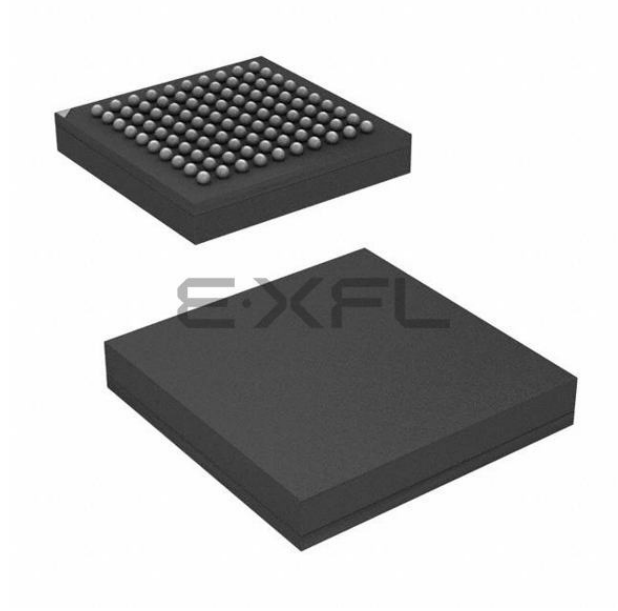


Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

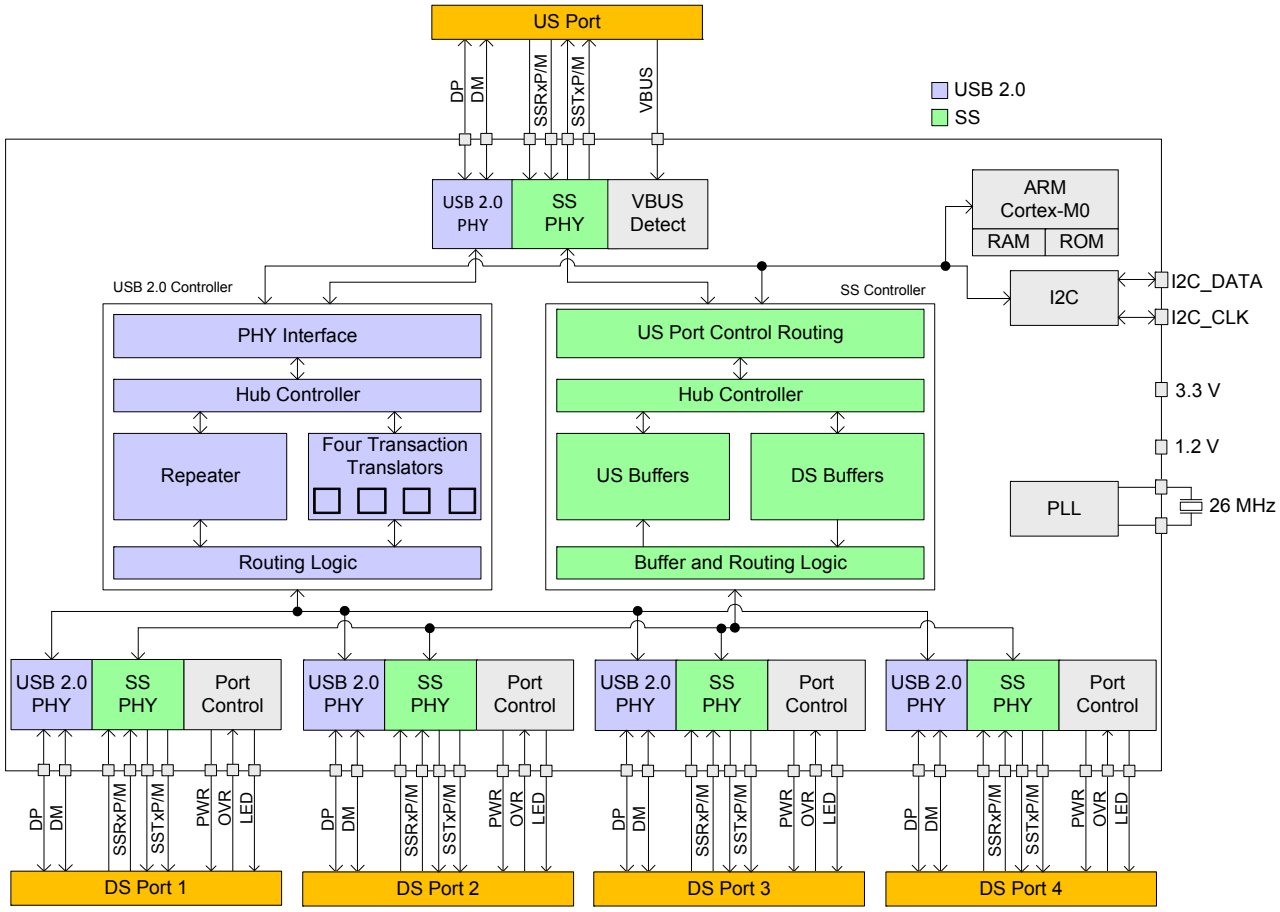
Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

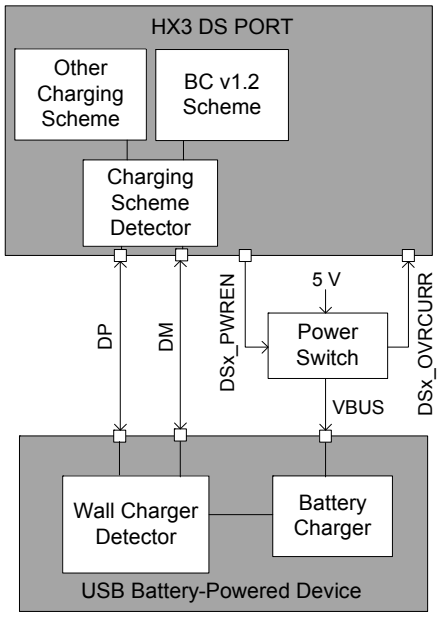
Details	
Product Status	Active
Applications	USB 3.0 Hub Controller
Core Processor	ARM® Cortex®-M0
Program Memory Type	ROM (32kB)
Controller Series	CYUSB
RAM Size	16K x 8
Interface	I²C
Number of I/O	10
Voltage - Supply	1.14V ~ 1.26V, 2.5V ~ 2.7V, 3V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3328-bvxc

Block Diagram



When the US port is disconnected from the host, HX3 detects if any of the DS ports are connected to a device requesting charging. It determines the charging method and then switches to the appropriate signaling based on the detected charging specification as shown in Figure 4. The hub either emulates a USB-compliant dedicated charging port by connecting DP and DM (see the BC v1.2 specification) or other supported proprietary charging schemes.

Figure 4. Ghost Charge Implementation in HX3



Ghost Charge is enabled by default and can be disabled through configuration. Refer to Configuration Options on page 24.

Vendor-Command Support

HX3 supports vendor-specific requests and can also enumerate as a vendor-specific device. The vendor-specific request can be used to (a) bridge USB and I^2C and (b) configure HX3. This feature can be used for the following applications:

- Firmware upgrade of an external ASSP connected to HX3 through USB
- In-System programming (ISP) of an EEPROM connected to HX3 through USB

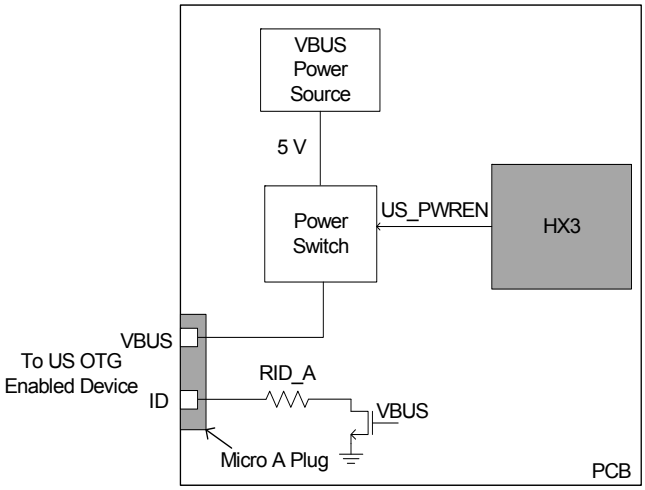
ACA-Dock Support

In traditional USB topologies, the host provides VBUS to enable and charge the connected devices. For OTG hosts, however, an ACA-Dock provides VBUS and a method to charge the host. HX3 supports the ACA-Dock standard (see BC v1.2 specification) by integrating the functions of the adapter controller.

Figure 5 shows the ACA-Dock system. If the ACA-Dock feature is enabled, HX3 turns on the external power switch to drive VBUS on the US port. To inform the OTG host that it is connected to an ACA-Dock, the ID pin is tied to ground using a resistor RID_A,[3] as shown in Figure 5. The ACA-Dock feature can be disabled using the Configuration Options on page 24.

For example, a BC v1.2 compliant phone such as a Sony Xperia (neo V) can be docked to a HX3-based ACA-Dock system. The phone acts as an OTG host and the ACA-Dock charges the phone connected to the US port while also powering the four DS ports.

Figure 5. ACA-Dock Support



Note
3. 124 kΩ is the recommended RID_A value as per BC v1.2 specification, but some portable devices use custom RID_A values.

Pin Information

Figure 6. HX3 68-Pin QFN 2-Port Pinout

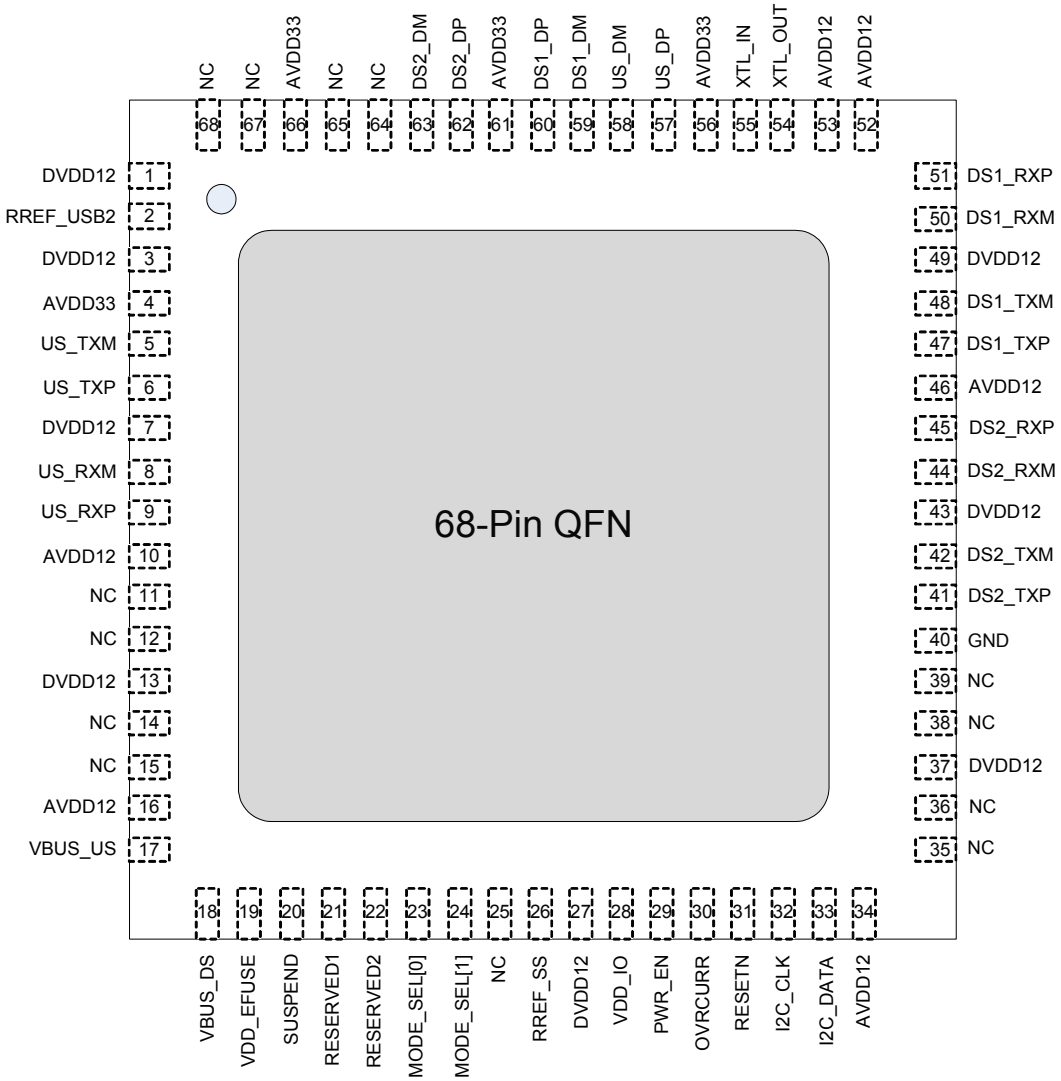


Table 2. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB3302 and CYUSB3304 *(continued)*

Pin Name		Type	68-QFN Pin#	100-BGA Ball #	Description
CYUSB3302	CYUSB3304				
RESERVED1		I/O	21	G4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
RESERVED2		I	22	H4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
Mode Select, Clock, and Reset					
MODE_SEL[0]		I	23	G5	Device operation mode select bit 0; refer to Table 5 on page 24
MODE_SEL[1]		I	24	F4	Device operation mode select bit 1; refer to Table 5 on page 24
XTL_OUT		A	54	E6	Crystal out
XTL_IN		A	55	E5	Crystal in
RESETN		I	31	F7	Active LOW reset input
I2C_CLK		I/O	32	J6	I^2C clock
I2C_DATA		I/O	33	G8	I^2C data
SUSPEND		I/O	20	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and Ground					
VDD_EFUSE		PWR	19	H3	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V.
AVDD12		PWR	10, 16, 34, 46, 52, 53	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND		PWR	40	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12		PWR	1, 3, 7, 13, 27, 37, 43, 49,	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS _US		PWR	17	H2	This pin must be connected to VBUS from US port
VBUS_DS		PWR	18	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	4, 56, 61, 66	A4, A7, B6, F3	3.3 V analog supply
VDD_IO		PWR	28	B4, E7, G6	3.3 V I/O supply
USB Precision Resistors					
RREF_USB2		A	2	E2	Connect pin to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY.
RREF_SS		A	26	H5	Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration.

Note
4. These pins are Do Not Use (DNU); they must be left floating.

Table 3. 68-Pin QFN, 100-Ball BGA Pinout for CYUSB2302 and CYUSB2304 *(continued)*

Pin Name		Type	68-QFN Pin#	100-BGA Ball #	Description
CYUSB2302	CYUSB2304				
RESERVED1		I/O	21	G4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
RESERVED2		I	22	H4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
Mode Select, Clock, and Reset					
MODE_SEL[0]		I	23	G5	Device operation mode select bit 0; refer to Table 5 on page 24
MODE_SEL[1]		I	24	F4	Device operation mode select bit 1; refer to Table 5 on page 24
XTL_OUT		A	54	E6	Crystal out
XTL_IN		A	55	E5	Crystal in
RESETN		I	31	F7	Active LOW reset input
I2C_CLK		I/O	32	J6	I^2C clock
I2C_DATA		I/O	33	G8	I^2C data
SUSPEND		I/O	20	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and Ground					
VDD_EFUSE		PWR	19	H3	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V.
AVDD12		PWR	10, 16, 34, 46, 52, 53	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND		PWR	40	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12		PWR	1, 3, 7, 13, 27, 37, 43, 49,	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS _US		PWR	17	H2	This pin must be connected to VBUS from US port
VBUS_DS		PWR	18	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	4, 56, 61, 66	A4, A7, B6, F3	3.3 V analog supply
VDD_IO		PWR	28	B4, E7, G6	3.3 V I/O supply
USB Precision Resistors					
RREF_USB2		A	2	E2	Connect pin to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY.
RREF_SS		A	26	H5	Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration.

Figure 10. HX3 88-Pin QFN 2-Port Pinout

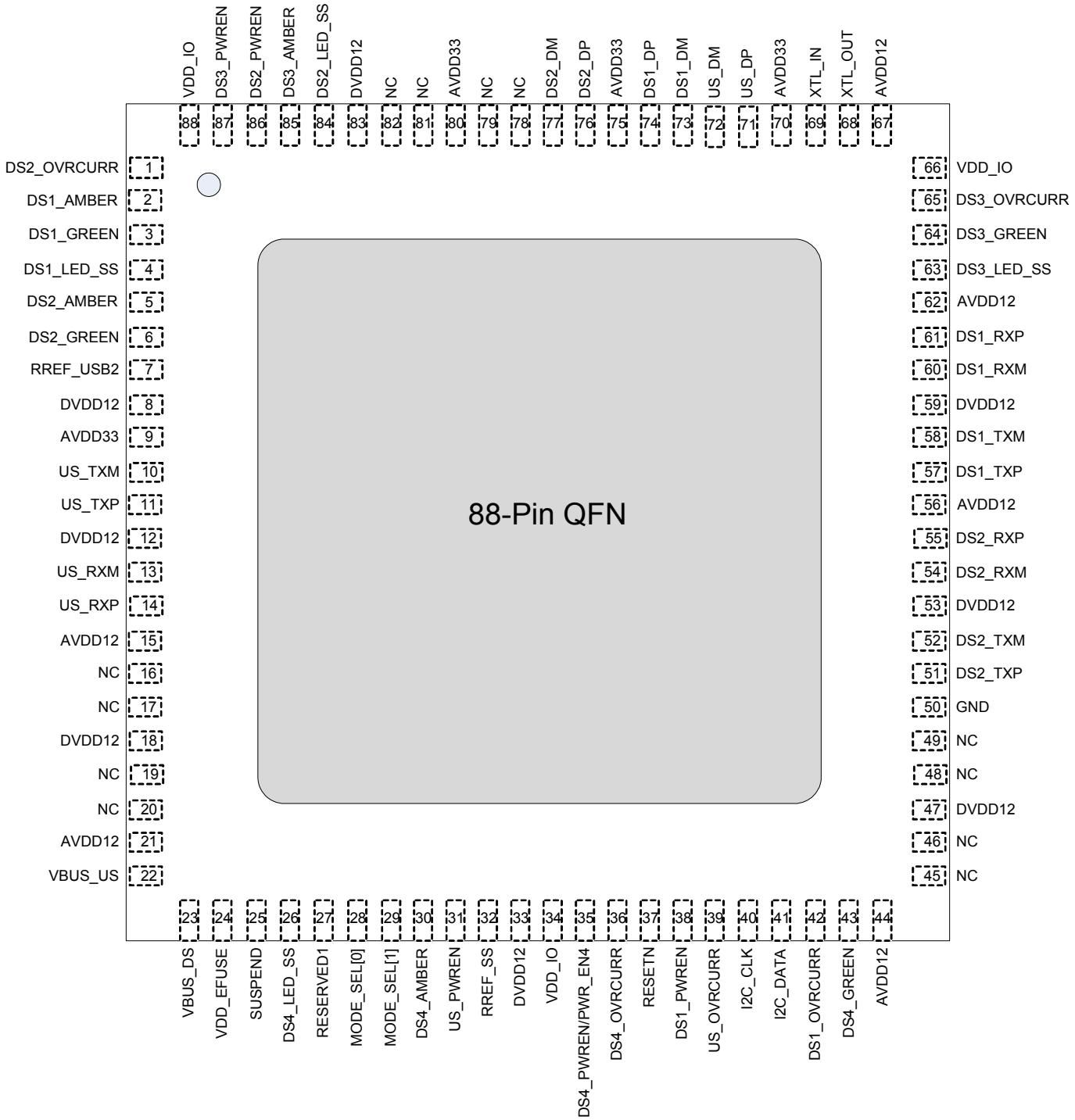


Figure 12. HX3 100-Ball BGA Pinout for CYUSB3312

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
DS3_PWREN	NC	NC	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**	**B9**	**B10**
DS2_OVRCURR	DS2_PWREN	DS3_AMBER	VDD_IO	VSS	AVDD33	DS3_OVRCURR	DS3_GREEN	DS3_LED_SS	DVDD12
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**
US_TXM	DS1_AMBER	DS2_LED_SS	NC	NC	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**	**D9**	**D10**
US_TXP	DS1_LED_SS	DS1_GREEN	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**	**E8**	**E9**	**E10**
DVDD12	RREF_USB2	DS2_GREEN	DS2_AMBER	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**	**F9**	**F10**
US_RXM	VSS	AVDD33	MODE_SEL[1]	DVDD12	DS4_OVRCURR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**	**G9**	**G10**
US_RXP	VBUS_DS	SUSPEND	RESERVED1	MODE_SEL[0]	VDD_IO	DS4_PWREN	I2C_DATA	VSS	DS2_RXM
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**	**H9**	**H10**
AVDD12	VBUS_US	VDD_EFUSE	DS4_LED_SS	RREF_SS	VSS	DS2_TXM	DS2_TXP	DS4_GREEN	AVDD12
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**	**J10**
VSS	AVDD12	VSS	DS4_AMBER	US_PWREN	I2C_CLK	DS1_PWREN	DS1_OVRCURR	VSS	NC
K1	**K2**	**K3**	**K4**	**K5**	**K6**	**K7**	**K8**	**K9**	**K10**
NC	NC	DVDD12	NC	NC	US_OVRCURR	NC	NC	DVDD12	NC

Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314 CYUSB3324 CYUSB3326 CYUSB3328				
US Port					
US_RXP		I	14	G1	SuperSpeed receive plus
US_RXM		I	13	F1	SuperSpeed receive minus
US_TXP		O	11	D1	SuperSpeed transmit plus
US_TXM		O	10	C1	SuperSpeed transmit minus
US_DP		I/O	71	A9	USB 2.0 data plus
US_DM		I/O	72	A8	USB 2.0 data minus
US_OVRCURR		I	39	K6	CYUSB3324/3328: Overcurrent detect input for US port in ACA-Dock mode. If ACA-Dock mode is disabled using Configuration Options on page 24, this pin must be pulled HIGH using a 10 kΩ to VDD_IO. Other part numbers: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
US_PWREN[5]		I/O	31	J5	CYUSB3324/3328: VBUS power enable output for US port in ACA-Dock mode. If ACA-Dock mode is disabled using Configuration Options on page 24, this pin can be left floating if Pin-Strap is not enabled. Other part numbers: This pin can be left floating if Pin-Strap (Pin# 63) is not enabled.
PWR_SW_POL[6]					This pin is called PWR_SW_POL in pin-strap configuration mode.
DS1 Port					
DS1_RXP		I	61	D10	SuperSpeed receive plus
DS1_RXM		I	60	C10	SuperSpeed receive minus
DS1_TXP		O	57	F8	SuperSpeed transmit plus
DS1_TXM		O	58	E8	SuperSpeed transmit minus
DS1_DP		I/O	74	C7	USB 2.0 data plus
DS1_DM		I/O	73	C8	USB 2.0 data minus
DS1_OVRCURR		I	42	J8	Overcurrent detect input for DS1 port
DS1_PWREN[5]		I/O	38	J7	VBUS power enable output for DS1 port. When the port is disabled, this pin is in tristate.
DS1_CDP_EN[6]					This pin is called DS1_CDP_EN in pin-strap configuration mode.
DS1_AMBER[5]		I/O	2	C2	LED_AMBER output for DS1 port
ACA_DOCK[6]					This pin is called ACA-DOCK in pin-strap configuration mode.
DS1_GREEN[5]		I/O	3	D3	CYUSB3312/3314/3324: LED_GREEN output for DS1 port
DS1_VBUSEN_SL[5]					CYUSB3326/3328: VBUS power enable output for SS port 1
PORT_DISABLE[0][6]					This pin is called PORT_DISABLE[0] in pin-strap configuration mode.
DS1_LED_SS[5]		I/O	4	D2	LED_SS output for DS1 port
PORT_DISABLE[1][6]					This pin is called PORT_DISABLE[1] in pin-strap configuration mode.

Notes
5. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
6. For pin-strap configuration details, refer to Table 6 on page 25.

Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X *(continued)*

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314 CYUSB3324 CYUSB3326 CYUSB3328				
DS2 Port					
DS2_RXP		I	55	F10	SuperSpeed receive plus
DS2_RXM		I	54	G10	SuperSpeed receive minus
DS2_TXP		O	51	H8	SuperSpeed transmit plus
DS2_TXM		O	52	H7	SuperSpeed transmit minus
DS2_DP		I/O	76	A6	USB 2.0 data plus
DS2_DM		I/O	77	A5	USB 2.0 data minus
DS2_OVRCURR		I	1	B1	Overcurrent detect input for DS2 port
DS2_PWREN[7]		I/O	86	B2	VBUS power enable output for DS2 port. When the port is disabled, this pin is in tristate.
DS2_CDP_EN[8]					This pin is called DS2_CDP_EN in the pin-strap configuration mode.
DS2_AMBER[7]		I/O	5	E4	LED_AMBER output for DS2 port
NON_REMOVABLE[0][8]					This pin is called NON_REMOVABLE[0] in the pin-strap configuration mode.
DS2_GREEN[7]		I/O	6	E3	CYUSB3312/3314/3324: LED_GREEN output for DS2 port
DS2_VBUSEN_SL[7]					CYUSB3326/3328: VBUS power enable output for SS port 2
NON_REMOVABLE[1][8]					This pin is called NON_REMOVABLE[1] in the pin-strap configuration mode.
DS2_LED_SS[7]		I/O	84	C3	LED_SS output for DS2 port
PWR_EN_SEL[8]					This pin is called PWR_EN_SEL in the pin-strap configuration mode.
DS3 Port					
NC	DS3_RXP	I	45	K10	SuperSpeed receive plus
NC	DS3_RXM	I	46	J10	SuperSpeed receive minus
NC	DS3_TXP	O	48	K7	SuperSpeed transmit plus
NC	DS3_TXM	O	49	K8	SuperSpeed transmit minus
NC	DS3_DP	I/O	79	C4	USB 2.0 data plus
NC	DS3_DM	I/O	78	C5	USB 2.0 data minus
DS3_OVRCURR		I	65	B7	CYUSB3314/3324/3326/3328: Overcurrent detect input for DS3 port CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
DS3_PWREN[7]		I/O	87	A1	VBUS power enable output for DS3 port. When the port is disabled, this pin is in tristate.
DS3_CDP_EN[8]					This pin is called DS3_CDP_EN in the pin-strap configuration mode.
DS3_AMBER[7]		I/O	85	B3	LED_AMBER output for DS3 port
VID_SEL[2][8]					This pin is called VID_SEL[2] in the pin-strap configuration mode.

Notes
7. This pin can be configured as a GPIO using custom firmware. For information contact www.cypress.com/support.
8. For pin-strap configuration details, refer to Table 6 on page 25.

Table 4. 88-Pin QFN, 100-Ball BGA Pinout for CYUSB331X and CYUSB332X *(continued)*

Pin Name		Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314 CYUSB3324 CYUSB3326 CYUSB3328				
SUSPEND		I/O	25	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and Ground					
VDD_EFUSE		PWR	24	H3	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V
AVDD12		PWR	15, 21, 44, 56, 62, 67	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND		PWR	50	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12		PWR	8, 12, 18, 33, 47, 53, 59, 83	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS _US		PWR	22	H2	CYUSB3324/3328: Connect the VBUS_US pin to the local 5 V supply. If ACA-Dock mode is disabled using Configuration Options on page 24, this pin must be connected to VBUS from US port. Other part numbers: This pin must be connected to VBUS from US port.
VBUS_DS		PWR	23	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	9, 70, 75, 80	A4, A7, B6, F3	3.3 V analog supply
VDD_IO		PWR	34, 66, 88	B4, E7, G6	3.3 V I/O supply
USB Precision Resistors					
RREF_USB2		A	7	E2	Connect pin to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY.
RREF_SS		A	32	H5	Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration.

Table 7. EEPROM Map *(continued)*

I²C Offset	Bits	Name	Default	Description
23	7:6	HS_AMPLITUDE_DS4	b'00	HS driver amplitude control; HS driver current: +0% to +7.5% b'00: Default b'01: +2.5% b'10: +5% b'11: +7.5%
	5:4	HS_AMPLITUDE_DS3	b'00	
	3:2	HS_AMPLITUDE_DS2	b'00	
	1:0	HS_AMPLITUDE_DS2	b'00	
24	7:6	HS_AMPLITUDE_US	b'00	
	5:2	HS_SLOPE	b'0100	HS driver slope control for all ports b'0000: +15% b'0001: +5% b'0100: Default b'0101: -5% b'1111: -7.5%
	1:0	HS_TX_VREF	b'10	Reference voltage for HS squelch (transmission envelope detector) for all ports b'00: 96 mV b'01: 108 mV b'10: 120 mV b'11: 132 mV
25	7:3	HS_PREEMP_EN[4:0]	b'00000	HS driver pre-emphasis enable – for ports DS4, DS3, DS2, DS1, and US 0: pre-emphasis is disabled 1: pre-emphasis is enabled
	2	HS_PREEMP_DEPTH_DS4[17]	0	HS driver pre-emphasis depth 0: +10% 1: +20%
	1	HS_PREEMP_DEPTH_DS3[17]	0	
	0	HS_PREEMP_DEPTH_DS2[17]	0	
26	7	HS_PREEMP_DEPTH_DS1[17]	0	
	6	HS_PREEMP_DEPTH_US[17]	0	
	5	Reserved	1	Reserved
	4:1	PCS_TX_DEEMPH_DS4	0x6	USB 3.0 Tx driver de-emphasis value 0x3: -2.75 dB 0x6: -3.4 dB (Default) 0x9: -4.0 dB
	0	Reserved	0	Reserved
27	7:4	PCS_TX_DEEMPH_DS3	0x6	USB 3.0 Tx driver de-emphasis value 0x3: -2.75 dB 0x6: -3.4 dB (Default) 0x9: -4.0 dB
	3:0	PCS_TX_DEEMPH_DS2	0x6	
28	7:4	PCS_TX_DEEMPH_DS1	0x6	
	3:0	PCS_TX_DEEMPH_US	0x6	
29	7	Reserved	0	Reserved
	6	Reserved	1	Reserved
	5:0	PCS_TX_SWING_FULL_DS4	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
30	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_DS3	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V

Note
17. HS_PREEMP_DEPTH is valid only when corresponding HS_PREEMP_EN is set for that port.

Table 7. EEPROM Map *(continued)*

I²C Offset	Bits	Name	Default	Description
31	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_DS2	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
32	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_DS1	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
33	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_US	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
34	7:0	Reserved	0	Reserved
35	7:0	UHC_PID [7:0]_LSB	0x06	USB 2.0 PID. If bD4Length ≥ 40, USB 2.0 PID will be read from this location.
36	7:0	UHC_PID [15:8]_MSB	0x65	
37–44	7:0	Reserved	0	Eight bytes reserved for future expansion
45	7:0	bLength: LangID	4	Size of LangID (defined by spec as N+2)
46	7:0	DescType	3	String descriptor type (constant value)
47	7:0	LangID - MSB	9	String language ID - MSB of wLangID
48	7:0	LangID - LSB	4	String language ID - MSB of wLangID
49	7:0	bLength: Manufacturer (X)	54	Manufacturer string length (“bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number” should be less than or equal to 152 bytes). X ≤ 66.
50	7:0	DescType	3	String descriptor type (constant value)
51	7:0	bString: Manufacturer	‘2’, 0, ‘0’, 0, ‘1’, 0, ‘4’, 0, ‘ ‘, 0, ‘C’, 0, ‘y’, 0, ‘p’, 0, ‘r’, 0, ‘e’, 0, ‘s’, 0, ‘s’, 0, ‘ ‘, 0, ‘S’, 0, ‘e’, 0, ‘m’, 0, ‘i’, 0, ‘c’, 0, ‘o’, 0, ‘n’, 0, ‘d’, 0, ‘u’, 0, ‘c’, 0, ‘t’, 0, ‘o’, 0, ‘r’, 0	Manufacturer string: UNICODE UTF-16LE per USB 2.0 specification: “2014 Cypress Semiconductor”
49 + X	7:0	bLength: Product (Y)	22	Product string length (“bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number” should be less than or equal to 152 bytes). Y ≤ 66.
50 + X	7:0	DescType	3	String descriptor type (constant value)

Table 7. EEPROM Map *(continued)*

I²C Offset	Bits	Name	Default	Description
51 + X	7:0	bString: Product	'C', 0, 'Y', 0, '-', 0, 'H', 0, 'X', 0, '3', 0, ' ', 0, 'H', 0, 'U', 0, 'B', 0	Product string: UNICODE UTF-16LE per USB 2.0 specification: "CY-HX3 HUB"
49 + X + Y	7:0	bLength: Serial Number (Z)	22	Serial number string length ("bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number" should be less than or equal to 152 bytes). Z ≤ 66.
50 + X + Y	7:0	DescType	3	String descriptor type (constant value)
51 + X + Y	7:0	bString: Serial Number	'1', 0, '2', 0, '3', 0, '4', 0, '5', 0, '6', 0, '7', 0, '8', 0, '9', 0, 'A', 0	Serial number string: UNICODE UTF-16LE per USB 2.0 specification: "123456789A"

EMI

HX3 meets the EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. HX3 tolerates EMI conducted by aggressors outlined by the above specifications and continues to function as expected.

ESD

HX3 has a built-in ESD protection on all pins. The ESD protection level provided on these ports is 2.2 kV Human Body Model (HBM) based on the JESD22-A114 specification.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature..... –65 °C to +150 °C

Operating temperature ..... –40 °C to +85 °C

Electrostatic discharge voltage ..... 2200 V

Oscillator or crystal frequency ..... 26 MHz ±150 ppm

I/O voltage supply .....3 V to 3.6 V

Maximum input sink current per I/O ..... 4 mA

Electrical Specifications

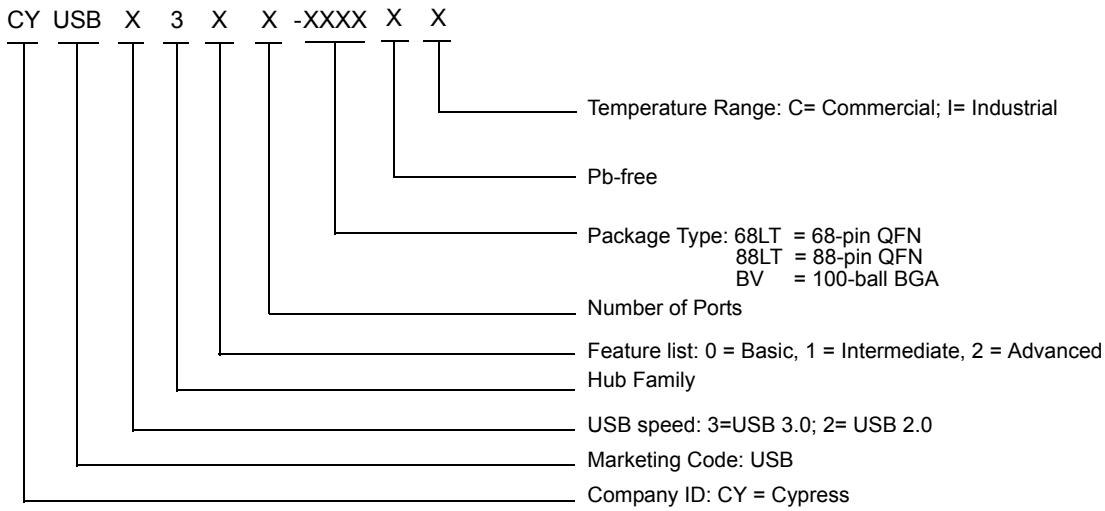
HX3 meets all USB-IF Electrical Compliance specifications.

DC Electrical Characteristics

Table 8. DC Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
DVDD12	1.2 V core supply	–	1.14	1.2	1.26	V
VDD_EFUSE	eFuse supply	Normal operation	1.14	1.2	1.26	V
		Programming	2.5	2.6	2.7	V
AVDD12	1.2 V analog supply	–	1.14	1.2	1.26	V
VDD_IO	3.3 V I/O supply	–	3	3.3	3.6	V
AVDD33	3.3 V analog supply	–	3	3.3	3.6	V
V_{IH}	Input HIGH voltage	–	0.7 × VDD_IO	–	VDD_IO	V
V_{IL}	Input LOW voltage	–	0	–	0.3 × VDD_IO	V
V_{OH}	Output HIGH voltage	Output HIGH voltage at $I_{OH} \leq +4$ mA	2.4	–	–	V
V_{OL}	Output LOW voltage	Output LOW voltage at $I_{OL} \geq -4$ mA	–	–	0.4	V
I_{OS}	Input sink current	LED GPIO usage	–	–	4	mA
I_{IX}	Input leakage current	All I/O signals held at VDD_IO or GND	–1	–	1	µA
I_{OZ}	Output HI-Z leakage current	–	–	–	10	µA
I_{CC}	1.2 V supplies combined operating current	–	–	410	526	mA
I_{CC}	3.3 V supplies combined operating current	–	–	260	286	mA
V_{RAMP}	Voltage ramp rate on core and I/O supplies	Voltage ramp must be monotonic	0.2	–	50	V/ms
V_N	Noise level permitted on core and I/O supplies	Max p-p noise level permitted on all supplies except AVDD	–	–	100	mV
V_{N_USB}	Noise level permitted on AVDD12 and AVDD33 supply	Max p-p noise level permitted USB supply	–	–	20	mV

Ordering Code Definitions



Packaging

Table 12. Package Characteristics

Parameter	Description	Min	Typ	Max	Units
T_A	Operating ambient temperature	–40	–	85	°C
T_J	Operating junction temperature	–40	–	125	°C
T_{JA}	Package J_A (68-pin QFN)	–	16.2	–	°C/W
T_{JA}	Package J_A (88-pin QFN)	–	15.7	–	°C/W
T_{JA}	Package J_A (100-ball BGA)	–	35	–	°C/W
T_{JC}	Package J_C (68-pin QFN)	–	23.8	–	°C/W
T_{JC}	Package J_C (88-pin QFN)	–	18.9	–	°C/W
T_{JC}	Package J_C (100-ball BGA)	–	12	–	°C/W

Table 13. Solder Reflow Peak Temperature

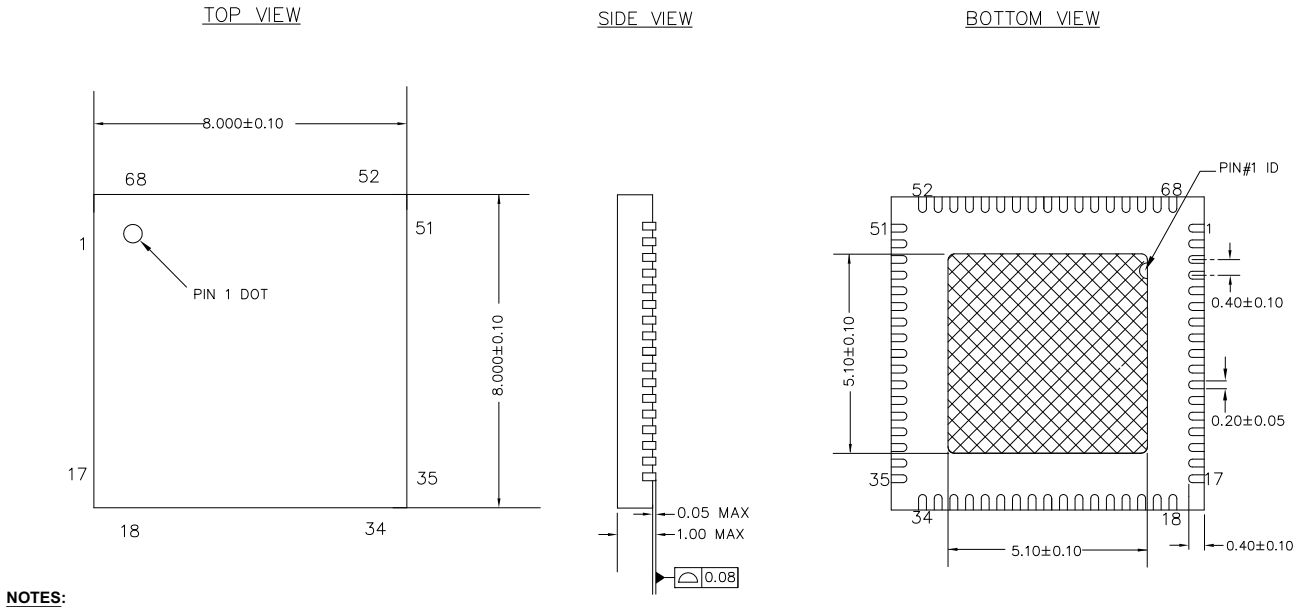
Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
68-pin QFN	260 °C	30 seconds
88-pin QFN	260 °C	30 seconds
100-ball BGA	260 °C	30 seconds

Table 14. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
68-pin QFN	MSL 3
88-pin QFN	MSL 3
100-ball BGA	MSL 3

Package Diagrams

Figure 18. 68-pin QFN (8 × 8 × 1.0 mm) LT68B 5.1 × 5.1 mm EPAD (Sawn) Package Outline

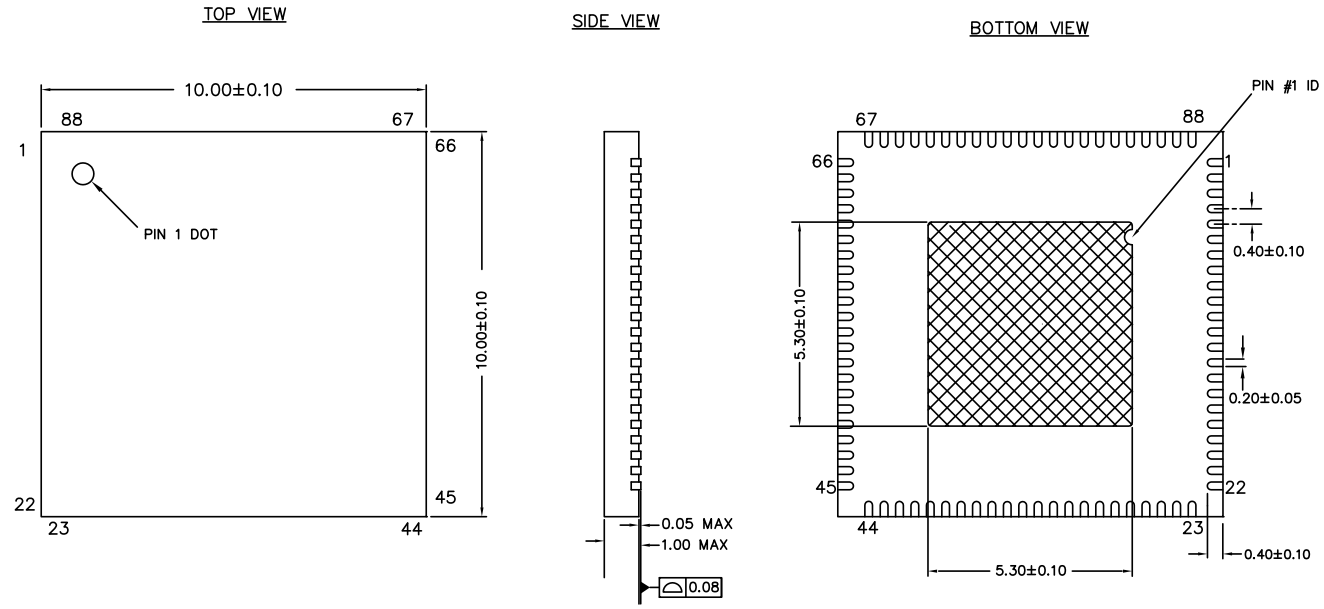


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC#: MO-220
3. ALL DIMENSIONS ARE IN MILLIMETERS

001-78925 *B

Figure 19. 88-pin QFN (10 × 10 × 1.0 mm) LT88B 5.3 × 5.3 EPAD (Sawn) Package Outline



001-76569 *B

Silicon Revision History

This datasheet is applicable for the USB-IF certified (TID# 330000060) HX3 Rev. *D and Rev. *C Silicon.

Rev. *D: This Silicon revision improves the yield of HX3, and is drop-in compatible for all the part numbers. There is no need to change the board design or layout to use the HX3 Rev. *D Silicon. Products are completely compatible with the HX3 Rev. *C Silicon.

Rev. *C: This Silicon revision fixes the errata applicable to the Rev. *A Silicon.

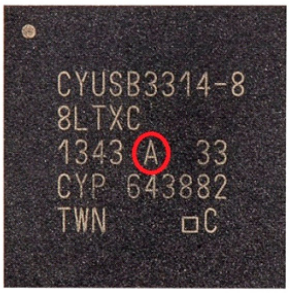
The following table defines the changes between Rev. *A, Rev. *C, and Rev. *D Silicon.

No.	Items	Part Numbers	Rev. *A	Rev. *C	Rev. *D
1	USB-IF Compliance	All	Requires firmware on external EEPROM	No external EEPROM required	No external EEPROM required
2	FS-only hub or host connected to HX3 Upstream Port	All	Not supported	Supported	Supported
3	Suspend Power	All	90 mW	37.8 mW	37.8 mW

Method of Identification

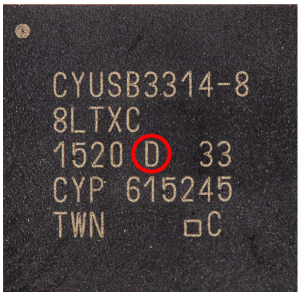
Markings on row 3 of the HX3 package differentiate Rev. *D Silicon from Rev. *C Silicon and Rev. *A Silicon as indicated in the example below. Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

HX3 REV *A SILICON



HX3 REV *C SILICON

HX3 REV *D SILICON



Document History Page

Document Title: CYUSB330x/CYUSB331x/CYUSB332x/CYUSB230x, HX3 USB 3.0 Hub Document Number: 001-73643				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	4271496	MURT	02/21/2014	Changed status from Preliminary to Final.
*F	4291210	MURT	02/25/2014	Post to external web.
*G	4308926	MURT	03/14/2014	Updated System Interfaces: Updated Configuration Options: Updated HX3 as I2C Slave: Updated Table 7.
*H	4463533	MURT	08/01/2014	Updated Features: Updated TID#. Updated Electrical Specifications: Updated Power Consumption: Updated Table 9: Updated details corresponding to suspend power. Removed Errata.
*I	4483117	RAJM	08/22/2014	Added Silicon Revision History.
*J	4499514	RAJM	09/15/2014	Added BGA package information.
*K	4582512	PRJI	11/28/2014	Updated HX3 Product Options: Updated Table 1. Updated Pin Information: Updated Table 4.
*L	4632890	HBM	01/20/2015	Updated Pin Information: Updated Figure 12. Updated Figure 13. Updated Table 4. Added Packaging. Updated Package Diagrams: spec 51-85209 – Changed revision from *D to *E.
*M	4669639	HBM	02/24/2015	No technical updates. Completing Sunset Review.
*N	4764583	HBM	05/13/2015	Updated Package Diagrams: spec 001-76569 – Changed revision from *A to *B. Updated Silicon Revision History. Updated Method of Identification.
*O	4941772	HBM	11/25/2015	Updated HX3 Product Options: Updated Table 1: Included CYUSB2302-68LTXI and CYUSB2304-68LTXI part numbers related information. Updated Ordering Information: Updated Table 11: Updated part numbers.
*P	5466603	HBM	10/20/2016	Updated Features: Replaced “USB 3.0-Certified Hub, TID# 330000060” with “USB-IF Certified Hub, TID# 330000060, 30000074”. Updated Package Diagrams: spec 51-85209 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.

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