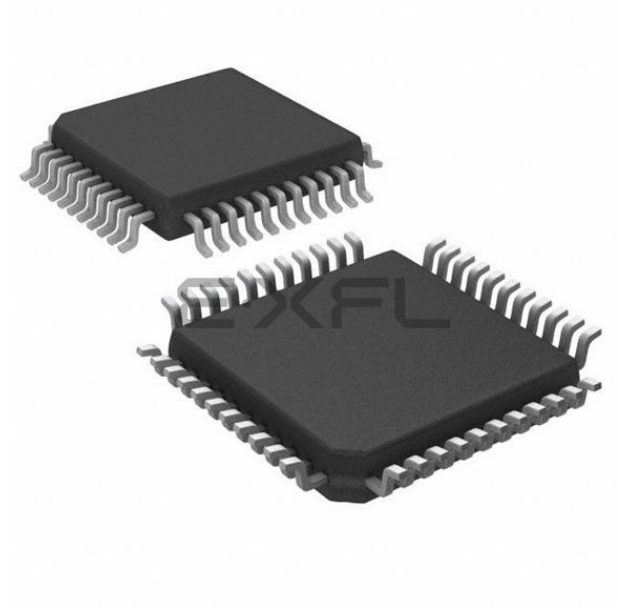

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Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	2MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	26
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-QFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68711d3cfbe2

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Central Processor Unit (CPU)

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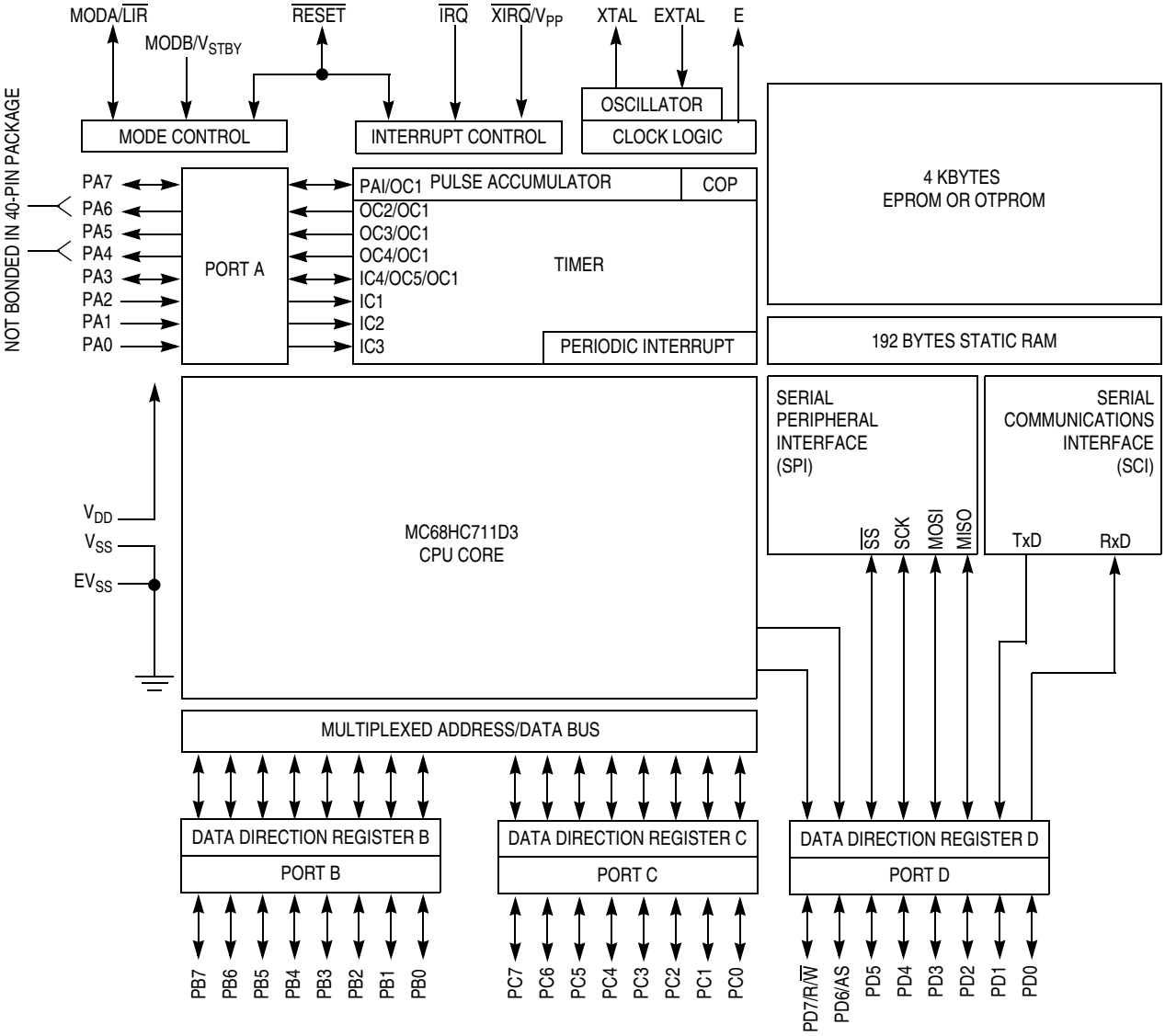


Figure 1-1. MC68HC711D3 Block Diagram

1.4 Pin Descriptions

Refer to Figure 1-2, Figure 1-3, and Figure 1-4 for pin assignments.

Table 2-2. Bootstrap Mode Jump Vectors (Continued)

Address	Vector
00EB	Real-time interrupt
00EE	IRQ
00F1	XIRQ
00F4	SWI
00F7	Illegal opcode
00FA	COP fail
00FD	Clock monitor
BF00 (Boot)	Reset

2.2.4 Special Test Mode

This special expanded mode is primarily intended or production testing. The user can access a number of special test control bits in this mode. Reset and interrupt vectors are fetched externally from locations $BFC0–$BFFF. A switch can be made from this mode to other modes under program control.

2.3 Memory Map

Figure 2-1 illustrates the memory map for both normal modes of operation (single-chip and expanded-multiplexed), as well as for both special modes of operation (bootstrap and test).

- In the single-chip mode, the MCU does not generate external addresses. The internal memory locations are shown in the shaded areas, and the contents of these shaded areas are explained on the right side of the diagram.
- In expanded-multiplexed mode, the memory locations are basically the same as in the single-chip mode except that the memory locations between shaded areas are for externally addressed memory and I/O.
- The special bootstrap mode is similar to the single-chip mode, except that the bootstrap program ROM is located at memory locations $BF00–$BFFF, vectors included.
- The special test mode is similar to the expanded-multiplexed mode except the interrupt vectors are at external memory locations.

2.3.1 Control and Status Registers

Figure 2-2 is a representation of all 64 bytes of control and status registers, I/O and data registers, and reserved locations that make up the internal register block. This block may be mapped to any 4-K boundary in memory, but reset locates it at $0000–$003F. This mappability factor and the default starting addresses are indicated by the use of a bold **0** as the starting character of a register's address.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003A	Arm/Reset COP Timer Circuitry Register (COPRST) See page 48.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$003B	PROM Programming Control Register (PPROG) See page 32.	Read: Write:	MBE	0	ELAT	EXCOL	EXROW	0	0	PGM
		Reset:	0	0	0	0	0	0	0	0
$003C	Highest Priority I-Bit Interrupt and Miscellaneous Register (HPRIO) See page 58.	Read:	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0
		Write:								
		Reset:	Note 1				0	1	0	1

1. The values of the RBOOT, SMOD, IRVNE, and MDA bits at reset depend on the mode during initialization. Refer to Table 4-3. Hardware Mode Select Summary.

$003D	RAM and I/O Mapping Register (INIT) See page 29.	Read: Write:	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
		Reset:	0	0	0	0	0	0	0	1
$003E	Test 1 Register (TEST)	Read: Write:	TILOP	0	OCC4	CBYP	DISR	FCM	FCOP	0
		Reset:	0	0	0	0	0	0	0	0
$003F	System Configuration Register (CONFIG) See page 30.	Read: Write:	0	0	0	0	0	NOCOP	ROMON	0
		Reset:	0	0	0	0	0	U	U	0

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Register and Control Bit Assignments (Sheet 5 of 5)

2.3.2 RAM and I/O Mapping Register

The random-access memory (RAM) and input/output (I/O) mapping register (INIT) is a special-purpose 8-bit register that is used during initialization to change the default locations of RAM and control registers within the MCU memory map. It can be written to only once within the first 64 E-clock cycles after a reset in normal modes. Thereafter, it becomes a read-only register.

Address: $003D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
Reset:	0	0	0	0	0	0	0	0

Figure 2-3. RAM and I/O Mapping Register (INIT)

ROMON — PROM Enable Bit

This bit is set out of reset, enabling the EPROM or OTPROM in all modes. This bit is writable once in normal modes (SMOD = 0), but is writable at any time in special modes (SMOD = 1).

1 = PROM is present in the memory map.

0 = PROM is disabled from the memory map.

NOTE

In expanded mode out of reset, the EPROM or OTPROM is located at $7000–$7FFF. In all other modes, the PROM resides at $F000–$FFFF.

2.4 Programmable Read-Only Memory (PROM)

The MC68HC711D3 has 4-Kbytes of one-time programmable read-only memory (OTPROM). The PROM address is $F000–$FFFF in all modes except expanded multiplexed. In expanded- multiplexed mode, the PROM is located at $7000–$7FFF after reset.

The on-chip read-only memory (ROM) of an MC68HC711D3 is programmed in MCU mode. In this mode, the PROM is programmed through the MCU in the bootstrap or test modes. The erased state of a PROM byte is $FF.

Using the on-chip OTPROM programming feature requires an external 12-volt nominal power supply (V_{PP}). Normal programming is accomplished using the OTPROM programming register (PPROG).

As described in the following subsections, these two methods of programming and verifying EPROM are possible:

1. Programming an individual EPROM address
2. Programming the EPROM with downloaded data

2.4.1 Programming an Individual EPROM Address

In this method, the MCU programs its own EPROM by controlling the PPROG register. Use these procedures to program the EPROM through the MCU with:

- The ROMON bit set in the CONFIG register
- The 12-volt nominal programming voltage present on the $\overline{XIRQ}/V_{PP}$ pin
- The $\overline{IRQ}$ pin must be pulled high.

```
EPROG   LDAB    #$20
        STAB    $003B   Set ELAT bit (PGM = 0) to enable
                        EPROM latches.
        STAA    $0,X    Store data to EPROM address
        LDAB    #$21
        STAB    $003B   Set PGM bit with ELAT = 1 to enable
                        EPROM programming voltage
        JSR     DLYEP   Delay 2-4 ms
        CLR     $003B   Turn off programming voltage and set
                        to READ mode
```

3.2.6.4 Negative (N)

The N bit is set if the result of an arithmetic, logic, or data manipulation operation is negative (MSB = 1). Otherwise, the N bit is cleared. A result is said to be negative if its most significant bit (MSB) is a 1. A quick way to test whether the contents of a memory location has the MSB set is to load it into an accumulator and then check the status of the N bit.

3.2.6.5 I-Interrupt Mask (I)

The interrupt request (IRQ) mask (I bit) is a global mask that disables all maskable interrupt sources. While the I bit is set, interrupts can become pending, but the operation of the CPU continues uninterrupted until the I bit is cleared. After any reset, the I bit is set by default and can be cleared only by a software instruction. When an interrupt is recognized, the I bit is set after the registers are stacked, but before the interrupt vector is fetched. After the interrupt has been serviced, a return-from-interrupt instruction is normally executed, restoring the registers to the values that were present before the interrupt occurred. Normally, the I bit is 0 after a return from interrupt is executed. Although the I bit can be cleared within an interrupt service routine, "nesting" interrupts in this way should be done only when there is a clear understanding of latency and of the arbitration mechanism. Refer to Chapter 4 Resets, Interrupts, and Low-Power Modes.

3.2.6.6 Half Carry (H)

The H bit is set when a carry occurs between bits 3 and 4 of the arithmetic logic unit during an ADD, ABA, or ADC instruction. Otherwise, the H bit is cleared. Half carry is used during BCD operations.

3.2.6.7 X-Interrupt Mask (X)

The XIRQ mask (X) bit disables interrupts from the $\overline{\text{XIRQ}}$ pin. After any reset, X is set by default and must be cleared by a software instruction. When an $\overline{\text{XIRQ}}$ interrupt is recognized, the X and I bits are set after the registers are stacked, but before the interrupt vector is fetched. After the interrupt has been serviced, an RTI instruction is normally executed, causing the registers to be restored to the values that were present before the interrupt occurred. The X interrupt mask bit is set only by hardware ($\overline{\text{RESET}}$ or $\overline{\text{XIRQ}}$ acknowledge). X is cleared only by program instruction (TAP, where the associated bit of A is 0; or RTI, where bit 6 of the value loaded into the CCR from the stack has been cleared). There is no hardware action for clearing X.

3.2.6.8 STOP Disable (S)

Setting the STOP disable (S) bit prevents the STOP instruction from putting the M68HC11 into a low-power stop condition. If the STOP instruction is encountered by the CPU while the S bit is set, it is treated as a no-operation (NOP) instruction, and processing continues to the next instruction. S is set by reset; STOP is disabled by default.

3.3 Data Types

The M68HC11 CPU supports four data types:

1. Bit data
2. 8-bit and 16-bit signed and unsigned integers
3. 16-bit unsigned fractions
4. 16-bit addresses

Table 3-2. Instruction Set (Sheet 4 of 8)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
COMA	Ones Complement A	$FF – A ⇒ A	A INH	43	—	2	—	—	—	—	Δ	Δ	0	1
COMB	Ones Complement B	$FF – B ⇒ B	B INH	53	—	2	—	—	—	—	Δ	Δ	0	1
CPD (opr)	Compare D to Memory 16-Bit	D – M : M + 1	IMM DIR EXT IND,X IND,Y	1A 83 1A 93 1A B3 1A A3 CD A3	jj kk dd hh ll ff ff	5 6 7 7 7	—	—	—	—	Δ	Δ	Δ	Δ
CPX (opr)	Compare X to Memory 16-Bit	IX – M : M + 1	IMM DIR EXT IND,X IND,Y	8C 9C BC AC CD AC	jj kk dd hh ll ff ff	4 5 6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
CPY (opr)	Compare Y to Memory 16-Bit	IY – M : M + 1	IMM DIR EXT IND,X IND,Y	18 8C 18 9C 18 BC 1A AC 18 AC	jj kk dd hh ll ff ff	5 6 7 7 7	—	—	—	—	Δ	Δ	Δ	Δ
DAA	Decimal Adjust A	Adjust Sum to BCD	INH	19	—	2	—	—	—	—	Δ	Δ	Δ	Δ
DEC (opr)	Decrement Memory Byte	M – 1 ⇒ M	EXT IND,X IND,Y	7A 6A 18 6A	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	—
DECA	Decrement Accumulator A	A – 1 ⇒ A	A INH	4A	—	2	—	—	—	—	Δ	Δ	Δ	—
DECB	Decrement Accumulator B	B – 1 ⇒ B	B INH	5A	—	2	—	—	—	—	Δ	Δ	Δ	—
DES	Decrement Stack Pointer	SP – 1 ⇒ SP	INH	34	—	3	—	—	—	—	—	—	—	—
DEX	Decrement Index Register X	IX – 1 ⇒ IX	INH	09	—	3	—	—	—	—	—	Δ	—	—
DEY	Decrement Index Register Y	IY – 1 ⇒ IY	INH	18 09	—	4	—	—	—	—	—	Δ	—	—
EORA (opr)	Exclusive OR A with Memory	A ⊕ M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	88 98 B8 A8 18 A8	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
EORB (opr)	Exclusive OR B with Memory	B ⊕ M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C8 D8 F8 E8 18 E8	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
FDIV	Fractional Divide 16 by 16	D / IX ⇒ IX; r ⇒ D	INH	03	—	41	—	—	—	—	—	Δ	Δ	Δ
IDIV	Integer Divide 16 by 16	D / IX ⇒ IX; r ⇒ D	INH	02	—	41	—	—	—	—	—	Δ	0	Δ
INC (opr)	Increment Memory Byte	M + 1 ⇒ M	EXT IND,X IND,Y	7C 6C 18 6C	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	—
INCA	Increment Accumulator A	A + 1 ⇒ A	A INH	4C	—	2	—	—	—	—	Δ	Δ	Δ	—
INCB	Increment Accumulator B	B + 1 ⇒ B	B INH	5C	—	2	—	—	—	—	Δ	Δ	Δ	—
INS	Increment Stack Pointer	SP + 1 ⇒ SP	INH	31	—	3	—	—	—	—	—	—	—	—

Table 4-2 provides a list of the interrupts with a vector location in memory for each, as well as the actual condition code and control bits that mask each interrupt. Figure 4-3 shows the interrupt stacking order.

Table 4-2. Interrupt and Reset Vector Assignments

Vector Address	Interrupt Source	CCR Mask	Local Mask
$FFC0, $FFC1 ↓ $FFD4, $FFD5	Reserved	—	—
$FFD6, $FFD7	SCI serial system: • SCI transmit complete • SCI transmit data register empty • SCI idle line detect • SCI receiver overrun • SCI receive data register full	I bit	TCIE TIE ILIE RIE RIE
$FFD8, $FFD9	SPI serial transfer complete	I bit	SPIE
$FFDA, $FFDB	Pulse accumulator input edge	I bit	PAII
$FFDC, $FFDD	Pulse accumulator overflow	I bit	PAOVI
$FFDE, $FFDF	Timer overflow	I bit	TOI
$FFE0, $FFE1	Timer input capture 4/output compare 5	I bit	I4/O5I
$FFE2, $FFE3	Timer output compare 4	I bit	OC4I
$FFE4, $FFE5	Timer output compare 3	I bit	OC3I
$FFE6, $FFE7	Timer output compare 2	I bit	OC2I
$FFE8, $FFE9	Timer output compare 1	I bit	OC1I
$FFEA, $FFEB	Timer input capture 3	I bit	IC3I
$FFEC, $FFED	Timer input capture 2	I bit	IC2I
$FFEE, $FFEF	Timer input capture 1	I bit	IC1I
$FFF0, $FFF1	Real time interrupt	I bit	RTII
$FFF2, $FFF3	$\overline{\text{IRQ}}$ (external pin)	I bit	None
$FFF4, $FFF5	$\overline{\text{XIRQ}}$ pin (pseudo non-maskable)	X bit	None
$FFF6, $FFF7	Software interrupt	None	None
$FFF8, $FFF9	Illegal opcode trap	None	None
$FFFA, $FFFB	COP failure (reset)	None	NOCOP
$FFFC, $FFFD	Clock monitor fail (reset)	None	CME
$FFFE, $FFFF	$\overline{\text{RESET}}$	None	None

PORTA can be read any time. Inputs return the pin level, whereas outputs return the pin driver input level. If written, PORTA stores the data in an internal latch. It drives the pins only if they are configured as outputs. Writes to PORTA do not change the pin state when the pins are configured for timer output compares.

Out of reset, port A bits 7 and 3–0 are general high-impedance inputs, while bits 6–4 are outputs, driving low. On bidirectional lines PA7 and PA3, the timer forces the I/O state to be an output if the associated output compare is enabled. In this case, the data direction bits DDRA7 and DDRA3 in PACTL will not be changed or have any effect on those bits. When the output compare functions associated with these pins are disabled, the DDR bits in PACTL govern the I/O state.

5.3 Port B

Port B is an 8-bit, general-purpose I/O port with a data register (PORTB) and a data direction register (DDRB).

- In the single-chip mode, port B pins are general-purpose I/O pins (PB7–PB0).
- In the expanded-multiplexed mode, all of the port B pins act as the high-order address bits (A15–A8) of the address bus.

5.3.1 Port B Data Register

Address: $0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Reset:	0	0	0	0	0	0	0	0
Alt. Func.:	A15	A14	A13	A12	A11	A10	A9	A8

Figure 5-2. Port B Data Register (PORTB)

PORTB can be read at any time. Inputs return the sensed levels at the pin, while outputs return the input level of the port B pin drivers. If PORTB is written, the data is stored in an internal latch and can be driven only if port B is configured for general-purpose outputs in single-chip or bootstrap mode.

Port B pins are general--purpose inputs out of reset in single-chip and bootstrap modes. These pins are outputs (the high-order address bits) out of reset in expanded multiplexed and test modes.

5.3.2 Port B Data Direction Register

Address: $0006

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
Reset:	0	0	0	0	0	0	0	0

Figure 5-3. Data Direction Register for Port B (DDRB)

DDB7–DDB0 — Data Direction Bits for Port B

1 = Corresponding port B pin configured as output
0 = Corresponding port B pin configured for input only

SCP1 and SCP0 — SCI Baud Rate Prescaler Select Bits

These two bits select a prescale factor for the SCI baud rate generator that determines the highest possible baud rate.

Table 6-1. Baud Rate Prescale Selects

SCP1 and SCP0	Divide Internal Clock By	Crystal Frequency in MHz			
		4.0 MHz (Baud)	8.0 MHz (Baud)	10.0 MHz (Baud)	12.0 MHz (Baud)
0 0	1	62.50 K	125.0 K	156.25 K	187.5 K
0 1	3	20.83 K	41.67 K	52.08 K	62.5 K
1 0	4	15.625 K	31.25 K	38.4 K	46.88 K
1 1	13	4800	9600	12.02 K	14.42 K

SCR2–SCR0 — SCI Baud Rate Select Bits

These three bits select receiver and transmitter bit rate based on output from baud rate prescaler stage.

Table 6-2. Baud Rate Selects

SCR2–SCR0	Divide Prescaler By	Highest Baud Rate (Prescaler Output from Table 6-1)		
		4800	9600	38.4 K
0 0 0	1	4800	9600	38.4 K
0 0 1	2	2400	4800	19.2 K
0 1 0	4	1200	2400	9600
0 1 1	8	600	1200	4800
1 0 0	16	300	600	2400
1 0 1	32	150	300	1200
1 1 0	64	—	150	600
1 1 1	128	—	—	300

The prescale bits, SCP1 and SCP0, determine the highest baud rate and the SCR2–SCR0 bits select an additional binary submultiple (÷1, ÷2, ÷4, through ÷128) of this highest baud rate. The result of these two dividers in series is the 16 X receiver baud rate clock. The SCR2–SCR0 bits are not affected by reset and can be changed at any time, although they should not be changed when any SCI transfer is in progress.

Figure 6-8 illustrates the SCI baud rate timing chain. The prescale select bits determine the highest baud rate. The rate select bits determine additional divide by two stages to arrive at the receiver timing (RT) clock rate. The baud rate clock is the result of dividing the RT clock by 16.

A write collision error occurs if the SPDR is written while a transfer is in progress. Because the SPDR is not double buffered in the transmit direction, writes to SPDR cause data to be written directly into the SPI shift register. Because this write corrupts any transfer in progress, a write collision error is generated. The transfer continues undisturbed, and the write data that caused the error is not written to the shifter.

A write collision is normally a slave error because a slave has no control over when a master initiates a transfer. A master knows when a transfer is in progress, so there is no reason for a master to generate a write-collision error, although the SPI logic can detect write collisions in both master and slave devices.

The SPI configuration determines the characteristics of a transfer in progress. For a master, a transfer begins when data is written to SPDR and ends when SPIF is set. For a slave with CPHA equal to zero, a transfer starts when $\overline{SS}$ goes low and ends when $\overline{SS}$ returns high. In this case, SPIF is set at the middle of the eighth SCK cycle when data is transferred from the shifter to the parallel data register, but the transfer is still in progress until $\overline{SS}$ goes high. For a slave with CPHA equal to one, transfer begins when the SCK line goes to its active level, which is the edge at the beginning of the first SCK cycle. The transfer ends in a slave in which CPHA equals one when SPIF is set. For a slave, after a byte transfer, SCK must be in inactive state for at least 2 E-clock cycles before the next byte transfer begins.

7.7 SPI Registers

The three SPI registers, SPCR, SPSR, and SPDR, provide control, status, and data storage functions. This sub-section provides a description of how these registers are organized.

7.7.1 SPI Control Register

Address: $0028

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
Reset:	0	0	0	0	0	1	U	U

U = Unaffected

Figure 7-3. SPI Control Register (SPCR)

SPIE — Serial Peripheral Interrupt Enable Bit

0 = SPI interrupt disabled
1 = SPI interrupt enabled

SPE — Serial Peripheral System Enable Bit

0 = SPI off
1 = SPI on

DWOM — Port D Wired-OR Mode Bit

DWOM affects all six port D pins.

0 = Normal CMOS outputs
1 = Open-drain outputs

MSTR — Master Mode Select Bit

0 = Slave mode
1 = Master mode

Table 8-1. Timer Summary

Control Bits	XTAL Frequencies			
	4.0 MHz	**8.0 MHz**	**12.0 MHz**	**Other Rates**
	1.0 MHz	**2.0 MHz**	**3.0 MHz**	**(E)**
	1000 ns	**500 ns**	**333 ns**	**(1/E)**
PR1 and PR0	**Main Timer Count Rates**			
0 0 1 count — overflow —	1.0 µs 65.536 ms	500 ns 32.768 ms	333 ns 21.845 ms	(E/1) ($E/2^{16}$)
0 1 1 count — overflow —	4.0 µs 262.14 ms	2.0 µs 131.07 ms	1.333 µs 87.381 ms	(E/4) ($E/2^{18}$)
1 0 1 count — overflow —	8.0 µs 524.29 ms	4.0 µs 262.14 ms	2.667 µs 174.76 ms	(E/8) ($E/2^{19}$)
1 1 1 count — overflow —	16.0 µs 1.049 s	8.0 µs 524.29 ms	5.333 µs 349.52 ms	(E/16) ($E/2^{20}$)

8.2 Timer Structure

Figure 8-2 shows the capture/compare system block diagram. The port A pin control block includes logic for timer functions and for general-purpose input/output (I/O). For pins PA2, PA1, and PA0, this block contains both the edge-detection logic and the control logic that enables the selection of which edge triggers an input capture. The digital level on PA2–PA0 can be read at any time (read PORTA register), even if the pin is being used for the input capture function. Pins PA6–PA4 are used for either general-purpose output or as output compare pins. Pin PA3 can be used for general-purpose I/O, input capture 4, output compare 5, or output compare 1. When one of these pins is being used for an output compare function, it cannot be written directly as if it were a general-purpose output. Each of the output compare functions (OC5–OC2) is related to one of the port A output pins. Output compare 1 (OC1) has extra control logic, allowing it optional control of any combination of the PA7–PA3 pins. The PA7 pin can be used as a general-purpose I/O pin, as an input to the pulse accumulator, or as an OC1 output pin.

8.3 Input Capture

The input capture function records the time an external event occurs by latching the value of the free-running counter when a selected edge is detected at the associated timer input pin. Software can store latched values and use them to compute the periodicity and duration of events. For example, by storing the times of successive edges of an incoming signal, software can determine the period and pulse width of a signal. To measure period, two successive edges of the same polarity are captured. To measure pulse width, two alternate polarity edges are captured.

In most cases, input capture edges are asynchronous to the internal timer counter, which is clocked relative to the PH2 clock. These asynchronous capture requests are synchronized to PH2 so that the latching occurs on the opposite half cycle of PH2 from when the timer counter is being incremented. This synchronization process introduces a delay from when the edge occurs to when the counter value is detected. Because these delays offset each other when the time between two edges is being measured, the delay can be ignored. When an input capture is being used with an output compare, there is a similar delay between the actual compare point and when the output pin changes state.

8.5 Real-Time Interrupt

The real-time interrupt feature, used to generate hardware interrupts at a fixed periodic rate, is controlled and configured by two bits (RTR1 and RTR0) in the pulse accumulator control (PACTL) register. The RTII bit in the TMSK2 register enables the interrupt capability. The four different rates available are a product of the MCU oscillator frequency and the value of bits RTR1 and RTR0. Refer to Table 8-5 for the periodic real-time interrupt rates.

Table 8-5. Periodic Real-Time Interrupt Rates

RTR1 and RTR0	E = 1 MHz	E = 2 MHz	E = 3 MHz	E = X MHz
0 0	2.731 ms	4.096 ms	8.192 ms	$(E/2^{13})$
0 1	5.461 ms	8.192 ms	16.384 ms	$(E/2^{14})$
1 0	10.923 ms	16.384 ms	32.768 ms	$(E/2^{15})$
1 1	21.845 ms	32.768 ms	65.536 ms	$(E/2^{16})$

The clock source for the RTI function is a free-running clock that cannot be stopped or interrupted except by reset. This clock causes the time between successive RTI timeouts to be a constant that is independent of the software latencies associated with flag clearing and service. For this reason, an RTI period starts from the previous timeout, not from when RTIF is cleared.

Every timeout causes the RTIF bit in TFLG2 to be set, and if RTII is set, an interrupt request is generated. After reset, one entire real-time interrupt period elapses before the RTIF flag is set for the first time. Refer to the TMSK2, TFLG2, and PACTL registers.

8.5.1 Timer Interrupt Mask 2 Register

The timer interrupt mask 2 register (TMSK2) contains the real-time interrupt enable bits.

Address: $0024

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
Reset:	0	0	0	0	0	0	0	0

Figure 8-16. Timer Interrupt Mask 2 Register (TMSK2)

TOI — Timer Overflow Interrupt Enable Bit
Refer to 8.4 Output Compare (OC).

RTII — Real-Time Interrupt Enable Bit
0 = RTIF interrupts disabled
1 = Interrupt requested

PAOVI — Pulse Accumulator Overflow Interrupt Enable Bit
Refer to 8.7 Pulse Accumulator.

PAII — Pulse Accumulator Input Edge Bit
Refer to 8.7 Pulse Accumulator.

Bits 3–2 — Unimplemented
Always read 0.

DDRA7 — Data Direction Control for Port A Bit 7
Refer to 8.7 Pulse Accumulator.

PAEN — Pulse Accumulator System Enable Bit
Refer to 8.7 Pulse Accumulator.

PAMOD — Pulse Accumulator Mode Bit
Refer to 8.7 Pulse Accumulator.

PEDGE — Pulse Accumulator Edge Control Bit
Refer to 8.7 Pulse Accumulator.

DDRA3 — Data Direction Register for Port A Bit 3
Refer to Chapter 5 Input/Output (I/O) Ports.

I4/O5 — Input Capture 4/Output Compare 5 Bit
Refer to 8.3 Input Capture.

RTR1 and RTR0 — RTI Interrupt Rate Select Bits
These two bits determine the rate at which the RTI system requests interrupts. The RTI system is driven by an E divided by 2^{13} rate clock that is compensated so it is independent of the timer prescaler. These two control bits select an additional division factor. See Table 8-6.

Table 8-6. Real-Time Interrupt Rates

RTR1 and RTR0	E = 1 MHz	E = 2 MHz	E = 3 MHz	E = X MHz
0 0	2.731 ms	4.096 ms	8.192 ms	$(E/2^{13})$
0 1	5.461 ms	8.192 ms	16.384 ms	$(E/2^{14})$
1 0	10.923 ms	16.384 ms	32.768 ms	$(E/2^{15})$
1 1	21.845 ms	32.768 ms	65.536 ms	$(E/2^{16})$

8.6 Computer Operating Properly Watchdog Function

The clocking chain for the COP function, tapped off of the main timer divider chain, is only superficially related to the main timer system. The CR1 and CR0 bits in the OPTION register and the NOCOP bit in the CONFIG register determine the status of the COP function. Refer to Chapter 4 Resets, Interrupts, and Low-Power Modes for a more detailed discussion of the COP function.

8.7 Pulse Accumulator

The MC68HC711D3 has an 8-bit counter that can be configured to operate either as a simple event counter or for gated time accumulation, depending on the state of the PAMOD bit in the PACTL register. Refer to the pulse accumulator block diagram, Figure 8-19.

In the event counting mode, the 8-bit counter is clocked to increasing values by an external pin. The maximum clocking rate for the external event counting mode is the E clock divided by two. In gated time accumulation mode, a free-running E-clock ÷ 64 signal drives the 8-bit counter, but only while the external PAI pin is activated. Refer to Table 8-7. The pulse accumulator counter can be read or written at any time.

Pulse accumulator control bits are also located within two timer registers, TMSK2 and TFLG2, as described here.

Chapter 9
Electrical Characteristics

9.1 Introduction

This section contains electrical specifications.

9.2 Maximum Ratings

Maximum ratings are the extreme limits to which the microcontroller unit (MCU) can be exposed without permanently damaging it.

NOTE

This device is not guaranteed to operate properly at the maximum ratings. Refer to 9.5 DC Electrical Characteristics for guaranteed operating conditions.

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Input voltage	V_{In}	–0.3 to +7.0	V
Current drain per pin(1) Excluding V_{DD}, V_{SS}, $V_{RH, and}$ V_{RL}	I_D	25	mA
Storage temperature	T_{STG}	–55 to +150	°C

1. One pin at a time, observing maximum power dissipation limits

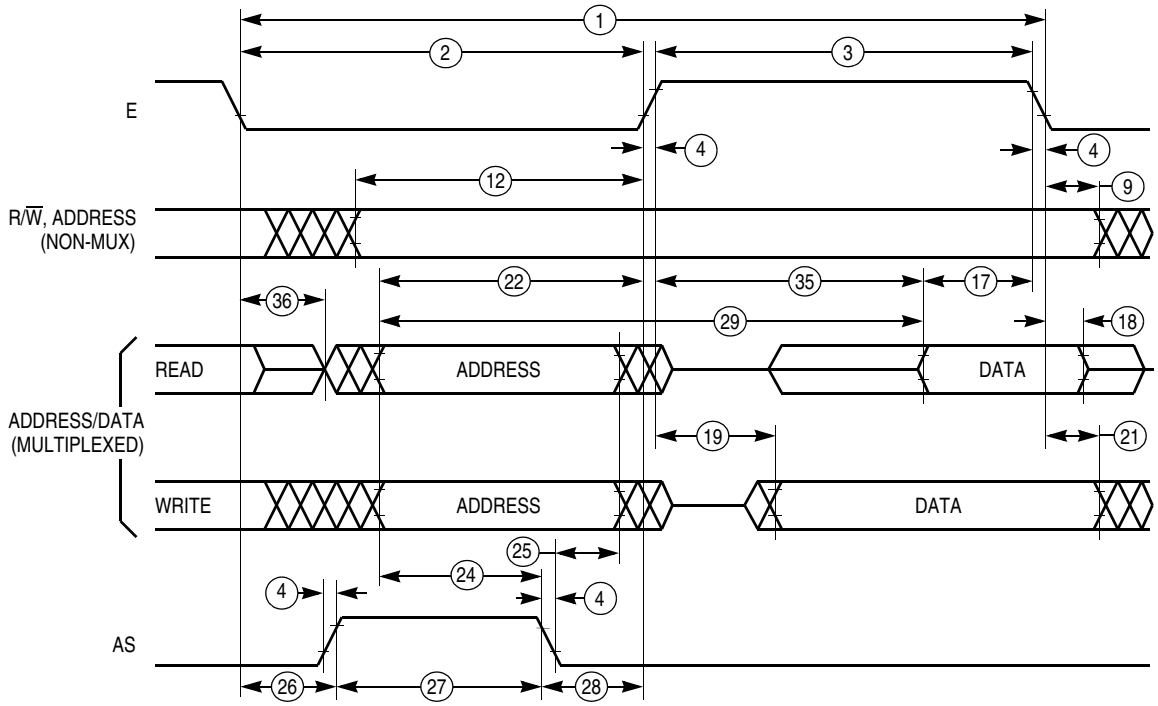
NOTE

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{In} and V_{Out} be constrained to the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}).

9.8 Expansion Bus Timing

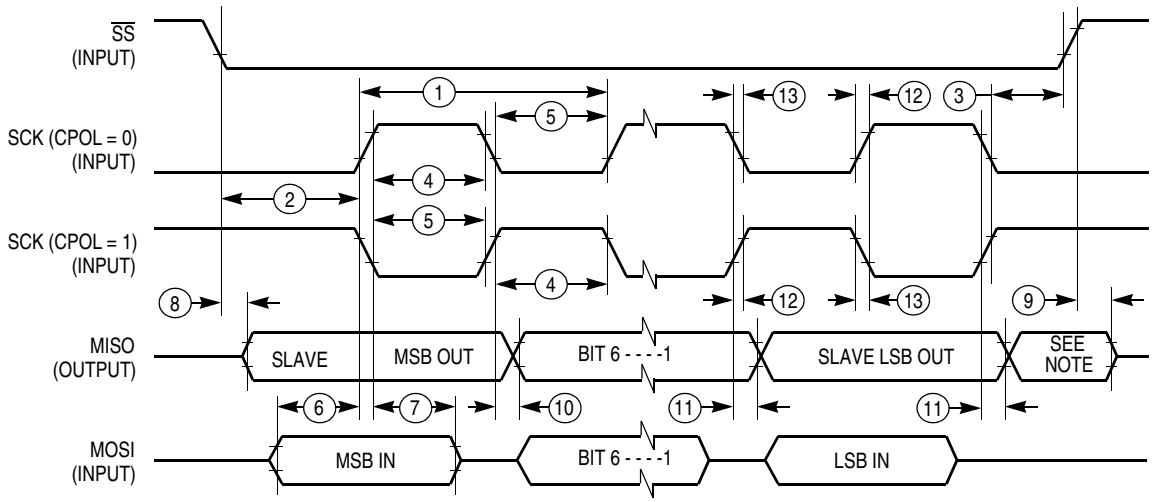
Num	Characteristic[1]	Symbol	1.0 MHz		2.0 MHz		3.0 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Frequency of operation (E-clock frequency)	f_O	dc	1.0	dc	2.0	dc	3.0	MHz
1	Cycle time	t_{cyc}	1000	—	500	—	333	—	ns
2	Pulse width, E low, PW_{EL} = 1/2 t_{cyc} — 23 ns	PW_{EL}	477	—	227	—	146	—	ns
3	Pulse width, E high, PW_{EH} = 1/2 t_{cyc} – 28 ns	PW_{EH}	472	—	222	—	141	—	ns
4A	E and AS rise time	t_r	—	20	—	20	—	20	ns
4B	E and AS fall time	t_f	—	20	—	20	—	15	ns
9	Address hold time[2]a, t_{AH} = 1/8 t_{cyc} – 29.5 ns	t_{AH}	95.5	—	33	—	26	—	ns
12	Non-muxed address valid time to E rise $t_{AV} = PW_{EL} – (t_{ASD} + 80\ ns)$[2]a	t_{AV}	281.5	—	94	—	54	—	ns
17	Read data setup time	t_{DSR}	30	—	30	—	30	—	ns
18	Read data hold time (max = t_{MAD})	t_{DHR}	0	145.5	0	83	0	51	ns
19	Write data delay time, t_{DDW} = 1/8 t_{cyc} + 65.5 ns[2]a	t_{DDW}	—	190.5	—	128	—	71	ns
21	Write data hold time, t_{DHW} = 1/8 t_{cyc} – 29.5 ns[2]a	t_{DHW}	95.5	—	33	—	26	—	ns
22	Muxed address valid time to E rise $t_{AVM} = PW_{EL} – (t_{ASD} + 90\ ns)$[2]a	t_{AVM}	271.5	—	84	—	54	—	ns
24	Muxed address valid time to AS fall $t_{ASL} = PW_{ASH} – 70$ ns	t_{ASL}	151	—	26	—	13	—	ns
25	Muxed address hold time, t_{AHL} = 1/8 t_{cyc} – 29.5 ns[2]b	t_{AHL}	95.5	—	33	—	31	—	ns
26	Delay time, E to AS rise, t_{ASD} = 1/8 t_{cyc} – 9.5 ns[2]a	t_{ASD}	115.5	—	53	—	31	—	ns
27	Pulse width, AS high, PW_{ASH} = 1/4 t_{cyc} – 29 ns	PW_{ASH}	221	—	96	—	63	—	ns
28	Delay time, AS to E rise, t_{ASED} = 1/8 t_{cyc} – 9.5 ns[2]b	t_{ASED}	115.5	—	53	—	31	—	ns
29	MPU address access time[2]a $t_{ACCA} = t_{cyc} – (PW_{EL} – t_{AVM}) – t_{DSR} – t_f$	t_{ACCA}	744.5	—	307	—	196	—	ns
35	MPU access time , $t_{ACCE} = PW_{EH} – t_{DSR}$	t_{ACCE}	—	442	—	192	—	111	ns
36	Muxed address delay (previous cycle MPU read) $t_{MAD} = t_{ASD} + 30\ ns$[2]a[3]	t_{MAD}	145.5	—	83	—	51	—	ns

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Input clocks with duty cycles other than 50% affect bus performance. Timing parameters affected by input clock duty cycle are identified by (a) and (b). To recalculate the approximate bus timing values, substitute the following expressions in place of 1/8 t_{CYC} in the above formulas, where applicable:
   (a) (1-dc) × 1/4 t_{CYC}
   (b) dc × 1/4 t_{CYC}
   Where:
   DC is the decimal value of duty cycle percentage (high time).
3. Formula only for dc to 2 MHz.



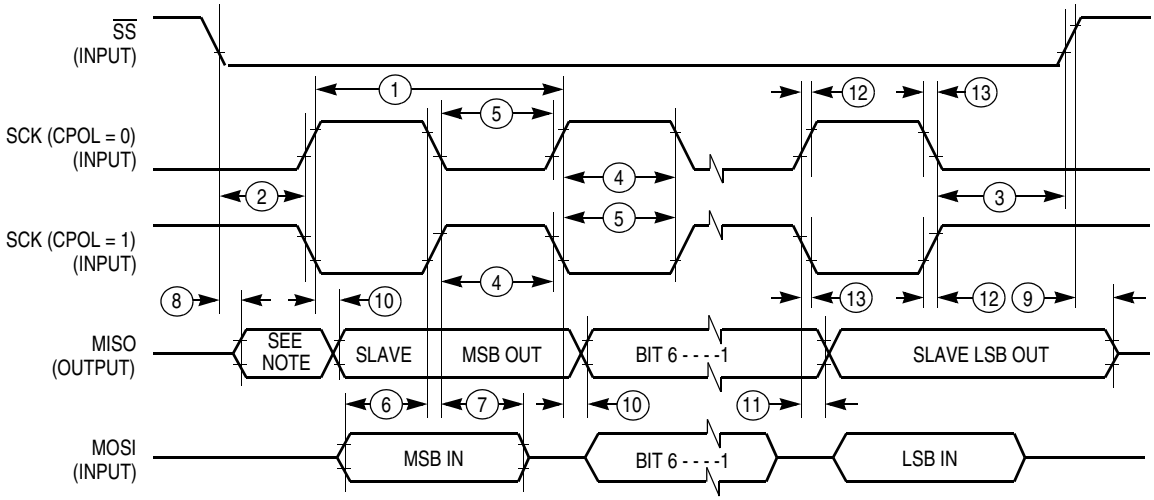
Note: Measurement points shown are 20% and 70% of V_{DD}.

Figure 9-10. Multiplexed Expansion Bus Timing Diagram



Note: Not defined but normally MSB of character just received

Figure 9-13. SPI Slave Timing (CPHA = 0)



Note: Not defined but normally LSB of character previously transmitted

Figure 9-14. SPI Slave Timing (CPHA = 1)