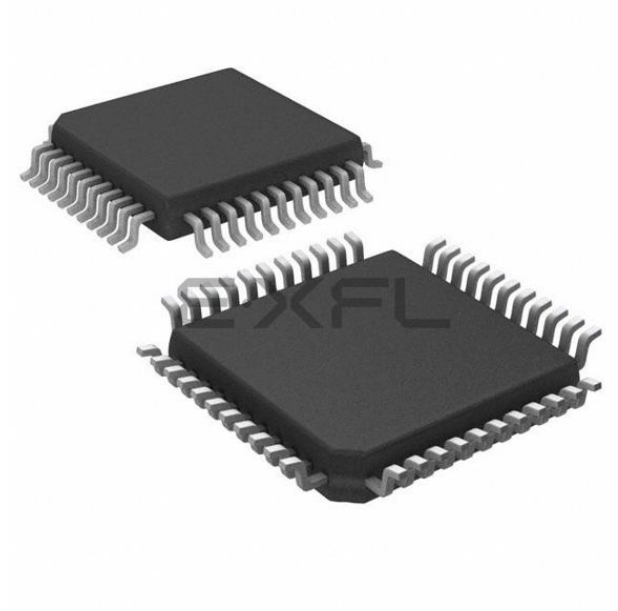

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	3MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	26
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-QFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc11d0cfbe3r

List of Chapters

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General Description

Chapter 2
Operating Modes and Memory

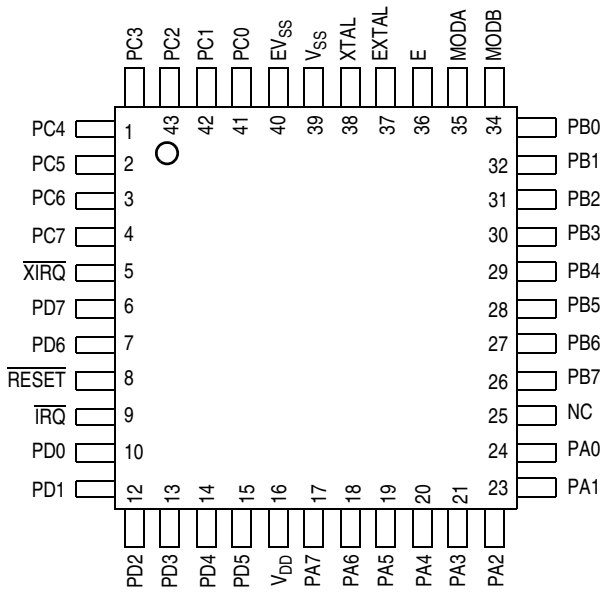


Figure 1-4. Pin Assignments for 44-Pin QFP

1.5 Power Supply (V_{DD}, V_{SS}, and EV_{SS})

Power is supplied to the MCU through V_{DD} and V_{SS}. V_{DD} is the power supply (+5 V ±10%) and V_{SS} is ground (0 V). EV_{SS}, available on the 44-pin PLCC and QFP, is an additional ground pin.

1.6 Reset ($\overline{\text{RESET}}$)

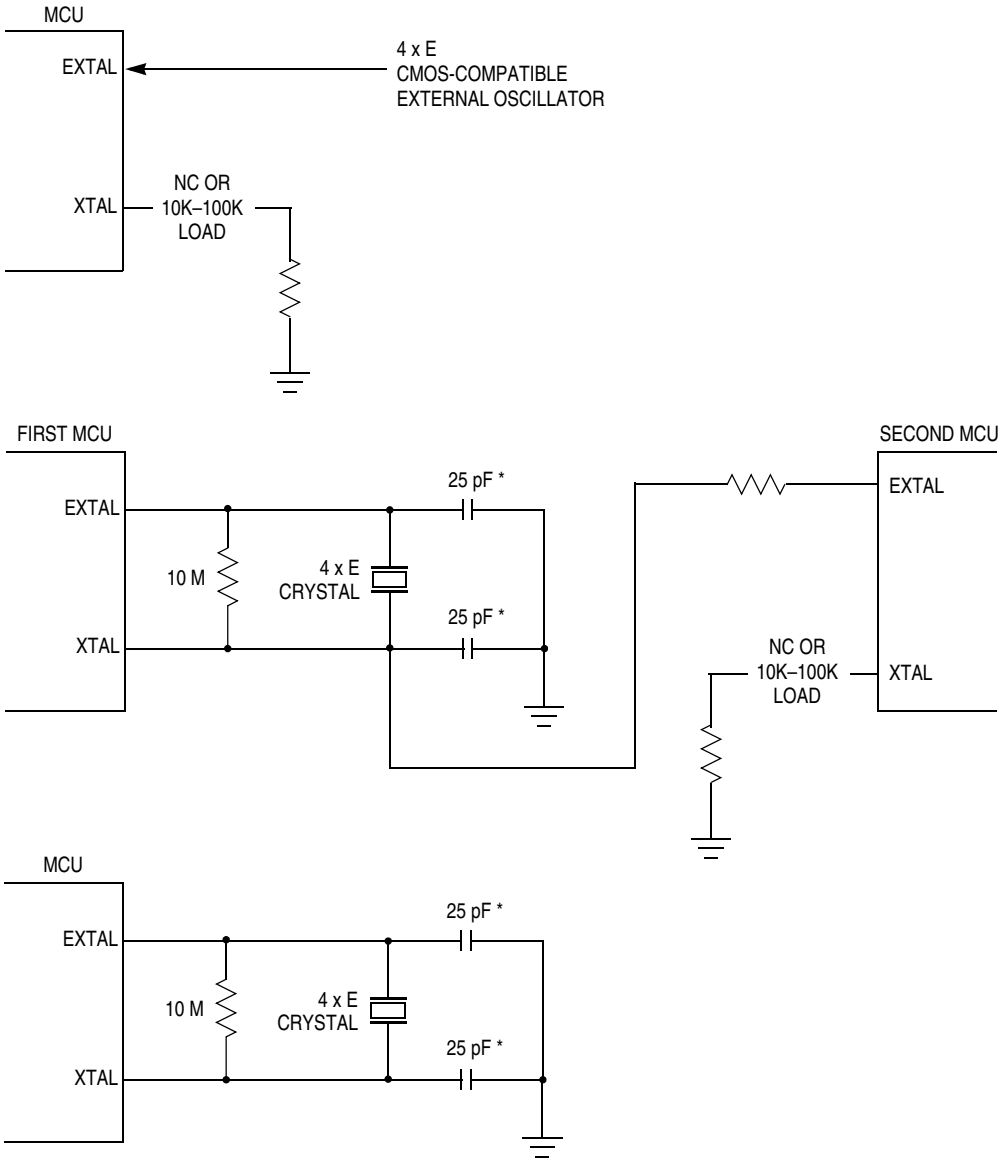
An active low bidirectional control signal, $\overline{\text{RESET}}$, acts as an input to initialize the MCU to a known startup state. It also acts as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or computer operating properly (COP) watchdog circuit. In addition, the state of this pin is one of the factors governing the selection of BOOT mode.

1.7 Crystal Driver and External Clock Input (XTAL and EXTAL)

These two pins provide the interface for either a crystal or a CMOS compatible clock to control the internal clock generator circuitry. The frequency applied to these pins is four times higher than the desired E-clock rate. Refer to Figure 1-5 for crystal and clock connections.

1.8 E-Clock Output (E)

E is the output connection for the internally generated E clock. The signal from E is used as a timing reference. The frequency of the E-clock output is one fourth that of the input frequency at the XTAL and EXTAL pins. The E clock can be turned off in single-chip mode for greater noise immunity if desired. See 4.3.6 Highest Priority I Interrupt and Miscellaneous Register (HPRIO) for details.



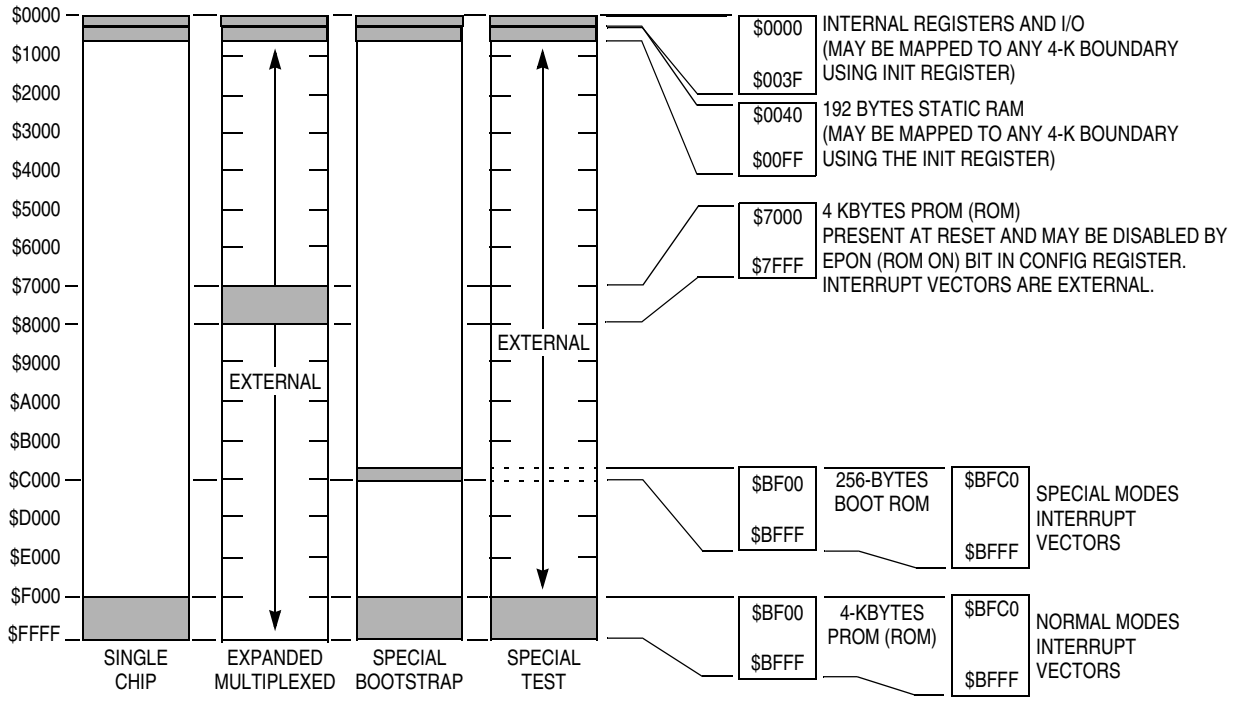
* Values includes all stray capacitances.

Figure 1-5. Oscillator Connections

1.9 Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ input provides a means of applying asynchronous interrupt requests to the microcontroller unit (MCU). Either negative edge-sensitive triggering or level-sensitive triggering is program selectable by using the IRQE bit of the OPTION register. $\overline{IRQ}$ is always configured to level-sensitive triggering at reset.

While the programmable read-only memory (PROM) is being programmed, this pin provides the chip enable ($\overline{CE}$) signal. To prevent accidental programming of the PROM during reset, an external resistor is required on $\overline{IRQ}$ to pull the pin to V_{DD}.



MODB	MODA	Mode Selected
1	0	Single-chip (mode 0)
1	1	Expanded multiplexed (mode 1)
0	0	Special bootstrap
0	1	Special test

Figure 2-1. MC68HC711D3 Memory Map

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0026	Pulse Accumulator Control Register (PACTL) See pages 99 and 102.	Read: Write:	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
		Reset:	0	0	0	0	0	0	0	0
$0027	Pulse Accumulator Count Register (PACNT) See page 103.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Unaffected by reset							
$0028	SPI Control Register (SPCR) See page 81.	Read: Write:	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
		Reset:	0	0	0	0	0	1	U	U
$0029	SPI Status Register (SPSR) See page 82.	Read: Write:	SPIF	WCOL	0	MODF	0	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$002A	SPI Data I/O Register (SPDR) See page 83.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Unaffected by reset							
$002B	Baud Rate Register (BAUD) See page 72.	Read: Write:	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
		Reset:	0	0	0	0	0	U	U	U
$002C	SCI Control Register 1 (SCCR1) See page 70.	Read: Write:	R8	T8	0	M	WAKE	0	0	0
		Reset:	U	U	0	0	0	0	0	0
$002D	SCI Control Register 2 (SCCR2) See page 70.	Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Reset:	0	0	0	0	0	0	0	0
$002E	SCI Status Register (SCSR) See page 71.	Read: Write:	TDRE	TC	RDRF	IDLE	OR	NF	FE	0
		Reset:	1	1	0	0	0	0	0	0
$002F	SCI Data Register (SCDR) See page 69.	Read: Write:	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
		Reset:	Unaffected by reset							
$0030 ↓ $0038	Reserved		R	R	R	R	R	R	R	R
$0039	System Configuration Options Register (OPTION) See page 49.	Read: Write:	0	0	IRQE	DLY	CME	0	CR1	CR0
		Reset:	0	0	0	1	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Register and Control Bit Assignments (Sheet 4 of 5)

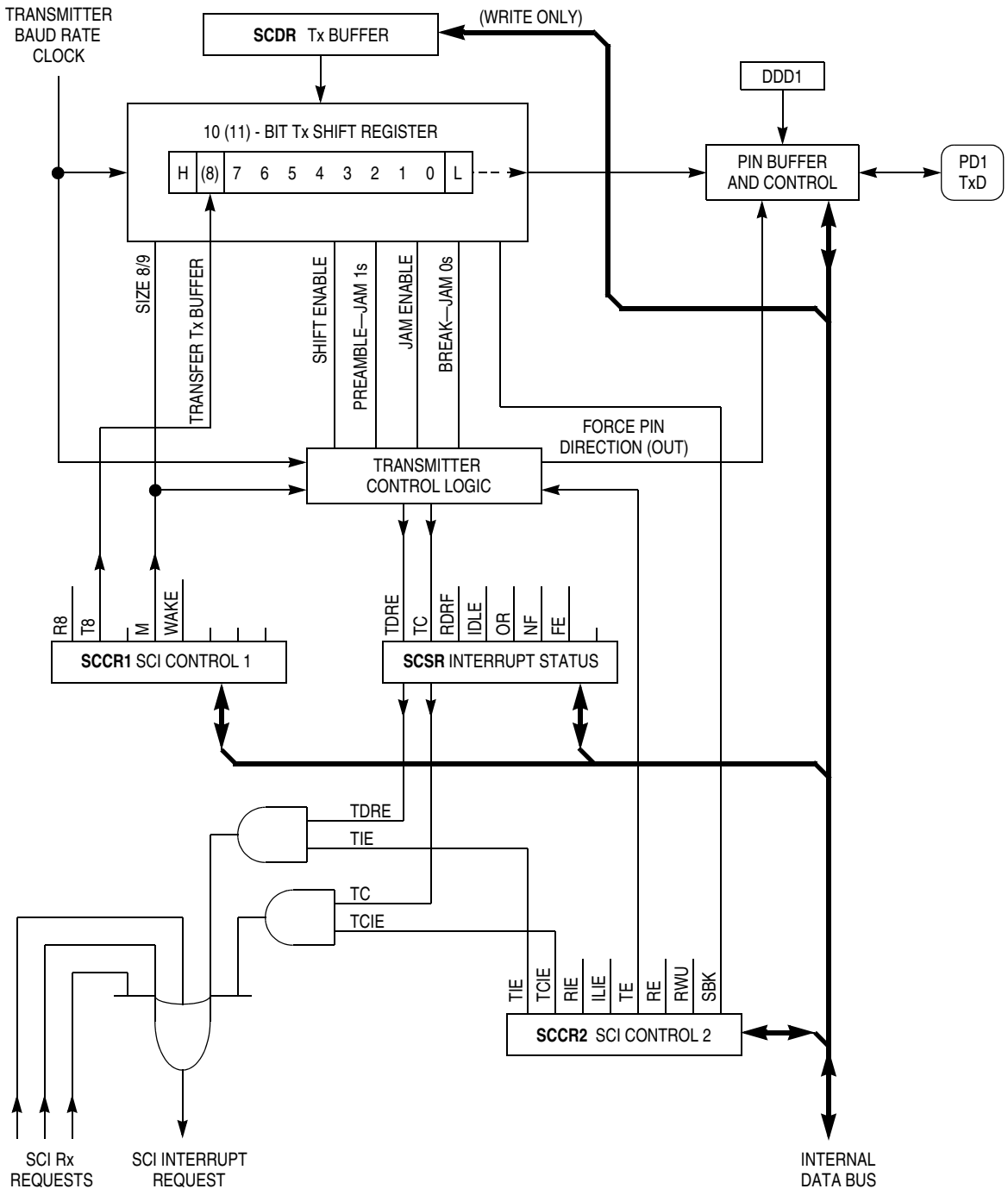


Figure 6-1. SCI Transmitter Block Diagram

IDLE — Idle Line Detected Flag

This flag is set if the RxD line is idle. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again. The IDLE flag is inhibited when RWU = 1. Clear IDLE by reading SCSR with IDLE set and then reading SCDR.

0 = RxD line active
1 = RxD line idle

OR — Overrun Error Flag

OR is set if a new character is received before a previously received character is read from SCDR. Clear the OR flag by reading SCSR with OR set and then reading SCDR.

0 = No overrun
1 = Overrun detected

NF — Noise Error Flag

NF is set if majority sample logic detects anything other than a unanimous decision. Clear NF by reading SCSR with NF set and then reading SCDR.

0 = Unanimous decision
1 = Noise detected

FE — Framing Error Bit

FE is set when a 0 is detected where a stop bit was expected. Clear the FE flag by reading SCSR with FE set and then reading SCDR.

0 = Stop bit detected
1 = Zero detected

6.7.5 Baud Rate Register

The baud rate register (BAUD) is used to select different baud rates for the SCI system. The SCP1 and SCP0 bits function as a prescaler for the SCR2–SCR0 bits. Together, these five bits provide multiple baud rate combinations for a given crystal frequency. Normally, this register is written once during initialization. The prescaler is set to its fastest rate by default out of reset and can be changed at any time. Refer to Table 6-1 and Table 6-2 for normal baud rate selections.

Address: $002B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
Reset:	0	0	0	0	0	U	U	U

U = Unaffected

Figure 6-7. Baud Rate Register (BAUD)

TCLR — Clear Baud Rate Counters (Test)

RCKB — SCI Baud Rate Clock Check (Test)

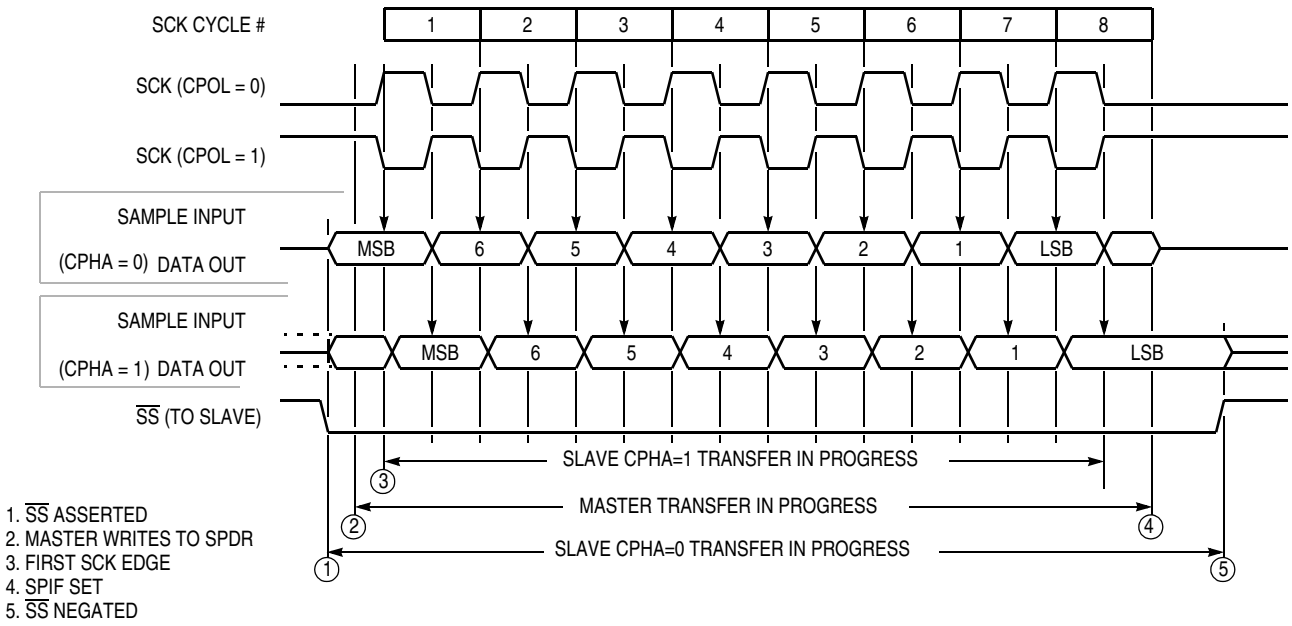


Figure 7-2. SPI Transfer Format

7.4 Clock Phase and Polarity Controls

Software can select one of four combinations of serial clock phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock, and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements.

When CPHA equals 0, the slave select ($\overline{SS}$) line must be negated and reasserted between each successive serial byte. Also, if the slave writes data to the SPI data register (SPDR) while $\overline{SS}$ is active low, a write collision error results.

When CPHA equals 1, the $\overline{SS}$ line can remain low between successive transfers.

7.5 SPI Signals

This subsection contains description of the four SPI signals:

- Master in/slave out (MISO)
- Master out/slave in (MOSI)
- Serial clock (SCK)
- Slave select ($\overline{SS}$)

7.5.1 Master In/Slave Out (MISO)

MISO is one of two unidirectional serial data signals. It is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.

8.4 Output Compare (OC)

Use the output compare (OC) function to program an action to occur at a specific time — when the 16-bit counter reaches a specified value. For each of the five output compare functions, there is a separate 16-bit compare register and a dedicated 16-bit comparator. The value in the compare register is compared to the value of the free-running counter on every bus cycle. When the compare register matches the counter value, an output compare status flag is set. The flag can be used to initiate the automatic actions for that output compare function.

To produce a pulse of a specific duration, write to the output compare register a value representing the time the leading edge of the pulse is to occur. The output compare circuit is configured to set the appropriate output either high or low, depending on the polarity of the pulse being produced. After a match occurs, the output compare register is reprogrammed to change the output pin back to its inactive level at the next match. A value representing the width of the pulse is added to the original value, and then is written to the output compare register. Because the pin state changes occur at specific values of the free-running counter, the pulse width can be controlled accurately at the resolution of the free-running counter, independent of software latencies. To generate an output signal of a specific frequency and duty cycle, repeat this pulse-generating procedure.

There are four 16-bit read/write output compare registers: TOC1, TOC2, TOC3, and TOC4, and the TI4/O5 register, which functions under software control as either IC4 or OC5. Each of the OC registers is set to $FFFF on reset. A value written to an OC register is compared to the free-running counter value during each E-clock cycle. If a match is found, the particular output compare flag is set in timer interrupt flag register 1 (TFLG1). If that particular interrupt is enabled in the timer interrupt mask register 1 (TMSK1), an interrupt is generated. In addition to an interrupt, a specified action can be initiated at one or more timer output pins. For OC5–OC2, the pin action is controlled by pairs of bits (OMx and OLx) in the TCTL1 register. The output action is taken on each successful compare, regardless of whether the OCxF flag in the TFLG1 register was previously cleared.

OC1 is different from the other output compares in that a successful OC1 compare can affect any or all five of the OC pins. The OC1 output action taken when a match is found is controlled by two 8-bit registers with three bits unimplemented: the output compare 1 mask register, OC1M, and the output compare 1 data register, OC1D. OC1M specifies which port A outputs are to be used, and OC1D specifies what data is placed on these port pins.

8.4.1 Timer Output Compare Registers

All output compare registers are 16-bit read-write. Each is initialized to $FFFF at reset. If an output compare register is not used for an output compare function, it can be used as a storage location. A write to the high-order byte of an output compare register pair inhibits the output compare function for one bus cycle. This inhibition prevents inappropriate subsequent comparisons. Coherency requires a complete 16-bit read or write. However, if coherency is not needed, byte accesses can be used.

For output compare functions, write a comparison value to output compare registers TOC1–TOC4 and TI4/O5. When TCNT value matches the comparison value, specified pin actions occur.

8.4.2 Timer Compare Force Register

The timer compare force register (CFORC) allows forced early compares. FOC1–FOC5 correspond to the five output compares. These bits are set for each output compare that is to be forced. The action taken as a result of a forced compare is the same as if there were a match between the OCx register and the free-running counter, except that the corresponding interrupt status flag bits are not set. The forced channels trigger their programmed pin actions to occur at the next timer count transition after the write to CFORC.

The CFORC bits should not be used on an output compare function that is programmed to toggle its output on a successful compare because a normal compare that occurs immediately before or after the force can result in an undesirable operation.

Address: $000B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 8-7. Timer Compare Force Register (CFORC)

FOC1–FOC5 — Write 1s to Force Compare Bits

0 = Not affected
1 = Output x action occurs

Bits 2–0 — Not implemented, always read 0.

8.4.3 Output Compare 1 Mask Register

Use OC1M with OC1 to specify the bits of port A that are affected by a successful OC1 compare. The bits of the OC1M register correspond to PA7–PA3.

Address: $000C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 8-8. Output Compare 1 Mask Register (OC1M)

OC1M7–OC1M3 — Output Compare Masks

0 = OC1 disabled
1 = OC1 enabled to control the corresponding pin of port A

Bits 2–0 — Not implemented; always read 0.

Set bit(s) to enable OC1 to control corresponding pin(s) of port A.

8.4.8 Timer Interrupt Flag 1 Register

The timer interrupt flag 1 register (TFLG1) bits indicate when timer system events have occurred. Coupled with the bits of TMSK1, the bits of TFLG1 allow the timer subsystem to operate in either a polled or interrupt driven system. Each bit of TFLG1 corresponds to a bit in TMSK1 in the same position.

Address: $0023

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
Reset:	0	0	0	0	0	0	0	0

Figure 8-13. Timer Interrupt Flag 1 Register (TFLG1)

Clear flags by writing a 1 to the corresponding bit position(s).

OC1F–OC5F — Output Compare x Flag
Set each time the counter matches output compare x value

I4/O5F — Input Capture 4/Output Compare 5 Flag
Set by IC4 or OC5, depending on the function enabled by I4/O5 bit in PACTL

IC1F–IC3F — Input Capture x Flag
Set each time a selected active edge is detected on the ICx input line

8.4.9 Timer Interrupt Mask 2 Register

The timer interrupt mask 1 register (TMSK2) is an 8-bit register used to enable or inhibit timer overflow and real-time interrupts. The timer prescaler control bits are included in this register.

Address: $0024

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
Reset:	0	0	0	0	0	0	0	0

Figure 8-14. Timer Interrupt Mask 2 Register (TMSK2)

TOI — Timer Overflow Interrupt Enable Bit
0 = TOF interrupts disabled
1 = Interrupt requested when TOF is set to 1

RTII — Real-Time Interrupt Enable Bit
Refer to 8.5 Real-Time Interrupt.

PAOVI — Pulse Accumulator Overflow Interrupt Enable Bit
Refer to 8.7 Pulse Accumulator.

PAII — Pulse Accumulator Input Edge Interrupt Enable Bit
Refer to 8.7 Pulse Accumulator.

NOTE

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

DDRA7 — Data Direction Control for Port A Bit 7
Refer to 8.7 Pulse Accumulator.

PAEN — Pulse Accumulator System Enable Bit
Refer to 8.7 Pulse Accumulator.

PAMOD — Pulse Accumulator Mode Bit
Refer to 8.7 Pulse Accumulator.

PEDGE — Pulse Accumulator Edge Control Bit
Refer to 8.7 Pulse Accumulator.

DDRA3 — Data Direction Register for Port A Bit 3
Refer to Chapter 5 Input/Output (I/O) Ports.

I4/O5 — Input Capture 4/Output Compare 5 Bit
Refer to 8.3 Input Capture.

RTR1 and RTR0 — RTI Interrupt Rate Select Bits
These two bits determine the rate at which the RTI system requests interrupts. The RTI system is driven by an E divided by 2^{13} rate clock that is compensated so it is independent of the timer prescaler. These two control bits select an additional division factor. See Table 8-6.

Table 8-6. Real-Time Interrupt Rates

RTR1 and RTR0	E = 1 MHz	E = 2 MHz	E = 3 MHz	E = X MHz
0 0	2.731 ms	4.096 ms	8.192 ms	$(E/2^{13})$
0 1	5.461 ms	8.192 ms	16.384 ms	$(E/2^{14})$
1 0	10.923 ms	16.384 ms	32.768 ms	$(E/2^{15})$
1 1	21.845 ms	32.768 ms	65.536 ms	$(E/2^{16})$

8.6 Computer Operating Properly Watchdog Function

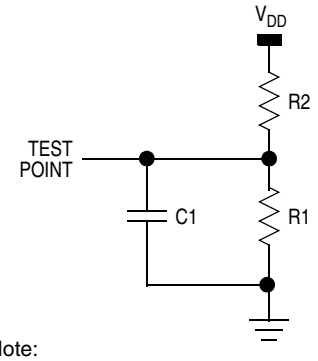
The clocking chain for the COP function, tapped off of the main timer divider chain, is only superficially related to the main timer system. The CR1 and CR0 bits in the OPTION register and the NOCOP bit in the CONFIG register determine the status of the COP function. Refer to Chapter 4 Resets, Interrupts, and Low-Power Modes for a more detailed discussion of the COP function.

8.7 Pulse Accumulator

The MC68HC711D3 has an 8-bit counter that can be configured to operate either as a simple event counter or for gated time accumulation, depending on the state of the PAMOD bit in the PACTL register. Refer to the pulse accumulator block diagram, Figure 8-19.

In the event counting mode, the 8-bit counter is clocked to increasing values by an external pin. The maximum clocking rate for the external event counting mode is the E clock divided by two. In gated time accumulation mode, a free-running E-clock ÷ 64 signal drives the 8-bit counter, but only while the external PAI pin is activated. Refer to Table 8-7. The pulse accumulator counter can be read or written at any time.

Pulse accumulator control bits are also located within two timer registers, TMSK2 and TFLG2, as described here.

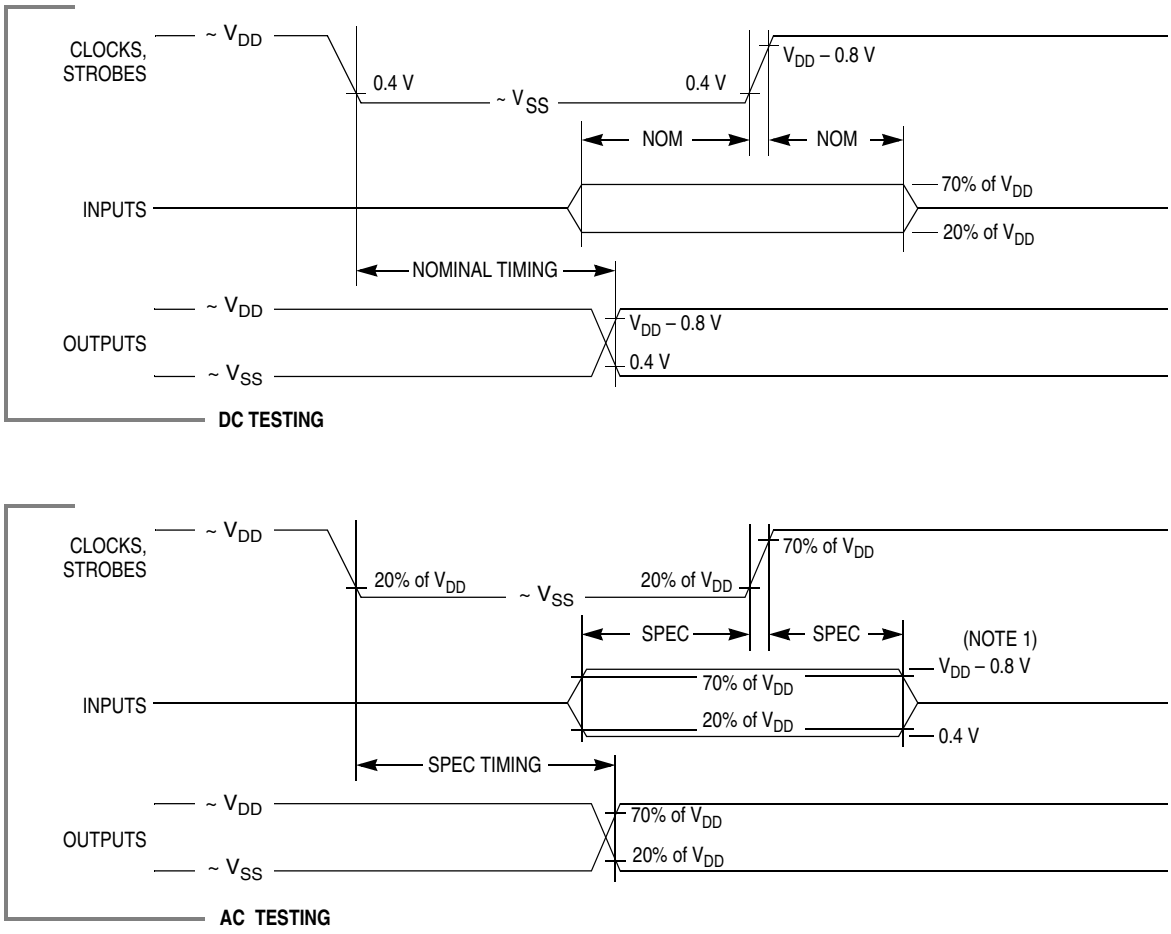


EQUIVALENT TEST LOAD(1)

Pins	R1	R2	C1
PA3–PA7 PB0–PB7 PC0–PC7 PD0, PD5–PD7 E	3.26 K	2.38 K	90 pF
PD1—PD4	3.26 K	2.38 K	200 pF

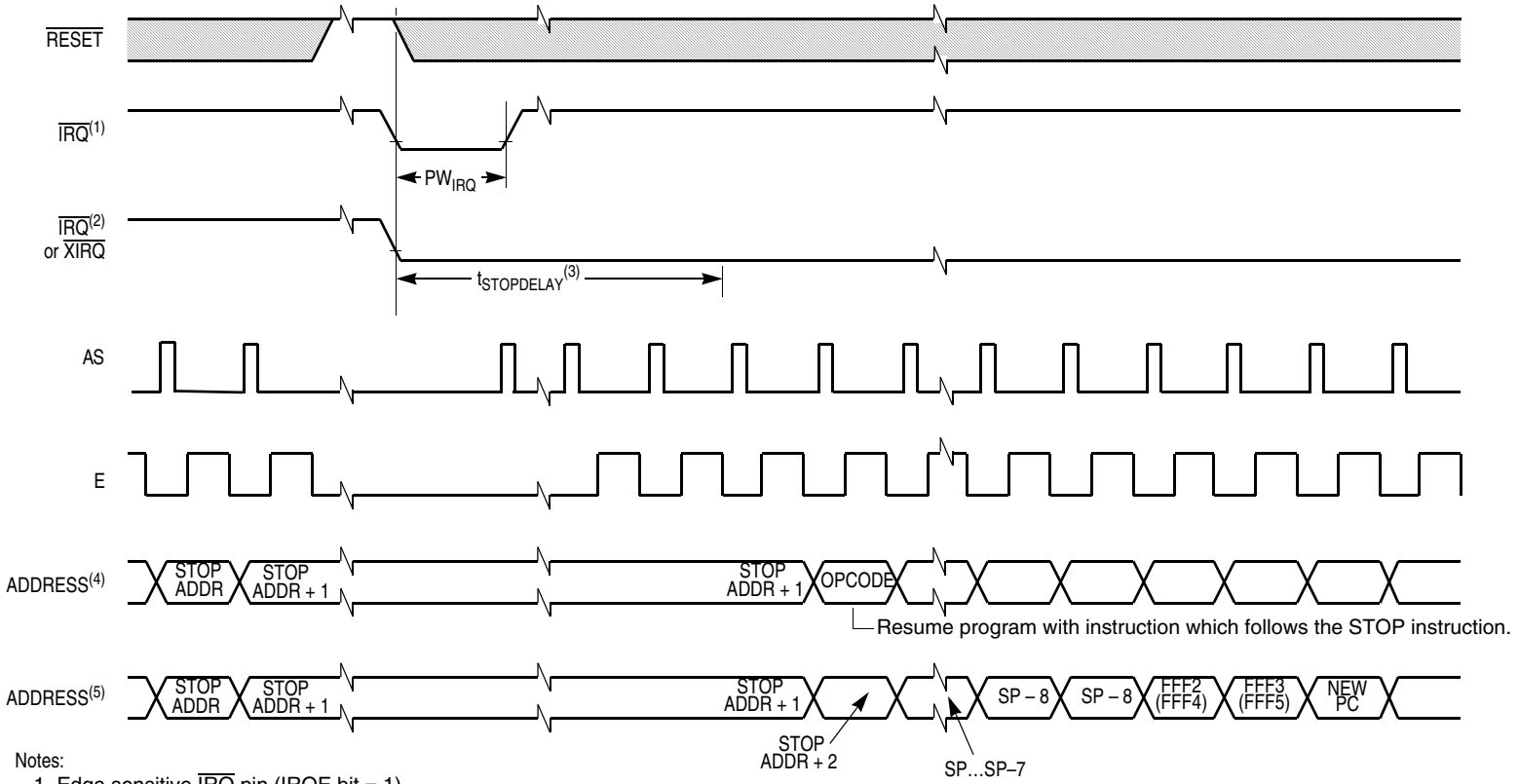
Note:
1. Full test loads are applied during all ac electrical timing measurements.

Figure 9-1. Equivalent Test Load



Note:
1. During ac timing measurements, inputs are driven to 0.4 volts and V_{DD} – 0.8 volts while timing measurements are taken at the 20% and 70% of V_{DD} points.

Figure 9-2. Test Methods



Notes:
1. Edge sensitive $\overline{\text{IRQ}}$ pin (IRQE bit = 1)
2. Edge sensitive $\overline{\text{IRQ}}$ pin (IRQE bit = 0)
3. $t_{STOPDELAY}$ = 4064 t_{cyc} if DLY bit = 1 or 4 t_{cyc} if DLY = 0.
4. $\overline{\text{XIRQ}}$ with X bit in CCR = 1.
5. $\overline{\text{IRQ}}$ or ($\overline{\text{XIRQ}}$ with X bit in CCR = 0)

Figure 9-5. STOP Recovery Timing Diagram

A.6 Ordering Information

MCU	Package	Temperature	MC Order Number	
			2 MHz	3 MHz
MC68HC11D3 (Custom ROM)	44-pin PLCC	–40 to +85°C	MC68HC11D3CFN2	MC68HC11D3CFN3
MC68HC11D0 (No ROM)	44-pin PLCC	–40 to +85°C	MC68HC11D0CFN2	MC68HC11D0CFN3
	44-pin QFP	–40 to +85°C	MC68HC11D0CFB2	MC68HC11D0CFB3

Appendix B
MC68L11D0

B.1 Introduction

The MC68L11D0 is an extended-voltage version of the MC68HC11D0 microcontroller that can operate in applications that require supply voltages as low as 3.0 volts. Operation is identical to that of the MC68HC11D0 (see Appendix A MC68HC11D3 and MC68HC11D0) in all aspects other than electrical parameters, as shown in this appendix.

Features of the MC68HC11D0 include:

- Suitable for battery-powered portable and hand-held applications
- Excellent for use in devices such as remote sensors and actuators
- Operating performance is same at 5 V and 3 V

B.2 MC68L11D0 Electrical Characteristics

The parameters given in Chapter 9 Electrical Characteristics apply to the MC68L11D0 with the exceptions given here.

B.2.1 Functional Operating Temperature Range

Rating	Symbol	Value	Unit
Operating temperature range	T_A	T_L to T_H –20 to +70	°C

B.2.2 DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Max	Unit
Output voltage[2] All outputs except XTAL I_{Load} = ± 10.0 µAAll outputs except XTAL, $\overline{RESET}$, and MODA	V_{OL} V_{OH}	— V_{DD} – 0.1	0.1 —	V
Output high voltage[1] All outputs except XTAL, $\overline{RESET}$, and MODA I_{Load} = – 0.5 mA, V_{DD} = 3.0 V I_{Load} = – 0.8 mA, V_{DD} = 4.5 V	V_{OH}	V_{DD} – 0.8	—	V
Output low voltage All outputs except XTAL I_{Load} = 1.6 mA, V_{DD} = 5.0 V I_{Load} = 1.0 mA, V_{DD} = 3.0 V	V_{OL}	—	0.4	V

The dc electrical table continues on next page.

B.3 Ordering Information

Package	Frequency	Features	MC Order Number
44-pin PLCC	2 MHz	No ROM	MC68L11D0FN2
44-pin QFP	2 MHz	No ROM	MC68L11D0FB2