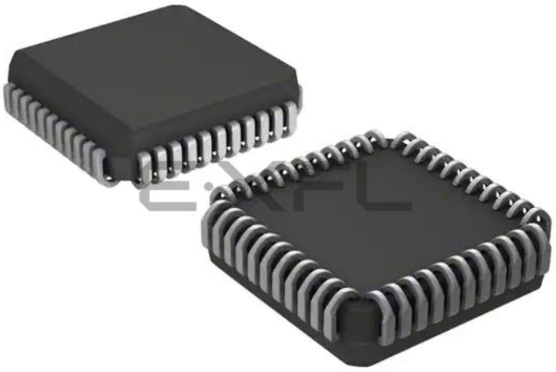


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	2MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	26
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc711d3cfn2

7.5.3 Serial Clock (SCK) . . . 80
7.5.4 Slave Select ($\overline{SS}$) . . . 80
7.6 SPI System Errors . . . 80
7.7 SPI Registers . . . 81
7.7.1 SPI Control Register . . . 81
7.7.2 SPI Status Register . . . 82
7.7.3 SPI Data I/O Register . . . 83

Chapter 8
Programmable Timer

8.1 Introduction . . . 85
8.2 Timer Structure . . . 87
8.3 Input Capture . . . 87
8.3.1 Timer Control 2 Register . . . 89
8.3.2 Timer Input Capture Registers . . . 89
8.3.3 Timer Input Capture 4/Output Compare 5 Register . . . 90
8.4 Output Compare (OC) . . . 91
8.4.1 Timer Output Compare Registers . . . 91
8.4.2 Timer Compare Force Register . . . 93
8.4.3 Output Compare 1 Mask Register . . . 93
8.4.4 Output Compare 1 Data Register . . . 94
8.4.5 Timer Counter Register . . . 94
8.4.6 Timer Control 1 Register . . . 95
8.4.7 Timer Interrupt Mask 1 Register . . . 95
8.4.8 Timer Interrupt Flag 1 Register . . . 96
8.4.9 Timer Interrupt Mask 2 Register . . . 96
8.4.10 Timer Interrupt Flag 2 Register . . . 97
8.5 Real-Time Interrupt . . . 98
8.5.1 Timer Interrupt Mask 2 Register . . . 98
8.5.2 Timer Interrupt Flag 2 Register . . . 99
8.5.3 Pulse Accumulator Control Register . . . 99
8.6 Computer Operating Properly Watchdog Function . . . 100
8.7 Pulse Accumulator . . . 100
8.7.1 Pulse Accumulator Control Register . . . 102
8.7.2 Pulse Accumulator Count Register . . . 103
8.7.3 Pulse Accumulator Status and Interrupt Bits . . . 103

Chapter 9
Electrical Characteristics

9.1 Introduction . . . 105
9.2 Maximum Ratings . . . 105
9.3 Functional Operating Temperature Range . . . 106
9.4 Thermal Characteristics . . . 106
9.5 DC Electrical Characteristics . . . 107
9.6 Control Timing . . . 109
9.7 Peripheral Port Timing . . . 114

Refer to Table 1-1 for details about the functions of the 32 port signals within different operating modes.

Table 1-1. Port Signal Functions

<table>
<tr><th>Port/Bit</th><th>Single-Chip
and Bootstrap Mode</th><th>Expanded Multiplexed
and Special Test Mode</th></tr>
<tr><td>PA0</td><td colspan="2">PA0/IC3</td></tr>
<tr><td>PA1</td><td colspan="2">PA1/IC2</td></tr>
<tr><td>PA2</td><td colspan="2">PA2/IC1</td></tr>
<tr><td>PA3</td><td colspan="2">PA3/OC5/IC4/and-or OC1</td></tr>
<tr><td>PA4[1]</td><td colspan="2">PA4/OC4/and-or OC1</td></tr>
<tr><td>PA5</td><td colspan="2">PA5/OC3/and-or OC1</td></tr>
<tr><td>PA6[1]</td><td colspan="2">PA6/OC2/and-or OC1</td></tr>
<tr><td>PA7</td><td colspan="2">PA7/PAI/and-or OC1</td></tr>
<tr><td>PB0</td><td>PB0</td><td>A8</td></tr>
<tr><td>PB1</td><td>PB1</td><td>A9</td></tr>
<tr><td>PB2</td><td>PB2</td><td>A10</td></tr>
<tr><td>PB3</td><td>PB3</td><td>A11</td></tr>
<tr><td>PB4</td><td>PB4</td><td>A12</td></tr>
<tr><td>PB5</td><td>PB5</td><td>A13</td></tr>
<tr><td>PB6</td><td>PB6</td><td>A14</td></tr>
<tr><td>PB7</td><td>PB7</td><td>A15</td></tr>
<tr><td>PC0</td><td>PC0</td><td>A0/D0</td></tr>
<tr><td>PC1</td><td>PC1</td><td>A1/D1</td></tr>
<tr><td>PC2</td><td>PC2</td><td>A2/D2</td></tr>
<tr><td>PC3</td><td>PC3</td><td>A3/D3</td></tr>
<tr><td>PC4</td><td>PC4</td><td>A4/D4</td></tr>
<tr><td>PC5</td><td>PC5</td><td>A5/D5</td></tr>
<tr><td>PC6</td><td>PC6</td><td>A6/D6</td></tr>
<tr><td>PC7</td><td>PC7</td><td>A7/D7</td></tr>
<tr><td>PD0</td><td colspan="2">PD0/RxD</td></tr>
<tr><td>PD1</td><td colspan="2">PD1/TxD</td></tr>
<tr><td>PD2</td><td colspan="2">PD2/MISO</td></tr>
<tr><td>PD3</td><td colspan="2">PD3/MOSI</td></tr>
<tr><td>PD4</td><td colspan="2">PD4/SCK</td></tr>
<tr><td>PD5</td><td colspan="2">PD5/$\overline{SS}$</td></tr>
<tr><td>PD6</td><td>PD6</td><td>AS</td></tr>
<tr><td>PD7</td><td>PD7</td><td>R/$\overline{W}$</td></tr>
</table>

1. In the 40-pin package, pins PA4 and PA6 are not bonded. Their associated I/O and output compare functions are not available externally. They can still be used as internal software timers, however.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003A	Arm/Reset COP Timer Circuitry Register (COPRST) See page 48.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$003B	PROM Programming Control Register (PPROG) See page 32.	Read: Write:	MBE	0	ELAT	EXCOL	EXROW	0	0	PGM
		Reset:	0	0	0	0	0	0	0	0
$003C	Highest Priority I-Bit Interrupt and Miscellaneous Register (HPRIO) See page 58.	Read: Write:	RBOOT	SMOD (read; write unimplemented)	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0
		Reset:	Note 1				0	1	0	1

1. The values of the RBOOT, SMOD, IRVNE, and MDA bits at reset depend on the mode during initialization. Refer to Table 4-3. Hardware Mode Select Summary.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003D	RAM and I/O Mapping Register (INIT) See page 29.	Read: Write:	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
		Reset:	0	0	0	0	0	0	0	1
$003E	Test 1 Register (TEST)	Read: Write:	TILOP	0	OCC4	CBYP	DISR	FCM	FCOP	0
		Reset:	0	0	0	0	0	0	0	0
$003F	System Configuration Register (CONFIG) See page 30.	Read: Write:	0	0	0	0	0	NOCOP	ROMON	0
		Reset:	0	0	0	0	0	U	U	0

(shaded) = Unimplemented R = Reserved U = Unaffected

Figure 2-2. Register and Control Bit Assignments (Sheet 5 of 5)

2.3.2 RAM and I/O Mapping Register

The random-access memory (RAM) and input/output (I/O) mapping register (INIT) is a special-purpose 8-bit register that is used during initialization to change the default locations of RAM and control registers within the MCU memory map. It can be written to only once within the first 64 E-clock cycles after a reset in normal modes. Thereafter, it becomes a read-only register.

Address: $003D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
Reset:	0	0	0	0	0	0	0	0

Figure 2-3. RAM and I/O Mapping Register (INIT)

Chapter 3
Central Processor Unit (CPU)

3.1 Introduction

This section presents information on M68HC11 central processor unit (CPU):

- Architecture
- Data types
- Addressing modes
- Instruction set
- Special operations such as subroutine calls and interrupts

The CPU is designed to treat all peripheral, input/output (I/O), and memory locations identically as addresses in the 64-Kbyte memory map. This is referred to as memory-mapped I/O. I/O has no instructions separate from those used by memory. This architecture also allows accessing an operand from an external memory location with no execution time penalty.

3.2 CPU Registers

M68HC11 CPU registers are an integral part of the CPU and are not addressed as if they were memory locations. The seven registers, discussed in the following paragraphs, are shown in Figure 3-1.

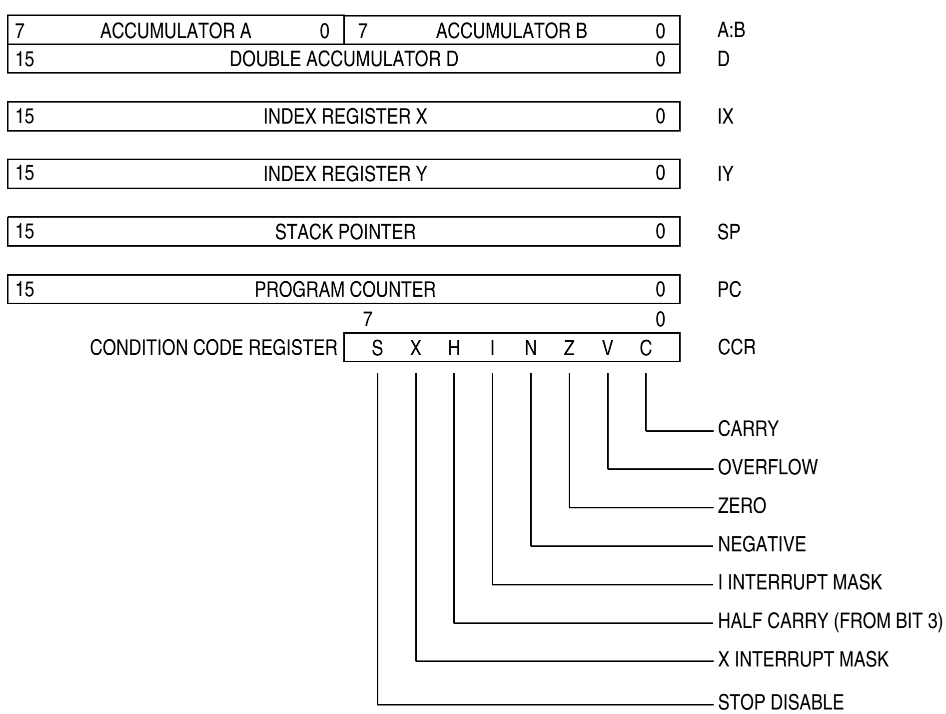


Figure 3-1. Programming Model

At the end of the interrupt service routine, a return-from interrupt (RTI) instruction is executed. The RTI instruction causes the saved registers to be pulled off the stack in reverse order. Program execution resumes at the return address.

Certain instructions push and pull the A and B accumulators and the X and Y index registers and are often used to preserve program context. For example, pushing accumulator A onto the stack when entering a subroutine that uses accumulator A and then pulling accumulator A off the stack just before leaving the subroutine ensures that the contents of a register will be the same after returning from the subroutine as it was before starting the subroutine.

3.2.5 Program Counter (PC)

The program counter, a 16-bit register, contains the address of the next instruction to be executed. After reset, the program counter is initialized from one of six possible vectors, depending on operating mode and the cause of reset.
See Table 3-1.

Table 3-1. Reset Vector Comparison

Mode	POR or $\overline{\text{RESET}}$ Pin	Clock Monitor	COP Watchdog
Normal	$FFFE, $FFFF	$FFFC, $FFFD	$FFFA, $FFFB
Test or boot	$BFFE, $BFFF	$BFFC, $FFFD	$BFFA, $FFFB

3.2.6 Condition Code Register (CCR)

This 8-bit register contains:

- Five condition code indicators (C, V, Z, N, and H)
- Two interrupt masking bits ($\overline{\text{IRQ}}$ and $\overline{\text{XIRQ}}$)
- One stop disable bit (S)

In the M68HC11 CPU, condition codes are updated automatically by most instructions. For example, load accumulator A (LDAA) and store accumulator A (STAA) instructions automatically set or clear the N, Z, and V condition code flags. Pushes, pulls, add B to X (ABX), add B to Y (ABY), and transfer/exchange instructions do not affect the condition codes. Refer to Table 3-2, which shows what condition codes are affected by a particular instruction.

3.2.6.1 Carry/Borrow (C)

The C bit is set if the arithmetic logic unit (ALU) performs a carry or borrow during an arithmetic operation. The C bit also acts as an error flag for multiply and divide operations. Shift and rotate instructions operate with and through the carry bit to facilitate multiple-word shift operations.

3.2.6.2 Overflow (V)

The overflow bit is set if an operation causes an arithmetic overflow. Otherwise, the V bit is cleared.

3.2.6.3 Zero (Z)

The Z bit is set if the result of an arithmetic, logic, or data manipulation operation is 0. Otherwise, the Z bit is cleared. Compare instructions do an internal implied subtraction and the condition codes, including Z, reflect the results of that subtraction. A few operations (INX, DEX, INY, and DEY) affect the Z bit and no other condition flags. For these operations, only = and ≠ conditions can be determined.

Table 3-2. Instruction Set (Sheet 3 of 8)

Mnemonic	Operation	Description	Addressing Mode	Instruction Opcode	Instruction Operand	Instruction Cycles	S	X	H	I	N	Z	V	C
BITB (opr)	Bit(s) Test B with Memory	B • M	B IMM B DIR B EXT B IND,X B IND,Y	C5 D5 F5 E5 18 E5	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
BLE (rel)	Branch if Δ Zero	? Z + (N ⊕ V) = 1	REL	2F	rr	3	—	—	—	—	—	—	—	—
BLO (rel)	Branch if Lower	? C = 1	REL	25	rr	3	—	—	—	—	—	—	—	—
BLS (rel)	Branch if Lower or Same	? C + Z = 1	REL	23	rr	3	—	—	—	—	—	—	—	—
BLT (rel)	Branch if < Zero	? N ⊕ V = 1	REL	2D	rr	3	—	—	—	—	—	—	—	—
BMI (rel)	Branch if Minus	? N = 1	REL	2B	rr	3	—	—	—	—	—	—	—	—
BNE (rel)	Branch if not = Zero	? Z = 0	REL	26	rr	3	—	—	—	—	—	—	—	—
BPL (rel)	Branch if Plus	? N = 0	REL	2A	rr	3	—	—	—	—	—	—	—	—
BRA (rel)	Branch Always	? 1 = 1	REL	20	rr	3	—	—	—	—	—	—	—	—
BRCLR(opr) (msk) (rel)	Branch if Bit(s) Clear	? M • mm = 0	DIR IND,X IND,Y	13 1F 18 1F	dd mm rr ff mm rr ff mm rr	6 7 8	—	—	—	—	—	—	—	—
BRN (rel)	Branch Never	? 1 = 0	REL	21	rr	3	—	—	—	—	—	—	—	—
BRSET(opr) (msk) (rel)	Branch if Bit(s) Set	? $(\overline{M})$ • mm = 0	DIR IND,X IND,Y	12 1E 18 1E	dd mm rr ff mm rr ff mm rr	6 7 8	—	—	—	—	—	—	—	—
BSET (opr) (msk)	Set Bit(s)	M + mm ⇒ M	DIR IND,X IND,Y	14 1C 18 1C	dd mm ff mm ff mm	6 7 8	—	—	—	—	Δ	Δ	0	—
BSR (rel)	Branch to Subroutine	See Figure 3-2	REL	8D	rr	6	—	—	—	—	—	—	—	—
BVC (rel)	Branch if Overflow Clear	? V = 0	REL	28	rr	3	—	—	—	—	—	—	—	—
BVS (rel)	Branch if Overflow Set	? V = 1	REL	29	rr	3	—	—	—	—	—	—	—	—
CBA	Compare A to B	A – B	INH	11	—	2	—	—	—	—	Δ	Δ	Δ	Δ
CLC	Clear Carry Bit	0 ⇒ C	INH	0C	—	2	—	—	—	—	—	—	—	0
CLI	Clear Interrupt Mask	0 ⇒ I	INH	0E	—	2	—	—	—	0	—	—	—	—
CLR (opr)	Clear Memory Byte	0 ⇒ M	EXT IND,X IND,Y	7F 6F 18 6F	hh ll ff ff	6 6 7	—	—	—	—	0	1	0	0
CLRA	Clear Accumulator A	0 ⇒ A	A INH	4F	—	2	—	—	—	—	0	1	0	0
CLRB	Clear Accumulator B	0 ⇒ B	B INH	5F	—	2	—	—	—	—	0	1	0	0
CLV	Clear Overflow Flag	0 ⇒ V	INH	0A	—	2	—	—	—	—	—	—	0	—
CMPA (opr)	Compare A to Memory	A – M	A IMM A DIR A EXT A IND,X A IND,Y	81 91 B1 A1 18 A1	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ
CMPB (opr)	Compare B to Memory	B – M	B IMM B DIR B EXT B IND,X B IND,Y	C1 D1 F1 E1 18 E1	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ
COM (opr)	Ones Complement Memory Byte	\$FF – M ⇒ M	EXT IND,X IND,Y	73 63 18 63	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	0	1

Table 3-2. Instruction Set (Sheet 8 of 8)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
TBA	Transfer B to A	B ⇒ A	INH	17	—	2	—	—	—	—	Δ	Δ	0	—
TEST	TEST (Only in Test Modes)	Address Bus Counts	INH	00	—	*	—	—	—	—	—	—	—	—
TPA	Transfer CC Register to A	CCR ⇒ A	INH	07	—	2	—	—	—	—	—	—	—	—
TST (opr)	Test for Zero or Minus	M – 0	EXT IND,X IND,Y	7D 6D 18 6D	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	0	0
TSTA	Test A for Zero or Minus	A – 0	A INH	4D	—	2	—	—	—	—	Δ	Δ	0	0
TSTB	Test B for Zero or Minus	B – 0	B INH	5D	—	2	—	—	—	—	Δ	Δ	0	0
TSX	Transfer Stack Pointer to X	SP + 1 ⇒ IX	INH	30	—	3	—	—	—	—	—	—	—	—
TSY	Transfer Stack Pointer to Y	SP + 1 ⇒ IY	INH	18 30	—	4	—	—	—	—	—	—	—	—
TXS	Transfer X to Stack Pointer	IX – 1 ⇒ SP	INH	35	—	3	—	—	—	—	—	—	—	—
TYS	Transfer Y to Stack Pointer	IY – 1 ⇒ SP	INH	18 35	—	4	—	—	—	—	—	—	—	—
WAI	Wait for Interrupt	Stack Regs & WAIT	INH	3E	—	**	—	—	—	—	—	—	—	—
XGDX	Exchange D with X	IX ⇒ D, D ⇒ IX	INH	8F	—	3	—	—	—	—	—	—	—	—
XGDY	Exchange D with Y	IY ⇒ D, D ⇒ IY	INH	18 8F	—	4	—	—	—	—	—	—	—	—

Cycle

- * Infinity or until reset occurs
- ** 12 cycles are used beginning with the opcode fetch. A wait state is entered which remains in effect for an integer number of MPU E-clock cycles (n) until an interrupt is recognized. Finally, two additional cycles are used to fetch the appropriate interrupt vector (14 + n total).

Operands

- dd = 8-bit direct address ($0000–$00FF) (high byte assumed to be $00)
- ff = 8-bit positive offset $00 (0) to $FF (255) (is added to index)
- hh = High-order byte of 16-bit extended address
- ii = One byte of immediate data
- jj = High-order byte of 16-bit immediate data
- kk = Low-order byte of 16-bit immediate data
- ll = Low-order byte of 16-bit extended address
- mm = 8-bit mask (set bits to be affected)
- rr = Signed relative offset $80 (–128) to $7F (+127) (offset relative to address following machine code offset byte)

Operators

- ( ) Contents of register shown inside parentheses
- ⇐ Is transferred to
- ⇑ Is pulled from stack
- ⇓ Is pushed onto stack
- • Boolean AND
- \+ Arithmetic addition symbol except where used as inclusive-OR symbol in Boolean formula
- ⊕ Exclusive-OR
- * Multiply
- : Concatenation
- – Arithmetic subtraction symbol or negation symbol (two's complement)

Condition Codes

- — Bit not changed
- 0 Bit always cleared
- 1 Bit always set
- Δ Bit cleared or set, depending on operation
- ↓ Bit can be cleared, cannot become set

4.3.6 Highest Priority I Interrupt and Miscellaneous Register (HPRIO)

Four bits of this register (PSEL3–PSEL0) are used to select one of the I bit related interrupt sources and to elevate it to the highest I bit masked position of the priority resolution circuit. In addition, four miscellaneous system control bits are included in this register.

Address: $003C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0
Write:								
Reset:	Note 1				0	1	0	1

1. The values of the RBOOT, SMOD, IRVNE, and MDA bits at reset depend on the mode during initialization. Refer to Table 4-3.

Figure 4-7. Highest Priority I-Bit Interrupt and Miscellaneous Register (HPRIO)

RBOOT — Read Bootstrap ROM

This bit can be read at any time. It can be written only in special modes (SMOD = 1). In special bootstrap mode, it is set during reset. Reset clears it in all other modes.

1 = Bootloader ROM is enabled in the memory map at $BF00–$BFFF.
0 = Bootloader ROM is disabled and is not in the memory map.

SMOD and MDA — Special Mode Select and Mode Select A

These two bits can be read at any time.These bits reflect the status of the MODA and MODB input pins at the rising edge of reset. SMOD may be written only in special modes. It cannot be written to a 1 after being cleared without an interim reset. MDA may be written at any time in special modes, but only once in normal modes. An interpretation of the values of these two bits is shown in Table 4-3.

Table 4-3. Hardware Mode Select Summary

Inputs		Mode	Latched at Reset	
MODB	MODA		SMOD	MDA
1	0	Single chip	0	0
1	1	Expanded multiplexed	0	1
0	0	Special bootstrap	1	0
0	1	Special test	1	1

IRVNE — Internal Read Visibility/Not E

This bit may be read at any time. It may be written once in any mode. IRVNE is set during reset in special test mode only, and cleared by reset in the other modes.

1 = Data from internal reads is driven out on the external data bus in expanded modes.
0 = Data from internal reads is not visible on the external data bus.

As shown in the table, in single-chip and bootstrap modes IRVNE determines whether the E clock is driven out or forced low.

1 = E pin driven low
0 = E clock driven out of the chip

Chapter 6
Serial Communications Interface (SCI)

6.1 Introduction

The serial communications interface (SCI) is a universal asynchronous receiver transmitter (UART), one of two independent serial input/output (I/O) subsystems in the MC68HC711D3. It has a standard non-return to zero (NRZ) format (one start, eight or nine data, and one stop bit). Several baud rates are available. The SCI transmitter and receiver are independent, but use the same data format and bit rate.

6.2 Data Format

The serial data format requires these conditions:

- An idle line in the high state before transmission or reception of a message
- A start bit, logic 0, transmitted or received, that indicates the start of each character
- Data that is transmitted and received least significant bit (LSB) first
- A stop bit, logic 1, used to indicate the end of a frame. A frame consists of a start bit, a character of eight or nine data bits, and a stop bit.
- A break, defined as the transmission or reception of a logic 0 for some multiple number of frames

Selection of the word length is controlled by the M bit in the SCI control register 1 (SCCR1).

6.3 Transmit Operation

The SCI transmitter includes a parallel transmit data register (SCDR) and a serial shift register that puts data from the SCDR into serial form. The contents of the serial shift register can only be written through the SCDR. This double-buffered operation allows a character to be shifted out serially while another character is waiting in the SCDR to be transferred into the serial shift register. The output of the serial shift register is applied to PD1 as long as transmission is in progress or the transmit enable (TE) bit of serial communication control register 2 (SCCR2) is set. The block diagram, Figure 6-1, shows the transmit serial shift register and the buffer logic at the top of the figure.

6.4 Receive Operation

During receive operations, the transmit sequence is reversed. The serial shift register receives data and transfers it to a parallel receive data register (SCDR) as a complete word. Refer to Figure 6-2. This double-buffered operation allows a character to be shifted in serially while another character is already in the SCDR. An advanced data recovery scheme distinguishes valid data from noise in the serial data stream. The data input is selectively sampled to detect receive data, and a majority voting circuit determines the value and integrity of each bit.

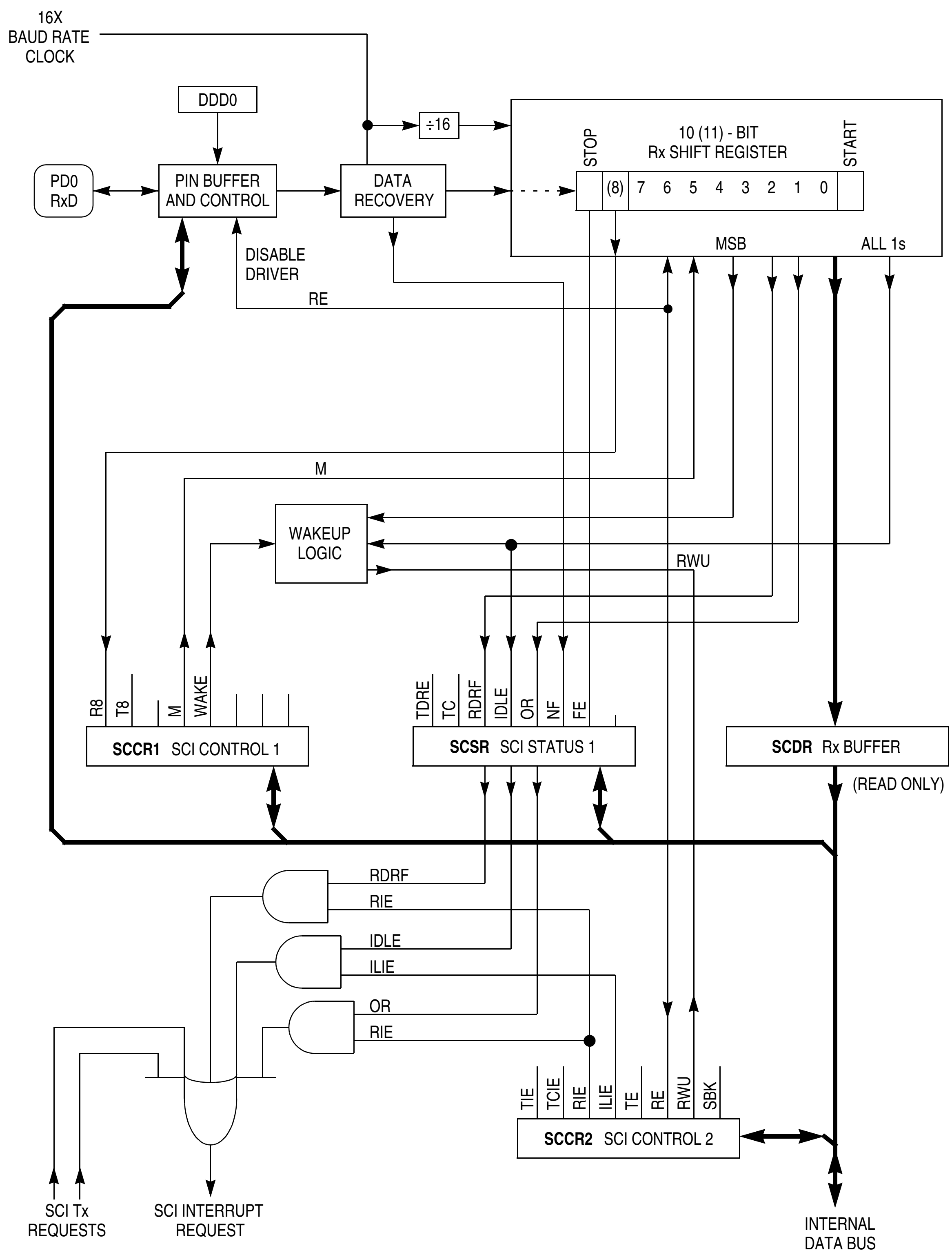


Figure 6-2. SCI Receiver Block Diagram

IDLE — Idle Line Detected Flag

This flag is set if the RxD line is idle. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again. The IDLE flag is inhibited when RWU = 1. Clear IDLE by reading SCSR with IDLE set and then reading SCDR.

0 = RxD line active
1 = RxD line idle

OR — Overrun Error Flag

OR is set if a new character is received before a previously received character is read from SCDR. Clear the OR flag by reading SCSR with OR set and then reading SCDR.

0 = No overrun
1 = Overrun detected

NF — Noise Error Flag

NF is set if majority sample logic detects anything other than a unanimous decision. Clear NF by reading SCSR with NF set and then reading SCDR.

0 = Unanimous decision
1 = Noise detected

FE — Framing Error Bit

FE is set when a 0 is detected where a stop bit was expected. Clear the FE flag by reading SCSR with FE set and then reading SCDR.

0 = Stop bit detected
1 = Zero detected

6.7.5 Baud Rate Register

The baud rate register (BAUD) is used to select different baud rates for the SCI system. The SCP1 and SCP0 bits function as a prescaler for the SCR2–SCR0 bits. Together, these five bits provide multiple baud rate combinations for a given crystal frequency. Normally, this register is written once during initialization. The prescaler is set to its fastest rate by default out of reset and can be changed at any time. Refer to Table 6-1 and Table 6-2 for normal baud rate selections.

Address: $002B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
Reset:	0	0	0	0	0	U	U	U

U = Unaffected

Figure 6-7. Baud Rate Register (BAUD)

TCLR — Clear Baud Rate Counters (Test)

RCKB — SCI Baud Rate Clock Check (Test)

8.3.1 Timer Control 2 Register

Use the control bits of timer control 2 register (TCTL2) to program input capture functions to detect a particular edge polarity on the corresponding timer input pin. Each of the input capture functions can be independently configured to detect rising edges only, falling edges only, any edge (rising or falling), or to disable the input capture function. The input capture functions operate independently of each other and can capture the same TCNT value if the input edges are detected within the same timer count cycle.

Address: $0021

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
Reset:	0	0	0	0	0	0	0	0

Figure 8-3. Timer Control 2 Register (TCTL2)

EDGxB and EDGxA — Input Capture Edge Control

There are four pairs of these bits. Each pair is cleared to 0 by reset and must be encoded to configure the corresponding input capture edge detector circuit. IC4 functions only if the I4/O5 bit in PACTL is set. Refer to Table 8-2 for timer control configuration.

Table 8-2. Timer Control Configuration

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge

8.3.2 Timer Input Capture Registers

When an edge has been detected and synchronized, the 16-bit free-running counter value is transferred into the input capture register pair as a single 16-bit parallel transfer. Timer counter value captures and timer counter incrementing occur on opposite half-cycles of the phase two clock so that the count value is stable whenever a capture occurs. The timer input capture (TICx) registers are not affected by reset. Input capture values can be read from a pair of 8-bit read-only registers. A read of the high-order byte of an input capture register pair inhibits a new capture transfer for one bus cycle. If a double-byte read instruction, such as LDD, is used to read the captured value, coherency is assured. When a new input capture occurs immediately after a high-order byte read, transfer is delayed for an additional cycle but the value is not lost.

Address: $0010 — TIC1 (High)

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	Unaffected by reset							

= Unimplemented

Figure 8-4. Timer Input Capture Registers (TICx)

8.4.4 Output Compare 1 Data Register

Use this register with OC1 to specify the data that is to be stored on the affected pin of port A after a successful OC1 compare. When a successful OC1 compare occurs, a data bit in OC1D is stored in the corresponding bit of port A for each bit that is set in OC1M.

Address: $000D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 8-9. Output Compare 1 Data Register (OC1D)

If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1 compares.

Bits 2–0 — Not implemented; always read 0.

8.4.5 Timer Counter Register

The 16-bit read-only timer count register (TCNT) contains the prescaled value of the 16-bit timer. A full counter read addresses the most significant byte (MSB) first. A read of this address causes the least significant byte (LSB) to be latched into a buffer for the next CPU cycle so that a double-byte read returns the full 16-bit state of the counter at the time of the MSB read cycle.

Address: $000E — TCNT High

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 08
Write:								
Reset:	0	0	0	0	0	0	0	0

Address: $000F — TCNT Low

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	0	0	0	0	0	0	0	0

(shaded) = Unimplemented

Figure 8-10. Timer Counter Registers (TCNT)

In normal modes, TCNT is read-only.

PR1 and PR0 — Timer Prescaler Select Bits
Refer to Table 8-4.

NOTE
Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

8.5.2 Timer Interrupt Flag 2 Register

Bits of the timer interrupt flag 2 register (TFLG2) indicate the occurrence of timer system events. Coupled with the four high-order bits of TMSK2, the bits of TFLG2 allow the timer subsystem to operate in either a polled or interrupt driven system. Each bit of TFLG2 corresponds to a bit in TMSK2 in the same position.

Address: $0025

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOF	RTIF	PAOVF	PAIF	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 8-17. Timer Interrupt Flag 2 Register (TFLG2)

Clear flags by writing a 1 to the corresponding bit position(s).

TOF — Timer Overflow Interrupt Flag
Set when TCNT changes from $FFFF to $0000

RTIF — Real-Time Interrupt Flag
The RTIF status bit is automatically set to 1 at the end of every RTI period. To clear RTIF, write a byte to TFLG2 with bit 6 set.

PAOVF — Pulse Accumulator Overflow Interrupt Flag
Refer to 8.7 Pulse Accumulator.

PAIF — Pulse Accumulator Input Edge Interrupt Flag
Refer to 8.7 Pulse Accumulator.

Bits 3–0 — Not implemented
Always read 0.

8.5.3 Pulse Accumulator Control Register

Bits RTR1 and RTR0 of the pulse accumulator control register (PACTL) select the rate for the real-time interrupt system. Bit DDRA3 determines whether port A bit three is an input or an output when used for general-purpose I/O. The remaining bits control the pulse accumulator.

Address: $0026

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
Reset:	0	0	0	0	0	0	0	0

Figure 8-18. Pulse Accumulator Control Register (PACTL)

DDRA7 — Data Direction Control for Port A Bit 7
Refer to 8.7 Pulse Accumulator.

PAEN — Pulse Accumulator System Enable Bit
Refer to 8.7 Pulse Accumulator.

PAMOD — Pulse Accumulator Mode Bit
Refer to 8.7 Pulse Accumulator.

PEDGE — Pulse Accumulator Edge Control Bit
Refer to 8.7 Pulse Accumulator.

DDRA3 — Data Direction Register for Port A Bit 3
Refer to Chapter 5 Input/Output (I/O) Ports.

I4/O5 — Input Capture 4/Output Compare 5 Bit
Refer to 8.3 Input Capture.

RTR1 and RTR0 — RTI Interrupt Rate Select Bits
These two bits determine the rate at which the RTI system requests interrupts. The RTI system is driven by an E divided by 2^{13} rate clock that is compensated so it is independent of the timer prescaler. These two control bits select an additional division factor. See Table 8-6.

Table 8-6. Real-Time Interrupt Rates

RTR1 and RTR0	E = 1 MHz	E = 2 MHz	E = 3 MHz	E = X MHz
0 0	2.731 ms	4.096 ms	8.192 ms	$(E/2^{13})$
0 1	5.461 ms	8.192 ms	16.384 ms	$(E/2^{14})$
1 0	10.923 ms	16.384 ms	32.768 ms	$(E/2^{15})$
1 1	21.845 ms	32.768 ms	65.536 ms	$(E/2^{16})$

8.6 Computer Operating Properly Watchdog Function

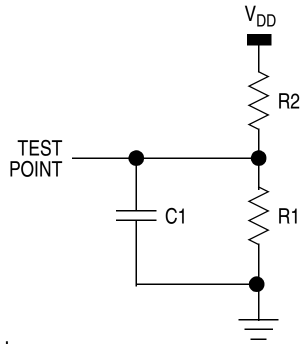
The clocking chain for the COP function, tapped off of the main timer divider chain, is only superficially related to the main timer system. The CR1 and CR0 bits in the OPTION register and the NOCOP bit in the CONFIG register determine the status of the COP function. Refer to Chapter 4 Resets, Interrupts, and Low-Power Modes for a more detailed discussion of the COP function.

8.7 Pulse Accumulator

The MC68HC711D3 has an 8-bit counter that can be configured to operate either as a simple event counter or for gated time accumulation, depending on the state of the PAMOD bit in the PACTL register. Refer to the pulse accumulator block diagram, Figure 8-19.

In the event counting mode, the 8-bit counter is clocked to increasing values by an external pin. The maximum clocking rate for the external event counting mode is the E clock divided by two. In gated time accumulation mode, a free-running E-clock ÷ 64 signal drives the 8-bit counter, but only while the external PAI pin is activated. Refer to Table 8-7. The pulse accumulator counter can be read or written at any time.

Pulse accumulator control bits are also located within two timer registers, TMSK2 and TFLG2, as described here.



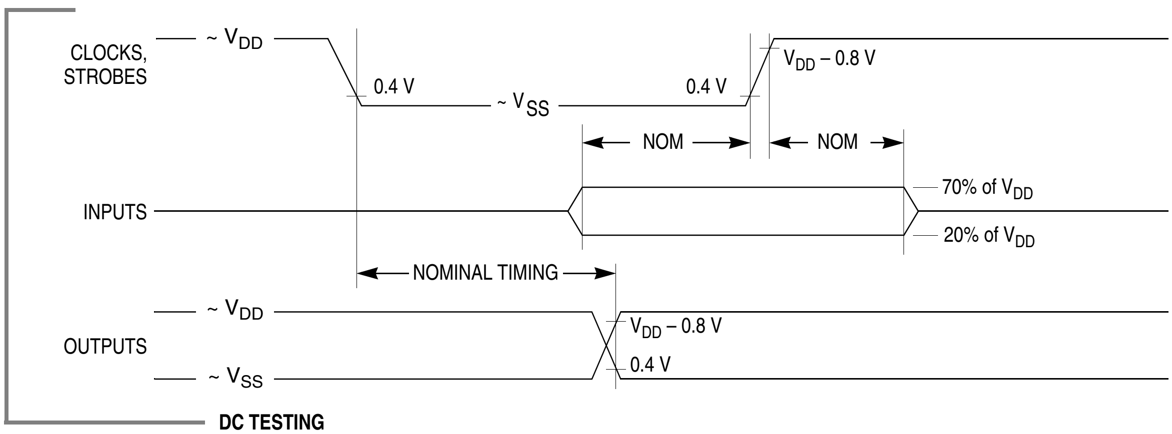
EQUIVALENT TEST LOAD[(1)]

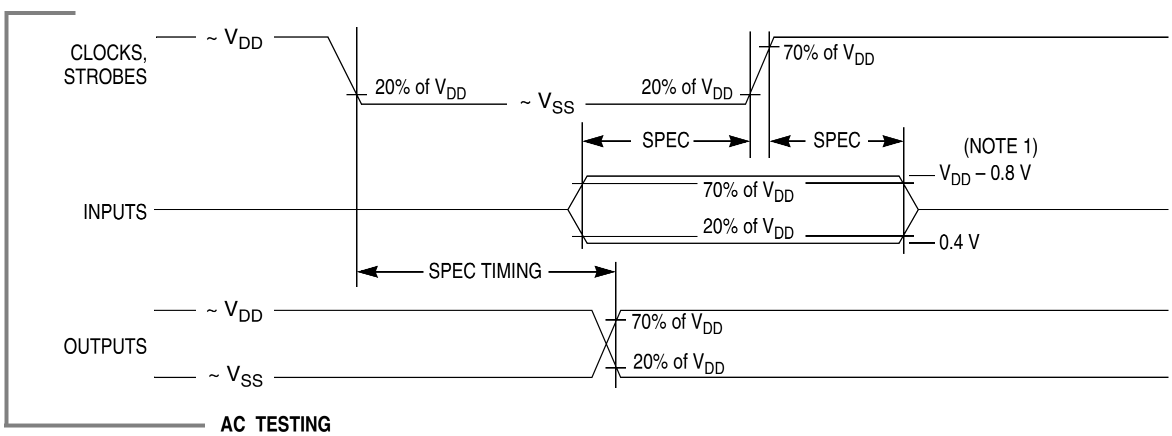
Pins	R1	R2	C1
PA3–PA7 PB0–PB7 PC0–PC7 PD0, PD5–PD7 E	3.26 K	2.38 K	90 pF
PD1—PD4	3.26 K	2.38 K	200 pF

Note:

1. Full test loads are applied during all ac electrical timing measurements.

Figure 9-1. Equivalent Test Load

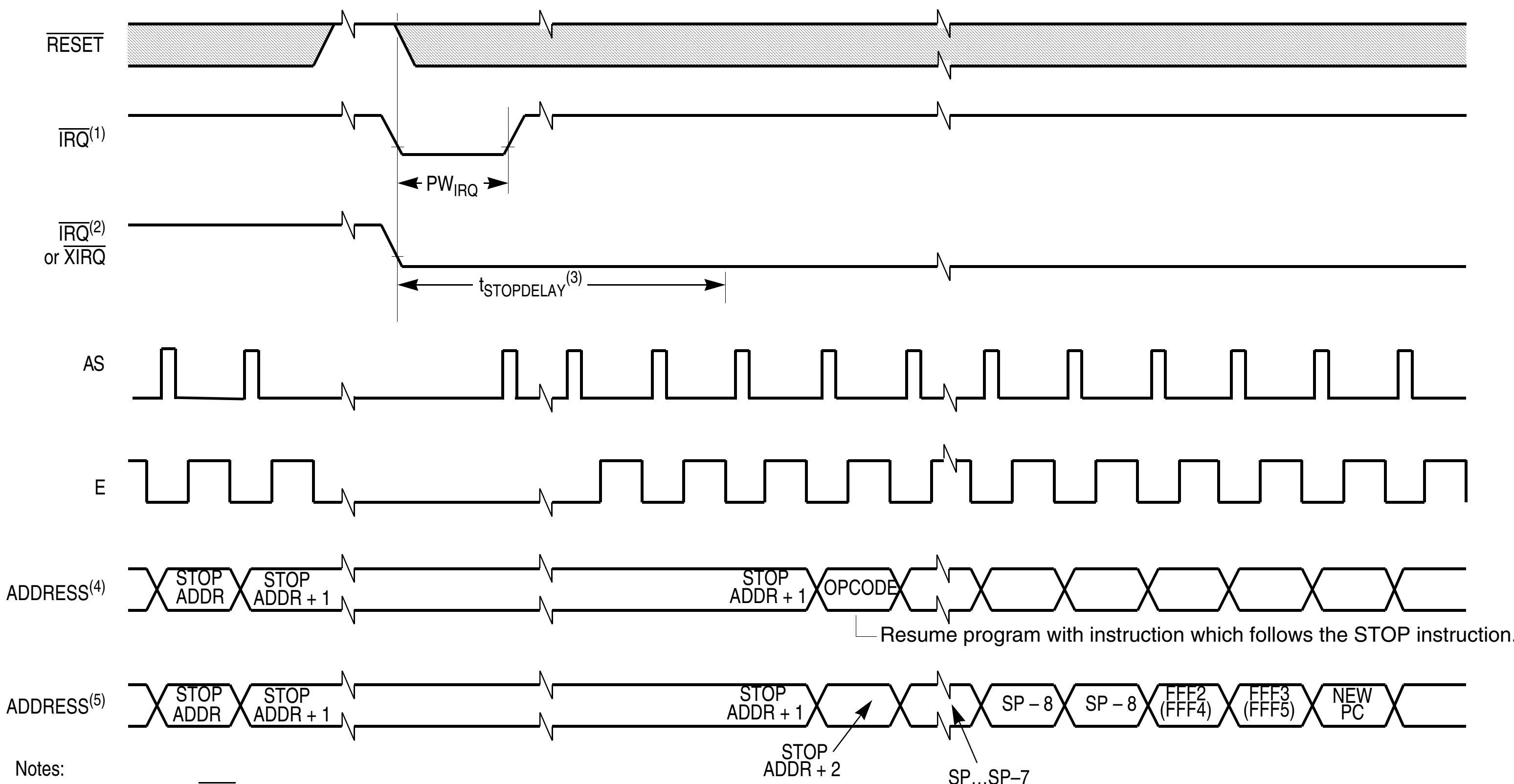




Note:

1. During ac timing measurements, inputs are driven to 0.4 volts and V_{DD} – 0.8 volts while timing measurements are taken at the 20% and 70% of V_{DD} points.

Figure 9-2. Test Methods



Notes:
1. Edge sensitive IRQ pin (IRQE bit = 1)
2. Edge sensitive IRQ pin (IRQE bit = 0)
3. $t_{STOPDELAY}$ = 4064 t_{cyc} if DLY bit = 1 or 4 t_{cyc} if DLY = 0.
4. XIRQ with X bit in CCR = 1.
5. IRQ or (XIRQ with X bit in CCR = 0)

Figure 9-5. STOP Recovery Timing Diagram

Appendix A
MC68HC11D3 and MC68HC11D0

A.1 Introduction

The MC68HC11D3 and MC68HC11D0 are read-only memory (ROM) based high-performance microcontrollers (MCU) based on the MC68HC11E9 design. Members of the Dx series are derived from the same mask and feature a high-speed multiplexed bus capable of running at up to 3 MHz and a fully static design that allows operations at frequencies to dc. The only difference between the MCUs in the Dx series is whether the ROM has been tested and guaranteed.

The information contained in this document applies to both the MC68HC11D3 and MC68HC11D0 with the differences given in this appendix.

Features of the MC68HC11D3 and MC68HC11D0 include:

- 4 Kbytes of on-chip ROM (MC68HC11D3)
- 0 bytes of on-chip ROM (MC68HC11D0)
- 192 bytes of on-chip random-access memory (RAM) all saved during standby
- 16-bit timer system:
  - Three input capture (IC) channels
  - Four output compare (OC) channels
  - One IC or OC software-selectable channel
- 32 input/output (I/O) pins:
  - 26 bidirectional I/O pins
  - 3 input-only pins
  - 3 output-only pins
- Available in these packages:
  - 44-pin plastic leaded chip carrier (PLCC)
  - 44-pin quad flat pack (QFP)

A.2 Block Diagram

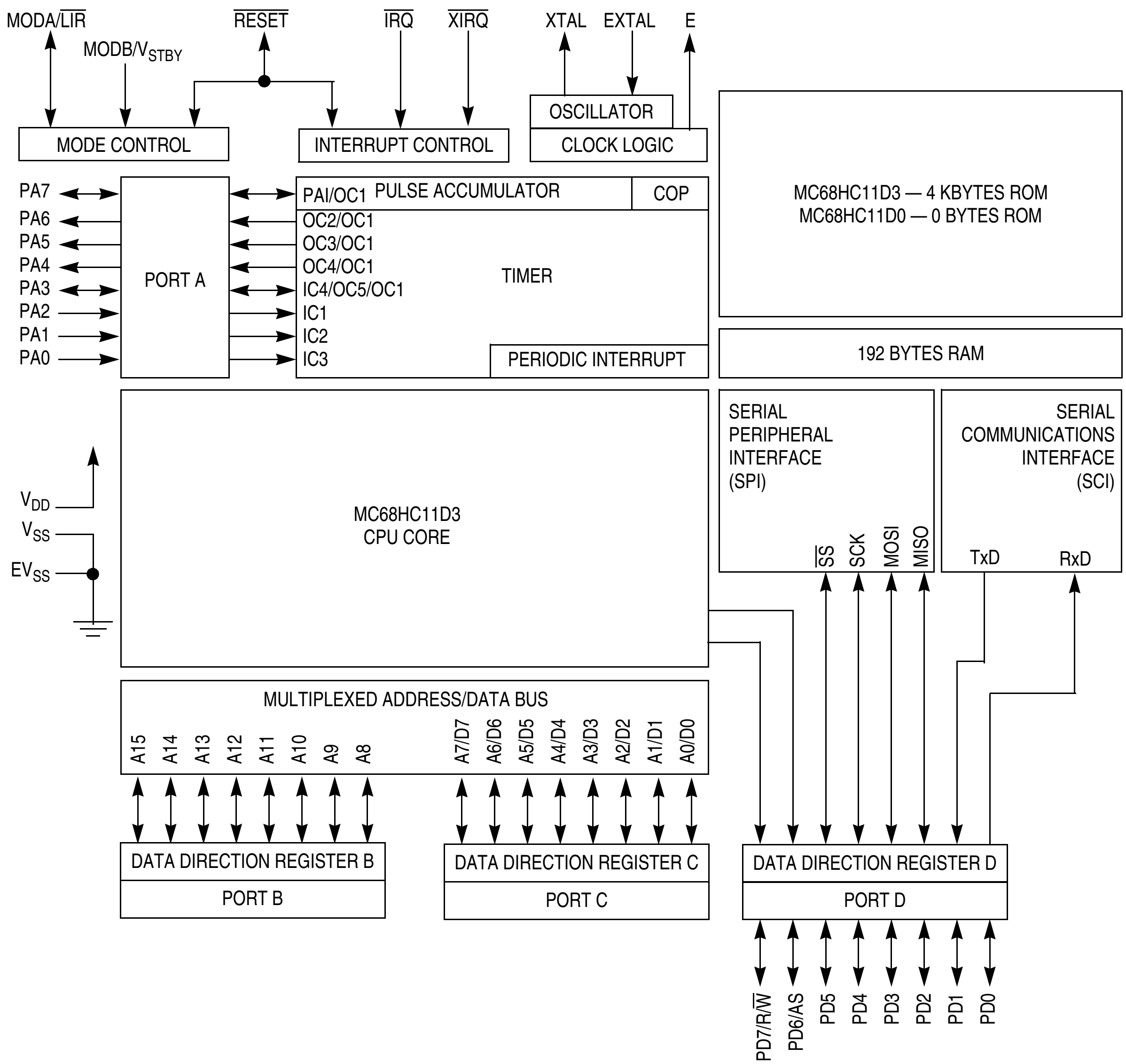


Figure A-1. MC68HC11D3 Block Diagram

B.3 Ordering Information

Package	Frequency	Features	MC Order Number
44-pin PLCC	2 MHz	No ROM	MC68L11D0FN2
44-pin QFP	2 MHz	No ROM	MC68L11D0FB2