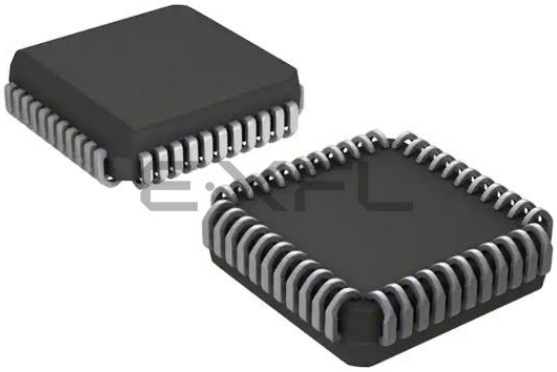

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	2MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	26
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc711d3cfne2

MC68HC711D3

Data Sheet

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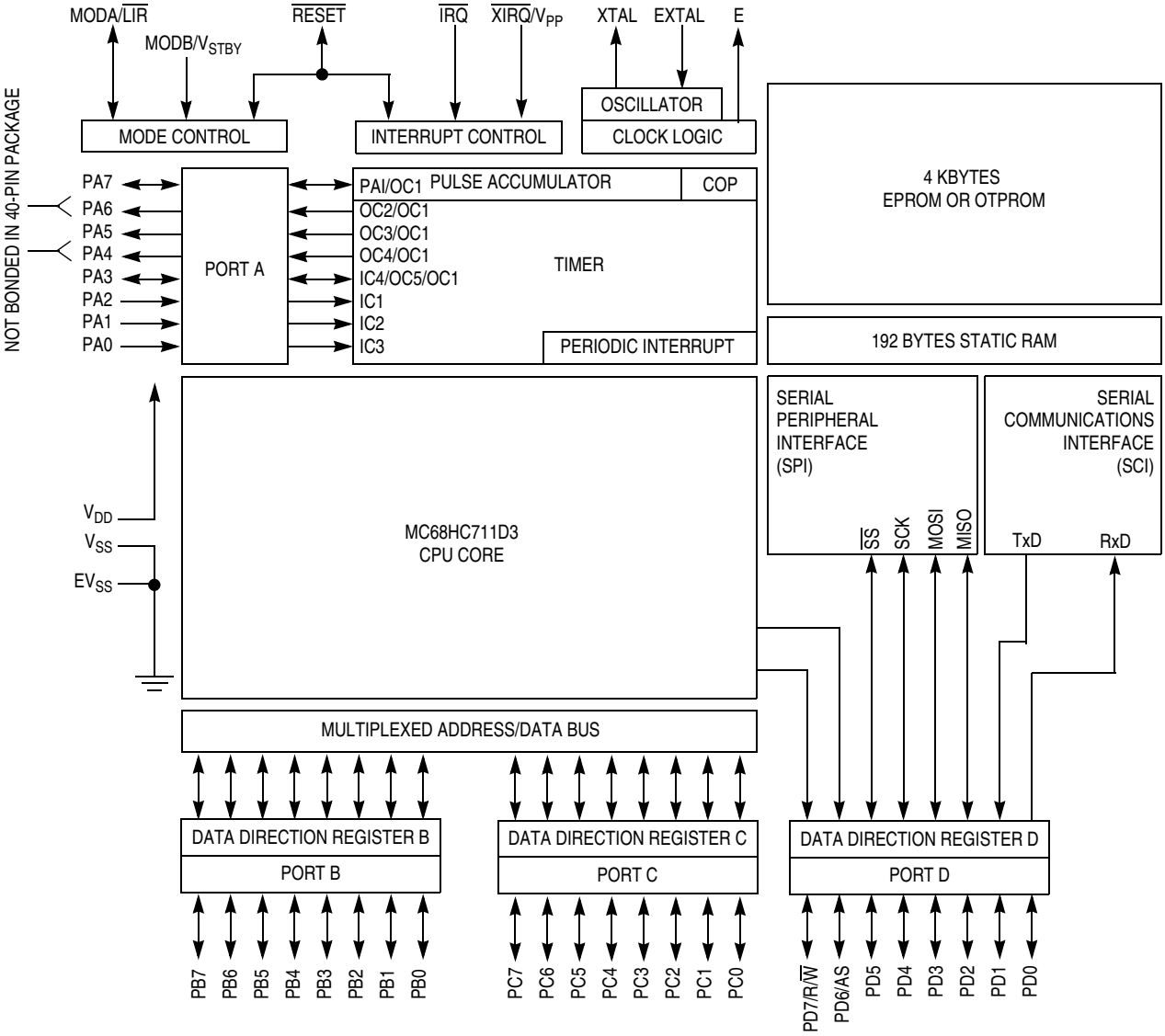


Figure 1-1. MC68HC711D3 Block Diagram

1.4 Pin Descriptions

Refer to Figure 1-2, Figure 1-3, and Figure 1-4 for pin assignments.

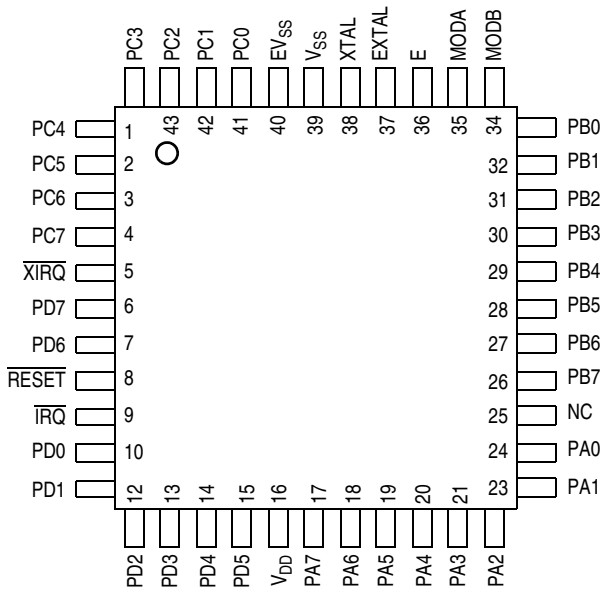


Figure 1-4. Pin Assignments for 44-Pin QFP

1.5 Power Supply (V_{DD}, V_{SS}, and EV_{SS})

Power is supplied to the MCU through V_{DD} and V_{SS}. V_{DD} is the power supply (+5 V ±10%) and V_{SS} is ground (0 V). EV_{SS}, available on the 44-pin PLCC and QFP, is an additional ground pin.

1.6 Reset ($\overline{\text{RESET}}$)

An active low bidirectional control signal, $\overline{\text{RESET}}$, acts as an input to initialize the MCU to a known startup state. It also acts as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or computer operating properly (COP) watchdog circuit. In addition, the state of this pin is one of the factors governing the selection of BOOT mode.

1.7 Crystal Driver and External Clock Input (XTAL and EXTAL)

These two pins provide the interface for either a crystal or a CMOS compatible clock to control the internal clock generator circuitry. The frequency applied to these pins is four times higher than the desired E-clock rate. Refer to Figure 1-5 for crystal and clock connections.

1.8 E-Clock Output (E)

E is the output connection for the internally generated E clock. The signal from E is used as a timing reference. The frequency of the E-clock output is one fourth that of the input frequency at the XTAL and EXTAL pins. The E clock can be turned off in single-chip mode for greater noise immunity if desired. See 4.3.6 Highest Priority I Interrupt and Miscellaneous Register (HPRIO) for details.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0026	Pulse Accumulator Control Register (PACTL) See pages 99 and 102.	Read: Write:	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
		Reset:	0	0	0	0	0	0	0	0
$0027	Pulse Accumulator Count Register (PACNT) See page 103.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Unaffected by reset							
$0028	SPI Control Register (SPCR) See page 81.	Read: Write:	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
		Reset:	0	0	0	0	0	1	U	U
$0029	SPI Status Register (SPSR) See page 82.	Read: Write:	SPIF	WCOL	0	MODF	0	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$002A	SPI Data I/O Register (SPDR) See page 83.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Unaffected by reset							
$002B	Baud Rate Register (BAUD) See page 72.	Read: Write:	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
		Reset:	0	0	0	0	0	U	U	U
$002C	SCI Control Register 1 (SCCR1) See page 70.	Read: Write:	R8	T8	0	M	WAKE	0	0	0
		Reset:	U	U	0	0	0	0	0	0
$002D	SCI Control Register 2 (SCCR2) See page 70.	Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Reset:	0	0	0	0	0	0	0	0
$002E	SCI Status Register (SCSR) See page 71.	Read: Write:	TDRE	TC	RDRF	IDLE	OR	NF	FE	0
		Reset:	1	1	0	0	0	0	0	0
$002F	SCI Data Register (SCDR) See page 69.	Read: Write:	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
		Reset:	Unaffected by reset							
$0030 ↓ $0038	Reserved		R	R	R	R	R	R	R	R
$0039	System Configuration Options Register (OPTION) See page 49.	Read: Write:	0	0	IRQE	DLY	CME	0	CR1	CR0
		Reset:	0	0	0	1	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Register and Control Bit Assignments (Sheet 4 of 5)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003A	Arm/Reset COP Timer Circuitry Register (COPRST) See page 48.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$003B	PROM Programming Control Register (PPROG) See page 32.	Read: Write:	MBE	0	ELAT	EXCOL	EXROW	0	0	PGM
		Reset:	0	0	0	0	0	0	0	0
$003C	Highest Priority I-Bit Interrupt and Miscellaneous Register (HPRIO) See page 58.	Read:	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0
		Write:								
		Reset:	Note 1				0	1	0	1
$003D	RAM and I/O Mapping Register (INIT) See page 29.	Read: Write:	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
		Reset:	0	0	0	0	0	0	0	1
$003E	Test 1 Register (TEST)	Read: Write:	TILOP	0	OCC4	CBYP	DISR	FCM	FCOP	0
		Reset:	0	0	0	0	0	0	0	0
$003F	System Configuration Register (CONFIG) See page 30.	Read: Write:	0	0	0	0	0	NOCOP	ROMON	0
		Reset:	0	0	0	0	0	U	U	0

1. The values of the RBOOT, SMOD, IRVNE, and MDA bits at reset depend on the mode during initialization. Refer to Table 4-3. Hardware Mode Select Summary.

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Register and Control Bit Assignments (Sheet 5 of 5)

2.3.2 RAM and I/O Mapping Register

The random-access memory (RAM) and input/output (I/O) mapping register (INIT) is a special-purpose 8-bit register that is used during initialization to change the default locations of RAM and control registers within the MCU memory map. It can be written to only once within the first 64 E-clock cycles after a reset in normal modes. Thereafter, it becomes a read-only register.

Address: $003D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
Reset:	0	0	0	0	0	0	0	0

Figure 2-3. RAM and I/O Mapping Register (INIT)

Table 3-2. Instruction Set (Sheet 4 of 8)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
COMA	Ones Complement A	$FF – A ⇒ A	A INH	43	—	2	—	—	—	—	Δ	Δ	0	1
COMB	Ones Complement B	$FF – B ⇒ B	B INH	53	—	2	—	—	—	—	Δ	Δ	0	1
CPD (opr)	Compare D to Memory 16-Bit	D – M : M + 1	IMM DIR EXT IND,X IND,Y	1A 83 1A 93 1A B3 1A A3 CD A3	jj kk dd hh ll ff ff	5 6 7 7 7	—	—	—	—	Δ	Δ	Δ	Δ
CPX (opr)	Compare X to Memory 16-Bit	IX – M : M + 1	IMM DIR EXT IND,X IND,Y	8C 9C BC AC CD AC	jj kk dd hh ll ff ff	4 5 6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
CPY (opr)	Compare Y to Memory 16-Bit	IY – M : M + 1	IMM DIR EXT IND,X IND,Y	18 8C 18 9C 18 BC 1A AC 18 AC	jj kk dd hh ll ff ff	5 6 7 7 7	—	—	—	—	Δ	Δ	Δ	Δ
DAA	Decimal Adjust A	Adjust Sum to BCD	INH	19	—	2	—	—	—	—	Δ	Δ	Δ	Δ
DEC (opr)	Decrement Memory Byte	M – 1 ⇒ M	EXT IND,X IND,Y	7A 6A 18 6A	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	—
DECA	Decrement Accumulator A	A – 1 ⇒ A	A INH	4A	—	2	—	—	—	—	Δ	Δ	Δ	—
DECB	Decrement Accumulator B	B – 1 ⇒ B	B INH	5A	—	2	—	—	—	—	Δ	Δ	Δ	—
DES	Decrement Stack Pointer	SP – 1 ⇒ SP	INH	34	—	3	—	—	—	—	—	—	—	—
DEX	Decrement Index Register X	IX – 1 ⇒ IX	INH	09	—	3	—	—	—	—	—	Δ	—	—
DEY	Decrement Index Register Y	IY – 1 ⇒ IY	INH	18 09	—	4	—	—	—	—	—	Δ	—	—
EORA (opr)	Exclusive OR A with Memory	A ⊕ M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	88 98 B8 A8 18 A8	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
EORB (opr)	Exclusive OR B with Memory	B ⊕ M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C8 D8 F8 E8 18 E8	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
FDIV	Fractional Divide 16 by 16	D / IX ⇒ IX; r ⇒ D	INH	03	—	41	—	—	—	—	—	Δ	Δ	Δ
IDIV	Integer Divide 16 by 16	D / IX ⇒ IX; r ⇒ D	INH	02	—	41	—	—	—	—	—	Δ	0	Δ
INC (opr)	Increment Memory Byte	M + 1 ⇒ M	EXT IND,X IND,Y	7C 6C 18 6C	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	—
INCA	Increment Accumulator A	A + 1 ⇒ A	A INH	4C	—	2	—	—	—	—	Δ	Δ	Δ	—
INCB	Increment Accumulator B	B + 1 ⇒ B	B INH	5C	—	2	—	—	—	—	Δ	Δ	Δ	—
INS	Increment Stack Pointer	SP + 1 ⇒ SP	INH	31	—	3	—	—	—	—	—	—	—	—

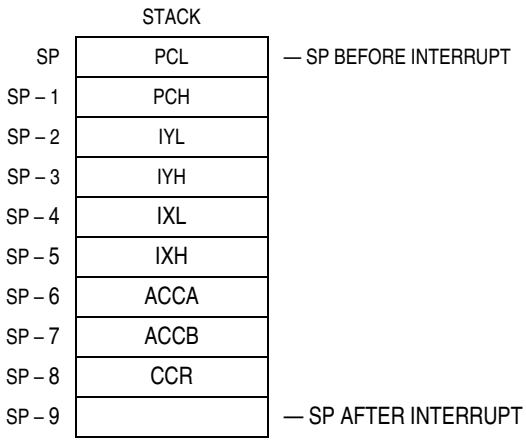


Figure 4-3. Interrupt Stacking Order

4.3.1 Software Interrupt (SWI)

The SWI is executed the same as any other instruction and takes precedence over interrupts only if the other interrupts are masked (with I and X bits in the CCR set). SWI execution is similar to that of the maskable interrupts in that it sets the I bit, stacks the central processor unit (CPU) registers, etc.

NOTE

The SWI instruction cannot be executed as long as another interrupt is pending. However, once the SWI instruction has begun, no other interrupt can be honored until the first instruction in the SWI service routine is completed.

4.3.2 Illegal Opcode Trap

Since not all possible opcodes or opcode sequences are defined, an illegal opcode detection circuit has been included in the MCU. When an illegal opcode is detected, an interrupt is required to the illegal opcode vector. The illegal opcode vector should never be left uninitialized.

4.3.3 Real-Time Interrupt (RTI)

The real-time interrupt (RTI) provides a programmable periodic interrupt. This interrupt is maskable by either the I bit in the CCR or the RTI enable (RTII) bit of the timer interrupt mask register 2 (TMSK2). The rate is based on the MCU E clock and is software selectable to the $E \div 2^{13}$, $E \div 2^{14}$, $E \div 2^{15}$, or $E \div 2^{16}$. See PACTL, TMSK2, and TFLG2 register descriptions in Chapter 8 Programmable Timer for control and status bit information.

4.3.4 Interrupt Mask Bits in the CCR

Upon reset, both the X bit and I bit of the CCR are set to inhibit all maskable interrupts and XIRQ. After minimum system initialization, software may clear the X bit by a TAP instruction, thus enabling XIRQ interrupts. Thereafter software cannot set the X bit. So, an XIRQ interrupt is effectively a non-maskable interrupt. Since the operation of the I bit related interrupt structure has no effect on the X bit, the internal $\overline{\text{XIRQ}}$ pin remains effectively non-masked. In the interrupt priority logic, the XIRQ interrupt is a higher priority than any source that is maskable by the I bit. All I bit related interrupts operate normally with their own priority relationship.

4.3.6 Highest Priority I Interrupt and Miscellaneous Register (HPRIO)

Four bits of this register (PSEL3–PSEL0) are used to select one of the I bit related interrupt sources and to elevate it to the highest I bit masked position of the priority resolution circuit. In addition, four miscellaneous system control bits are included in this register.

Address: $003C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0
Write:								
Reset:	Note 1				0	1	0	1

1. The values of the RBOOT, SMOD, IRVNE, and MDA bits at reset depend on the mode during initialization. Refer to Table 4-3.

Figure 4-7. Highest Priority I-Bit Interrupt and Miscellaneous Register (HPRIO)

RBOOT — Read Bootstrap ROM

This bit can be read at any time. It can be written only in special modes (SMOD = 1). In special bootstrap mode, it is set during reset. Reset clears it in all other modes.

1 = Bootloader ROM is enabled in the memory map at $BF00–$BFFF.
0 = Bootloader ROM is disabled and is not in the memory map.

SMOD and MDA — Special Mode Select and Mode Select A

These two bits can be read at any time.These bits reflect the status of the MODA and MODB input pins at the rising edge of reset. SMOD may be written only in special modes. It cannot be written to a 1 after being cleared without an interim reset. MDA may be written at any time in special modes, but only once in normal modes. An interpretation of the values of these two bits is shown in Table 4-3.

Table 4-3. Hardware Mode Select Summary

Inputs		Mode	Latched at Reset	
MODB	MODA		SMOD	MDA
1	0	Single chip	0	0
1	1	Expanded multiplexed	0	1
0	0	Special bootstrap	1	0
0	1	Special test	1	1

IRVNE — Internal Read Visibility/Not E

This bit may be read at any time. It may be written once in any mode. IRVNE is set during reset in special test mode only, and cleared by reset in the other modes.

1 = Data from internal reads is driven out on the external data bus in expanded modes.
0 = Data from internal reads is not visible on the external data bus.

As shown in the table, in single-chip and bootstrap modes IRVNE determines whether the E clock is driven out or forced low.

1 = E pin driven low
0 = E clock driven out of the chip

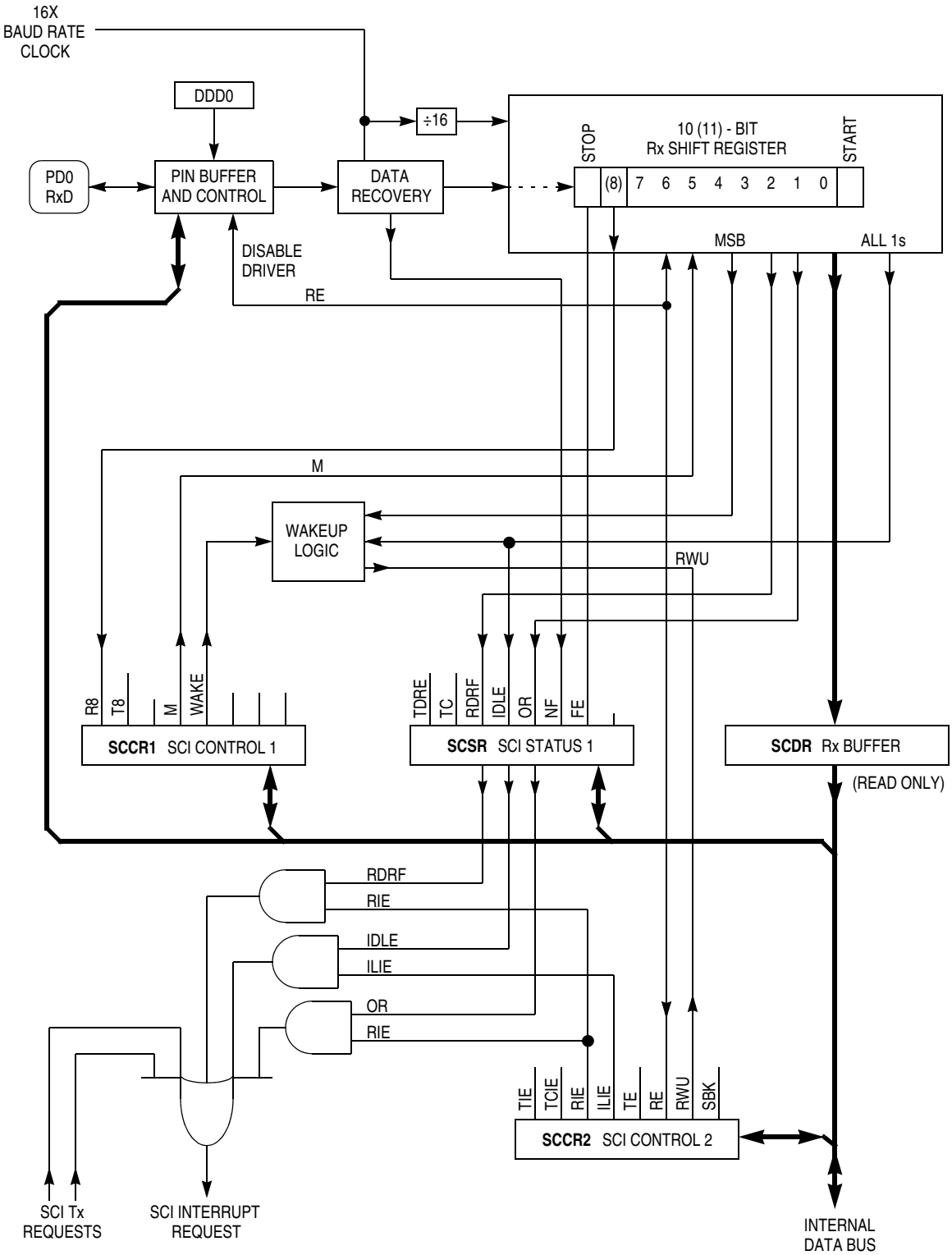


Figure 6-2. SCI Receiver Block Diagram

6.5 Wakeup Feature

The wakeup feature reduces SCI service overhead in multiple receiver systems. Software for each receiver evaluates the first character of each message. The receiver is placed in wakeup mode by writing a 1 to the RWU bit in the SCCR2 register. While RWU is 1, all of the receiver-related status flags (RDRF, IDLE, OR, NF, and FE) are inhibited (cannot become set). Although RWU can be cleared by a software write to SCCR2, to do so would be unusual. Normally, RWU is set by software and is cleared automatically with hardware. Whenever a new message begins, logic alerts the sleeping receivers to wake up and evaluate the initial character of the new message.

Two methods of wakeup are available:

- Idle line wakeup
- Address mark wakeup

During idle line wakeup, a sleeping receiver awakens as soon as the RxD line becomes idle. In the address mark wakeup, logic 1 in the most significant bit (MSB) of a character wakes up all sleeping receivers.

6.5.1 Idle-Line Wakeup

To use the receiver wakeup method, establish a software addressing scheme to allow the transmitting devices to direct a message to individual receivers or to groups of receivers. This addressing scheme can take any form as long as all transmitting and receiving devices are programmed to understand the same scheme. Because the addressing information is usually the first frame(s) in a message, receivers that are not part of the current task do not become burdened with the entire set of addressing frames. All receivers are awake (RWU = 0) when each message begins. As soon as a receiver determines that the message is not intended for it, software sets the RWU bit (RWU = 1), which inhibits further flag setting until the RxD line goes idle at the end of the message. As soon as an idle line is detected by receiver logic, hardware automatically clears the RWU bit so that the first frame of the next message can be received. This type of receiver wakeup requires a minimum of one idle-line frame time between messages and no idle time between frames in a message.

6.5.2 Address-Mark Wakeup

The serial characters in this type of wakeup consist of seven (eight if M = 1) information bits and an MSB, which indicates an address character (when set to 1 — mark). The first character of each message is an addressing character (MSB = 1). All receivers in the system evaluate this character to determine if the remainder of the message is directed toward this particular receiver. As soon as a receiver determines that a message is not intended for it, the receiver activates the RWU function by using a software write to set the RWU bit. Because setting RWU inhibits receiver-related flags, there is no further software overhead for the rest of this message. When the next message begins, its first character has its MSB set, which automatically clears the RWU bit and enables normal character reception. The first character whose MSB is set is also the first character to be received after wakeup because RWU gets cleared before the stop bit for that frame is serially received. This type of wakeup allows messages to include gaps of idle time, unlike the idle-line method, but there is a loss of efficiency because of the extra bit time for each character (address bit) required for all characters.

6.8 Status Flags and Interrupts

The SCI transmitter has two status flags. These status flags can be read by software (polled) to tell when the corresponding condition exists. Alternatively, a local interrupt enable bit can be set to enable each of these status conditions to generate interrupt requests when the corresponding condition is present. Status flags are automatically set by hardware logic conditions, but must be cleared by software, which provides an interlock mechanism that enables logic to know when software has noticed the status indication. The software clearing sequence for these flags is automatic — functions that are normally performed in response to the status flags also satisfy the conditions of the clearing sequence.

TDRE and TC flags are normally set when the transmitter is first enabled (TE set to 1). The TDRE flag indicates there is room in the transmit queue to store another data character in the TDR. The TIE bit is the local interrupt mask for TDRE. When TIE is 0, TDRE must be polled. When TIE and TDRE are 1, an interrupt is requested.

The TC flag indicates the transmitter has completed the queue. The TCIE bit is the local interrupt mask for TC. When TCIE is 0, TC must be polled; when TCIE is 1 and TC is 1, an interrupt is requested.

Writing a 0 to TE requests that the transmitter stop when it can. The transmitter completes any transmission in progress before actually shutting down. Only an MCU reset can cause the transmitter to stop and shut down immediately. If TE is written to 0 when the transmitter is already idle, the pin reverts to its general-purpose I/O function (synchronized to the bit-rate clock). If anything is being transmitted when TE is written to 0, that character is completed before the pin reverts to general-purpose I/O, but any other characters waiting in the transmit queue are lost. The TC and TDRE flags are set at the completion of this last character, even though TE has been disabled.

The SCI receiver has five status flags, three of which can generate interrupt requests. The status flags are set by the SCI logic in response to specific conditions in the receiver. These flags can be read (polled) at any time by software. Refer to Figure 6-9, which shows SCI interrupt arbitration.

When an overrun takes place, the new character is lost, and the character that was in its way in the parallel RDR is undisturbed. RDRF is set when a character has been received and transferred into the parallel RDR. The OR flag is set instead of RDRF if overrun occurs. A new character is ready to be transferred into RDR before a previous character is read from RDR.

The NF and FE flags provide additional information about the character in the RDR, but do not generate interrupt requests.

The last receiver status flag and interrupt source come from the IDLE flag. The RxD line is idle if it has constantly been at logic 1 for a full character time. The IDLE flag is set only after the RxD line has been busy and becomes idle, which prevents repeated interrupts for the whole time RxD remains idle.

Address:	$0011 — TIC1 (Low)							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Unaffected by reset							
Address:	$0012 — TIC2 (High)							
	Bit 15	14	13	12	11	10	9	Bit 8
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	Unaffected by reset							
Address:	$0013 — TIC2 (Low)							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Unaffected by reset							
Address:	$0014 — TIC3 (High)							
	Bit 15	14	13	12	11	10	9	Bit 8
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	Unaffected by reset							
Address:	$0015 — TIC3 (Low)							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Unaffected by reset							

= Unimplemented

Figure 8-4. Timer Input Capture Registers (TICx) (Continued)

8.3.3 Timer Input Capture 4/Output Compare 5 Register

Use timer input capture 4/output compare 5 (TI4/O5) as either an input capture register or an output compare register, depending on the function chosen for the I4/O5 pin. To enable it as an input capture pin, set the I4/O5 bit in the pulse accumulator control register (PACTL) to logic level 1. To use it as an output compare register, set the I4/O5 bit to a logic level 0. Refer to 8.7 Pulse Accumulator.

Address:	$001E — TI4/O5 (High)							
	Bit 15	14	13	12	11	10	9	Bit 8
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	1	1	1	1	1	1	1	1
Address:	$001F — TI4/O5 (Low)							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	1	1	1	1	1	1	1	1

= Unimplemented

Figure 8-5. Timer Input Capture 4/Output Compare 5 Register (TI4/O5)

8.7.1 Pulse Accumulator Control Register

Four of the pulse accumulator control register (PACTL) bits control an 8-bit pulse accumulator system. Another bit enables either the OC5 function or the IC4 function, while two other bits select the rate for the real-time interrupt system.

Address: $0026

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
Reset:	0	0	0	0	0	0	0	0

Figure 8-20. Pulse Accumulator Control Register (PACTL)

DDRA7 — Data Direction Control for Port A Bit 7

The pulse accumulator uses port A bit 7 as the PAI input, but the pin can also be used as general-purpose I/O or as an output compare.

NOTE

Even when port A bit 7 is configured as an output, the pin still drives the input to the pulse accumulator.

Refer to Chapter 5 Input/Output (I/O) Ports for more information.

PAEN — Pulse Accumulator System Enable Bit

0 = Pulse accumulator disabled
1 = Pulse accumulator enabled

PAMOD — Pulse Accumulator Mode Bit

0 = Event counter
1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control Bit

This bit has different meanings depending on the state of the PAMOD bit, as shown in Table 8-8.

Table 8-8. Pulse Accumulator Edge Control

PAMOD	PEDGE	Action on Clock
0	0	PAI falling edge increments the counter.
0	1	PAI rising edge increments the counter.
1	0	A 0 on PAI inhibits counting.
1	1	A 1 on PAI inhibits counting.

DDRA3 — Data Direction Register for Port A Bit 3

Refer to Chapter 5 Input/Output (I/O) Ports.

I4/O5 — Input Capture 4/Output Compare 5 Bit

Refer to 8.3 Input Capture.

RTR1 and RTR0 — RTI Interrupt Rate Select Bits

Refer to 8.5 Real-Time Interrupt.

8.7.2 Pulse Accumulator Count Register

The 8-bit read/write pulse accumulator count register (PACNT) contains the count of external input events at the PAI input or the accumulated count. The counter is not affected by reset and can be read or written at any time. Counting is synchronized to the internal PH2 clock so that incrementing and reading occur during opposite half cycles.

Address: $0027

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	Unaffected by reset							

Figure 8-21. Pulse Accumulator Count Register (PACNT)

8.7.3 Pulse Accumulator Status and Interrupt Bits

The pulse accumulator control bits, PAOVI and PAII, PAOVF, and PAIF are located within timer registers TMSK2 and TFLG2.

PAOVI and PAOVF — Pulse Accumulator Interrupt Enable and Overflow Flag

The PAOVF status bit is set each time the pulse accumulator count rolls over from $FF to $00. To clear this status bit, write a 1 in the corresponding data bit position (bit 5) of the TFLG2 register. The PAOVI control bit allows configuring the pulse accumulator overflow for polled or interrupt-driven operation and does not affect the state of PAOVF. When PAOVI is 0, pulse accumulator overflow interrupts are inhibited, and the system operates in a polled mode, which requires PAOVF to be polled by user software to determine when an overflow has occurred. When the PAOVI control bit is set, a hardware interrupt request is generated each time PAOVF is set. Before leaving the interrupt service routine, software must clear PAOVF by writing to the TFLG2 register.

PAII and PAIF — Pulse Accumulator Input Edge Interrupt Enable and Flag

The PAIF status bit is automatically set each time a selected edge is detected at the PA7/PAI/OC1 pin. To clear this status bit, write to the TFLG2 register with a 1 in the corresponding data bit position (bit 4). The PAII control bit allows configuring the pulse accumulator input edge detect for polled or interrupt-driven operation but does not affect setting or clearing the PAIF bit. When PAII is 0, pulse accumulator input interrupts are inhibited, and the system operates in a polled mode. In this mode, the PAIF bit must be polled by user software to determine when an edge has occurred. When the PAII control bit is set, a hardware interrupt request is generated each time PAIF is set. Before leaving the interrupt service routine, software must clear PAIF by writing to the TFLG register.

Address: $0024

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
Reset:	0	0	0	0	0	0	0	0

Figure 8-22. Timer Interrupt Mask 2 Register (TMSK2)

Address: $0025

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOF	RTIF	PAOVF	PAIF	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 8-23. Timer Interrupt Flag 2 Register (TFLG2)

9.5 DC Electrical Characteristics

Characteristic[1]		Symbol	Min	Max	Unit
Output voltage[2] I_{Load} = ± 10.0 µA	All outputs All outputs except $\overline{RESET}$ and MODA	V_{OL} V_{OH}	— V_{DD} – 0.1	0.1 —	V
Output high voltage[1] I_{Load} = – 0.8 mA, V_{DD} = 4.5 V	All outputs except $\overline{RESET}$, EXTAL, and MODA	V_{OH}	V_{DD} – 0.8	—	V
Output low voltage I_{Load} = 1.6 mA	All outputs except XTAL	V_{OL}	—	0.4	V
Input high voltage	All inputs except $\overline{RESET}$ $\overline{RESET}$	V_{IH}	0.7 x V_{DD} 0.8 x V_{DD}	V_{DD} + 0.3 V_{DD} + 0.3	V
Input low voltage	All inputs	V_{IL}	V_{SS} – 0.3	0.2 x V_{DD}	V
I/O ports, three-state leakage PA7, PA3, PC7–PC0, PD7–PD0, V_{In} = V_{IH} or V_{IL}	MODA/$\overline{LIR}$, $\overline{RESET}$	I_{OZ}	—	±10	µA
Input leakage current V_{In} = V_{DD} or V_{SS} V_{In} = V_{DD} or V_{SS}	$\overline{IRQ}$, $\overline{XIRQ}$ MODB/V_{STBY}	I_{In}	— —	±1 ±10	µA
RAM standby voltage	Power down	V_{SB}	4.0	V_{DD}	V
RAM standby current	Power down	I_{SB}	—	20	µA
Total supply current[3] RUN: Single-chip mode dc — 2 MHz 3 MHz Expanded multiplexed mode dc — 2 MHz 3 MHz		I_{DD}	 — — — —	 15 27 27 35	mA
WAIT — All peripheral functions shut down: Single-chip mode dc — 2 MHz 3 MHz Expanded multiplexed mode dc — 2 MHz 3 MHz		W_{IDD}	 — — — —	 6 15 10 20	mA
STOP — No clocks, single-chip mode: dc — 2 MHz 3 MHz		S_{IDD}	 — —	 100 150	µA
Input capacitance PA3–PA0, IRQ, XIRQ, EXTAL PA7, PC7–PC0, PD7–PD0, MODA/$\overline{LIR}$, $\overline{RESET}$		C_{In}	— —	8 12	pF
Power dissipation Single-chip mode dc — 2 MHz 3 MHz Expanded multiplexed mode dc — 2 MHz 3 MHz		P_D	 — — — —	 85 150 150 195	mW
EPROM programming voltage		V_{PP}	11.75	12.75	V
EPROM programming time		t_{PP}	2	4	ms

1. V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted.
2. V_{OH} specification for $\overline{RESET}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification is not applicable to ports C and D in wired-OR mode.
3. All ports configured as inputs: $V_{IL} \leq 0.2$ V, $V_{IH} \leq V_{DD} - 0.2$ V; no dc loads; EXTAL is driven with a square wave; t_{cyc} = 476.5 ns.

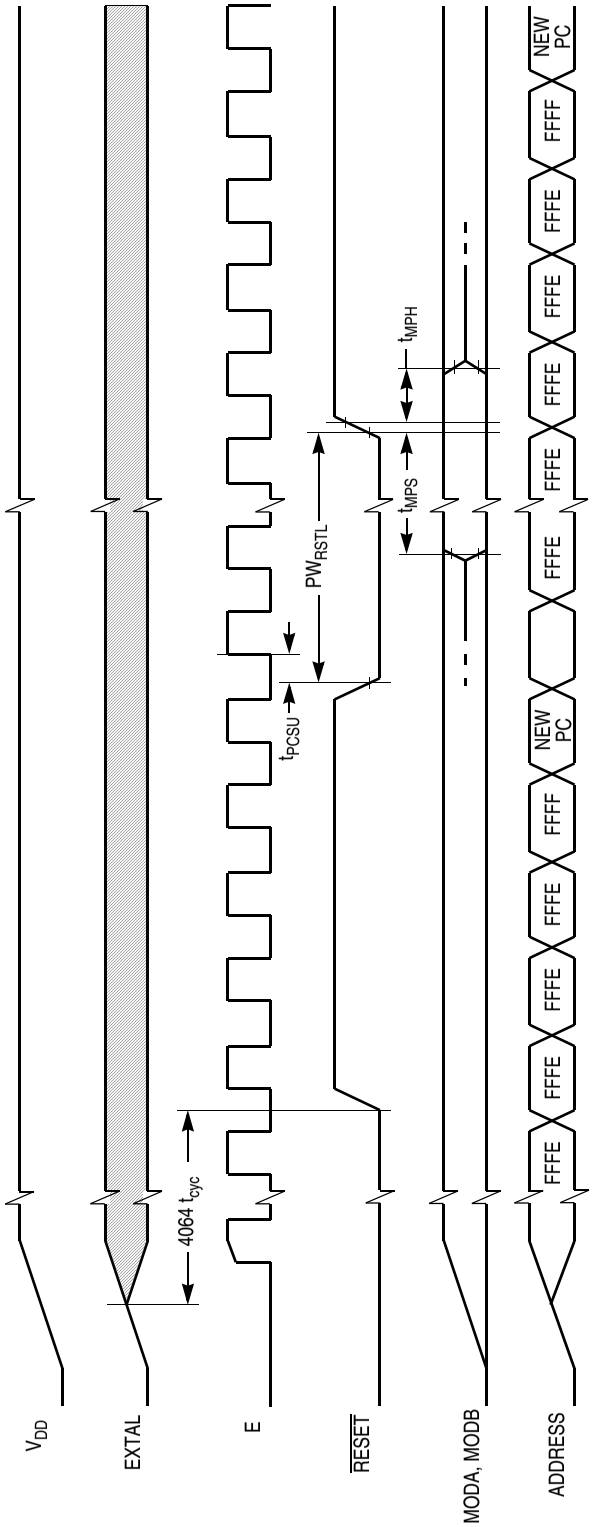
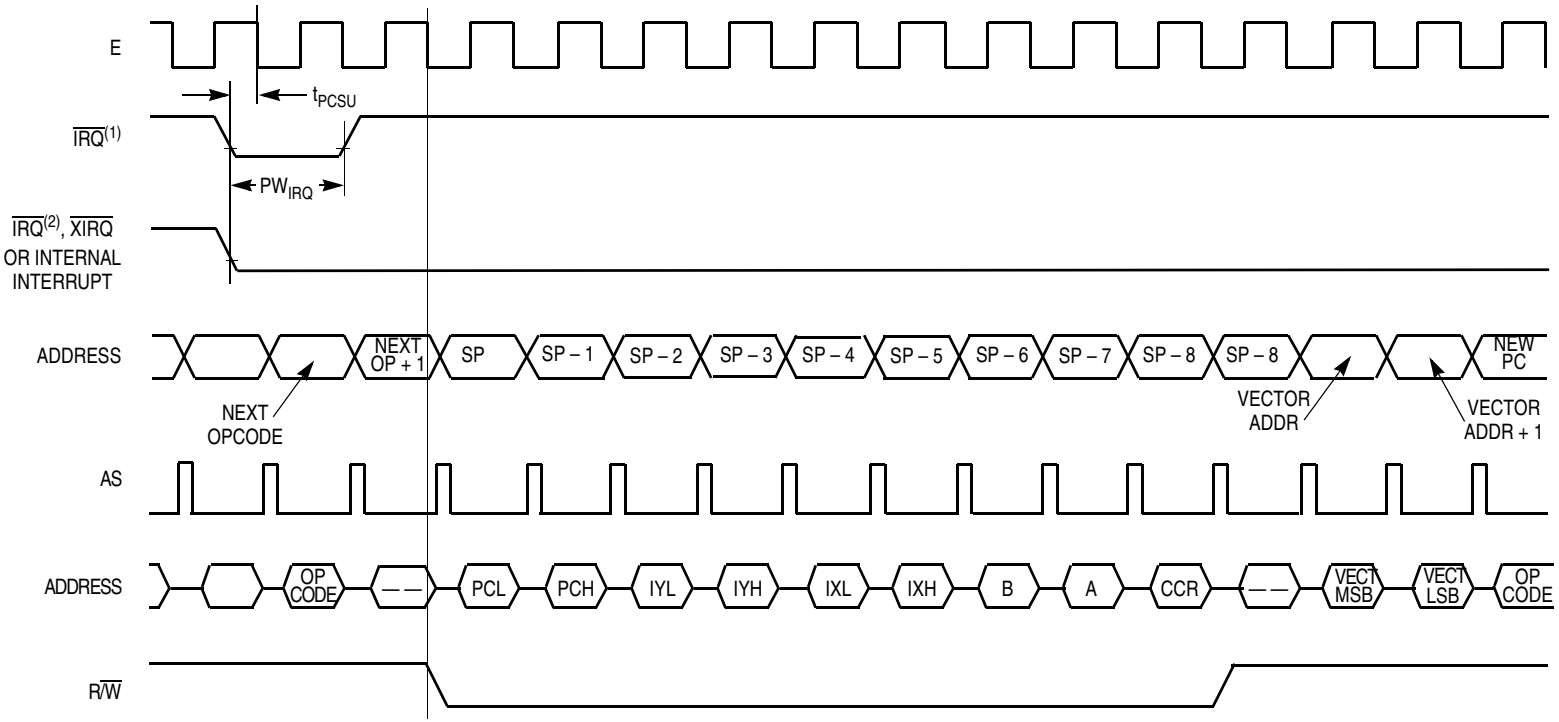
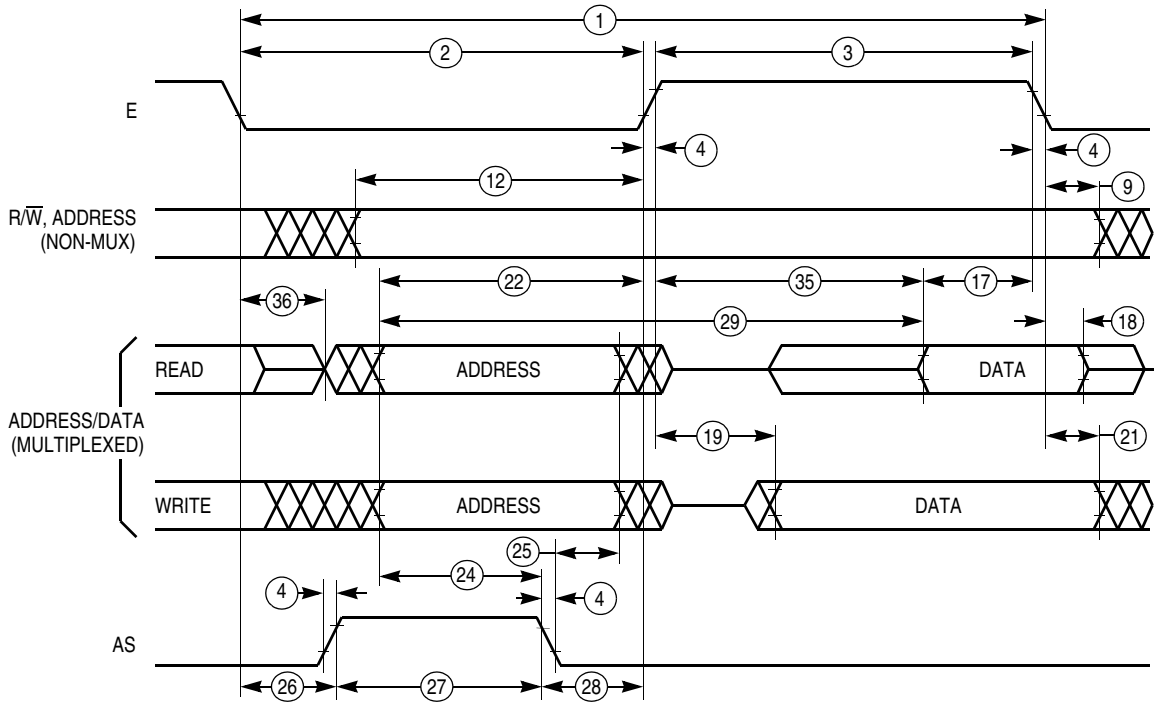


Figure 9-4. POR and External Reset Timing Diagram



Notes:
1. Edge sensitive $\overline{IRQ}$ pin (IRQE bit = 1)
2. Level sensitive $\overline{IRQ}$ pin (IRQE bit = 0)

Figure 9-7. Interrupt Timing Diagram



Note: Measurement points shown are 20% and 70% of V_{DD}.

Figure 9-10. Multiplexed Expansion Bus Timing Diagram

A.4 Memory Map

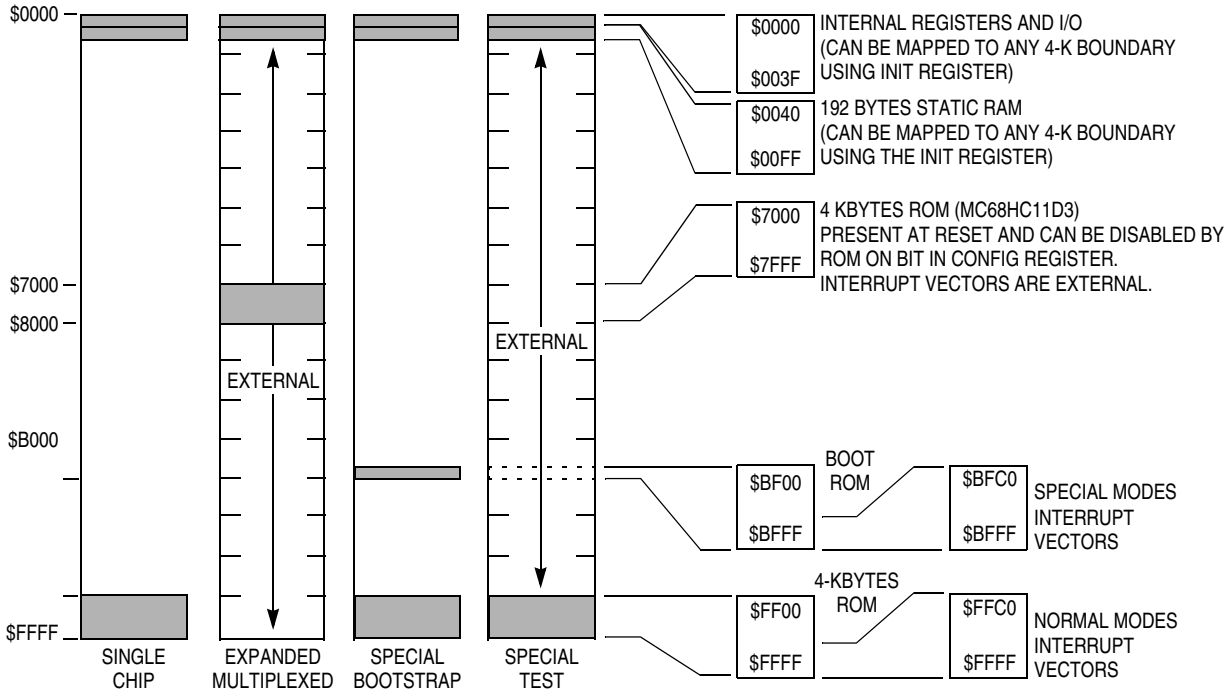


Figure A-4. MC68HC11Dx(1) Memory Map

A.5 MC68HC11D3 and MC68HC11D0 Electrical Characteristics

The parameters given in Chapter 9 Electrical Characteristics apply to the MC68HC11D3 and MC68HC11D0 with the exceptions given here.

A.5.1 Functional Operating Temperature Range

Rating	Symbol	Value	Unit
Operating temperature range MC68HC11D0C	T_A	T_L to T_H –40 to +85	°C

A.5.2 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Package thermal resistance (junction-to-ambient) 44-pin plastic leaded chip carrier (PLCC) 44-pin plastic quad flat pack (QFP	Θ_{JA}	 50 85	°C/W

1. MC68HC11D0 only operates in expanded multiplexed mode and bootstrap mode.

B.2.3 Control Timing

Characteristic[1]	Symbol	1.0 MHz		2.0 MHz		Unit
		Min	Max	Min	Max	
Frequency of operation	f_O	dc	1.0	dc	2.0	MHz
E-clock period	t_{cyc}	1000	—	500	—	ns
Crystal frequency	f_{XTAL}	—	4.0	—	8.0	MHz
External oscillator frequency	4 f_O	dc	4.0	dc	8.0	MHz
Processor control setup time t_{PCSU} = 1/4 t_{cyc} + 50 ns	t_{PCSU}	325	—	200	—	ns
Reset input pulse width[2] To guarantee external reset vector Minimum input time can be preempted by internal reset	PW_{RSTL}	8 1	— —	8 1	— —	t_{cyc}
Interrupt pulse width, PW_{IRQ} = t_{cyc} + 20 ns $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	1020	—	520	—	ns
Wait recovery startup time	t_{WRS}	—	4	—	4	t_{cyc}
Timer pulse width PW_{TIM} = t_{cyc} + 20 ns Input capture pulse accumulator input	PW_{TIM}	1020	—	520	—	ns

1. V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Reset is recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt. Refer to Chapter 4 Resets, Interrupts, and Low-Power Modes for further details.

B.2.4 Peripheral Port Timing

Characteristic[1]	Symbol	1.0 MHz		2.0 MHz		Unit
		Min	Max	Min	Max	
Frequency of operation (E-clock frequency)	f_O	dc	1.0	dc	2.0	MHz
E-clock period	t_{cyc}	1000	—	500	—	ns
Peripheral data setup time[2] MCU read of ports A, B, C, and D	t_{PDSU}	100	—	100	—	ns
Peripheral data hold time[2] MCU read of ports A, B, C, and D	t_{PDH}	50	—	50	—	ns
Delay time, peripheral data write MCU write to port A MCU writes to ports B, C, and D t_{PWD} = 1/4 t_{cyc} + 150 ns	t_{PWD}	— —	200 350	— —	200 225	ns

1. V_{DD} = 3.0 Vd to 5.5 Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Port C and D timing is valid for active drive (CWOM and DWOM bits not set in PIOC and SPCR registers respectively).