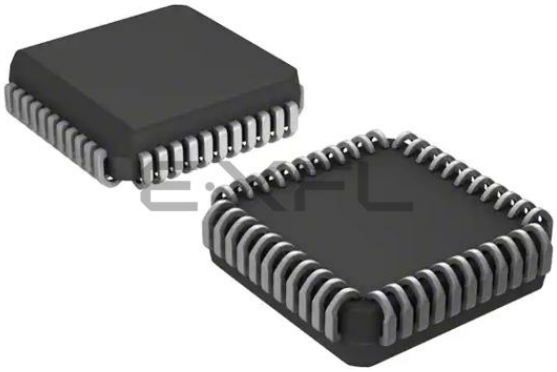

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Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	3MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	26
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc711d3cfne3

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Appendix A
MC68HC11D3 and MC68HC11D0

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MC68L11D0

2.4.2 Programming the EPROM with Downloaded Data

When using this method, the EPROM is programmed by software while in the special test or bootstrap modes. User-developed software can be uploaded through the SCI or a ROM-resident EPROM programming utility can be used. The 12-volt nominal programming voltage must be present on the $\overline{\text{XIRQ}}/V_{PP}$ pin. To use the resident utility, bootload a 3-byte program consisting of a single jump instruction to $BF00. $BF00 is the starting address of a resident EPROM programming utility. The utility program sets the X and Y index registers to default values, then receives programming data from an external host, and puts it in EPROM. The value in IX determines programming delay time. The value in IY is a pointer to the first address in EPROM to be programmed (default = $F000).

When the utility program is ready to receive programming data, it sends the host the $FF character. Then it waits. When the host sees the $FF character, the EPROM programming data is sent, starting with the first location in the EPROM array. After the last byte to be programmed is sent and the corresponding verification data is returned, the programming operation is terminated by resetting the MCU.

2.4.3 PROM Programming Control Register

The PROM programming control register (PPROG) is used to control the programming of the OTPROM or EPROM. PPROG is cleared on reset so that the PROM is configured for normal read.

Address: $003B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	MBE	0	ELAT	EXCOL	EXROW	0	0	PGM
Reset:	0	0	0	0	0	0	0	0

Figure 2-5. PROM Programming Control Register (PPROG)

MBE — Multiple Byte Program Enable Bit
This bit is reserved for testing.

Bit 6, 2, and 1 — Not implemented
Always read 0.

ELAT — EPROM (OTPROM) Latch Control Bit
1 = PROM address and data bus are configured for programming. Writes to PROM cause address and data to be latched. The PROM cannot be read.
0 = PROM address and data bus are configured for normal reads. PROM cannot be programmed.

EXCOL — Select Extra Columns Bit
This bit is reserved for testing.

EXROW — Select Extra Row Bit
This bit is reserved for testing.

PGM — EPROM (OTPROM) Program Command Bit
This bit may be written only when ELAT = 1.
1 = Programming power is switched on to PROM array.
0 = Programming power is switched off.

3.5.3 Extended

In the extended addressing mode, the effective address of the argument is contained in two bytes following the opcode byte. These are 3-byte instructions (or 4-byte instructions if a prebyte is required). One or two bytes are needed for the opcode and two for the effective address.

3.5.4 Indexed

In the indexed addressing mode, an 8-bit unsigned offset contained in the instruction is added to the value contained in an index register (IX or IY). The sum is the effective address. This addressing mode allows referencing any memory location in the 64-Kbyte address space. These are 2- to 5-byte instructions, depending on whether a prebyte is required.

3.5.5 Inherent

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations that use only the index registers or accumulators, as well as control instructions with no arguments, are included in this addressing mode. These are 1- or 2-byte instructions.

3.5.6 Relative

The relative addressing mode is used only for branch instructions. If the branch condition is true, an 8-bit signed offset included in the instruction is added to the contents of the program counter to form the effective branch address. Otherwise, control proceeds to the next instruction. These are usually 2-byte instructions.

3.6 Instruction Set

Refer to Table 3-2, which shows all the M68HC11 instructions in all possible addressing modes. For each instruction, the table shows the operand construction, the number of machine code bytes, and execution time in CPU E-clock cycles.

Table 3-2. Instruction Set (Sheet 1 of 8)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
ABA	Add Accumulators	A + B ⇒ A	INH	1B	—	2	—	—	Δ	—	Δ	Δ	Δ	Δ
ABX	Add B to X	IX + (00 : B) ⇒ IX	INH	3A	—	3	—	—	—	—	—	—	—	—
ABY	Add B to Y	IY + (00 : B) ⇒ IY	INH	18 3A	—	4	—	—	—	—	—	—	—	—
ADCA (opr)	Add with Carry to A	A + M + C ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	89 99 B9 A9 18 A9	ii dd hh ll ff ff	2 3 4 4 5	—	—	Δ	—	Δ	Δ	Δ	Δ
ADCB (opr)	Add with Carry to B	B + M + C ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C9 D9 F9 E9 18 E9	ii dd hh ll ff ff	2 3 4 4 5	—	—	Δ	—	Δ	Δ	Δ	Δ
ADDA (opr)	Add Memory to A	A + M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	8B 9B BB AB 18 AB	ii dd hh ll ff ff	2 3 4 4 5	—	—	Δ	—	Δ	Δ	Δ	Δ

Chapter 4
Resets, Interrupts, and Low-Power Modes

4.1 Introduction

This section describes the internal and external resets and interrupts of the MC68HC711D3 and its two low power-consumption modes.

4.2 Resets

The microcontroller unit (MCU) can be reset in any of these four ways:

1. An active-low input to the $\overline{\text{RESET}}$ pin
2. A power-on reset (POR) function
3. A clock monitor failure
4. A computer operating properly (COP) watchdog timer timeout

The $\overline{\text{RESET}}$ input consists mainly of a Schmitt trigger that senses the $\overline{\text{RESET}}$ line logic level.

4.2.1 $\overline{\text{RESET}}$ Pin

To request an external reset, the $\overline{\text{RESET}}$ pin must be held low for at least eight E-clock cycles, or for one E-clock cycle if no distinction is needed between internal and external resets.

4.2.2 Power-On Reset (POR)

Power-on reset occurs when a positive transition is detected on V_{DD}. This reset is used strictly for power turn on conditions and should not be used to detect any drop in the power supply voltage. If the external $\overline{\text{RESET}}$ pin is low at the end of the power-on delay time, the processor remains in the reset condition until $\overline{\text{RESET}}$ goes high.

4.2.3 Computer Operating Properly (COP) Reset

The MCU contains a watchdog timer that automatically times out unless it is serviced within a specific time by a program reset sequence. If the COP watchdog timer is allowed to timeout, a reset is generated, which drives the $\overline{\text{RESET}}$ pin low to reset the MCU and the external system.

In the MC68HC711D3, the COP reset function is enabled out of reset in normal modes. If the user does not want the COP enabled, he must write a 1 to the NOCOP bit of the configuration control register (CONFIG) after reset. This bit is writable only once after reset in normal modes (see 2.3.3 Configuration Control Register for more information). Protected control bits (CR1 and CR0) in the configuration options register (OPTION) allow the user to select one of the four COP timeout rates. Table 4-1 shows the relationship between CR1 and CR0 and the COP timeout period for various system clock frequencies.

Address:	$0039							
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	0	IRQE	DLY	CME	0	CR1	CR0
Reset:	0	0	0	1	0	0	0	0

Figure 4-2. System Configuration Options Register (OPTION)

Bits 7, 6, and 2 — Not implemented

Always read 0.

IRQE — $\overline{\text{IRQ}}$ Edge/Level Sensitivity Select

This bit can be written only once during the first 64 E-clock cycles after reset in normal modes.

1 = $\overline{\text{IRQ}}$ is configured to respond only to falling edges.

0 = $\overline{\text{IRQ}}$ is configured for low-level wired-OR operation.

DLY — Stop Mode Exit Turnon Delay

This bit is set during reset and can be written only once during the first 64 E-clock cycles after reset in normal modes. If an external clock source rather than a crystal is used, the stabilization delay can be inhibited because the clock source is assumed to be stable.

1 = A stabilization delay of 4064 E-clock cycles is imposed before processing resumes after a stop mode wakeup.

0 = No stabilization delay is imposed after story recovery.

CME — Clock Monitor Enable

1 = Clock monitor circuit is enabled.

0 = Clock monitor circuit is disabled.

CR1 and CR0 — COP Timer Rate Selects

The COP system is driven by a constant frequency of $E \div 2^{15}$. These two bits specify an additional divide-by value to arrive at the COP timeout rate. These bits are cleared during reset and can be written only once during the first 64 E-clock cycles after reset in normal modes. The value of these bits is:

CR1	CR0	$E \div 2^{15}$ Divided By
0	0	1
0	1	4
1	0	16
1	1	64

4.3 Interrupts

Excluding reset-type interrupts, there are 17 hardware interrupts and one software interrupt that can be generated from all the possible sources. These interrupts can be divided into two categories: maskable and non-maskable. Fifteen of the interrupts can be masked using the I bit of the condition code register (CCR). All the on-chip (hardware) interrupts are individually maskable by local control bits. The software interrupt is non-maskable. The external input to the $\overline{\text{XIRQ}}$ pin is considered a non-maskable interrupt because it cannot be masked by software once it is enabled. However, it is masked during reset and upon receipt of an interrupt at the $\overline{\text{XIRQ}}$ pin. Illegal opcode is also a non-maskable interrupt.

6.5 Wakeup Feature

The wakeup feature reduces SCI service overhead in multiple receiver systems. Software for each receiver evaluates the first character of each message. The receiver is placed in wakeup mode by writing a 1 to the RWU bit in the SCCR2 register. While RWU is 1, all of the receiver-related status flags (RDRF, IDLE, OR, NF, and FE) are inhibited (cannot become set). Although RWU can be cleared by a software write to SCCR2, to do so would be unusual. Normally, RWU is set by software and is cleared automatically with hardware. Whenever a new message begins, logic alerts the sleeping receivers to wake up and evaluate the initial character of the new message.

Two methods of wakeup are available:

- Idle line wakeup
- Address mark wakeup

During idle line wakeup, a sleeping receiver awakens as soon as the RxD line becomes idle. In the address mark wakeup, logic 1 in the most significant bit (MSB) of a character wakes up all sleeping receivers.

6.5.1 Idle-Line Wakeup

To use the receiver wakeup method, establish a software addressing scheme to allow the transmitting devices to direct a message to individual receivers or to groups of receivers. This addressing scheme can take any form as long as all transmitting and receiving devices are programmed to understand the same scheme. Because the addressing information is usually the first frame(s) in a message, receivers that are not part of the current task do not become burdened with the entire set of addressing frames. All receivers are awake (RWU = 0) when each message begins. As soon as a receiver determines that the message is not intended for it, software sets the RWU bit (RWU = 1), which inhibits further flag setting until the RxD line goes idle at the end of the message. As soon as an idle line is detected by receiver logic, hardware automatically clears the RWU bit so that the first frame of the next message can be received. This type of receiver wakeup requires a minimum of one idle-line frame time between messages and no idle time between frames in a message.

6.5.2 Address-Mark Wakeup

The serial characters in this type of wakeup consist of seven (eight if M = 1) information bits and an MSB, which indicates an address character (when set to 1 — mark). The first character of each message is an addressing character (MSB = 1). All receivers in the system evaluate this character to determine if the remainder of the message is directed toward this particular receiver. As soon as a receiver determines that a message is not intended for it, the receiver activates the RWU function by using a software write to set the RWU bit. Because setting RWU inhibits receiver-related flags, there is no further software overhead for the rest of this message. When the next message begins, its first character has its MSB set, which automatically clears the RWU bit and enables normal character reception. The first character whose MSB is set is also the first character to be received after wakeup because RWU gets cleared before the stop bit for that frame is serially received. This type of wakeup allows messages to include gaps of idle time, unlike the idle-line method, but there is a loss of efficiency because of the extra bit time for each character (address bit) required for all characters.

IDLE — Idle Line Detected Flag

This flag is set if the RxD line is idle. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again. The IDLE flag is inhibited when RWU = 1. Clear IDLE by reading SCSR with IDLE set and then reading SCDR.

0 = RxD line active
1 = RxD line idle

OR — Overrun Error Flag

OR is set if a new character is received before a previously received character is read from SCDR. Clear the OR flag by reading SCSR with OR set and then reading SCDR.

0 = No overrun
1 = Overrun detected

NF — Noise Error Flag

NF is set if majority sample logic detects anything other than a unanimous decision. Clear NF by reading SCSR with NF set and then reading SCDR.

0 = Unanimous decision
1 = Noise detected

FE — Framing Error Bit

FE is set when a 0 is detected where a stop bit was expected. Clear the FE flag by reading SCSR with FE set and then reading SCDR.

0 = Stop bit detected
1 = Zero detected

6.7.5 Baud Rate Register

The baud rate register (BAUD) is used to select different baud rates for the SCI system. The SCP1 and SCP0 bits function as a prescaler for the SCR2–SCR0 bits. Together, these five bits provide multiple baud rate combinations for a given crystal frequency. Normally, this register is written once during initialization. The prescaler is set to its fastest rate by default out of reset and can be changed at any time. Refer to Table 6-1 and Table 6-2 for normal baud rate selections.

Address: $002B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
Reset:	0	0	0	0	0	U	U	U

U = Unaffected

Figure 6-7. Baud Rate Register (BAUD)

TCLR — Clear Baud Rate Counters (Test)

RCKB — SCI Baud Rate Clock Check (Test)

Chapter 7
Serial Peripheral Interface (SPI)

7.1 Introduction

The serial peripheral interface (SPI), an independent serial communications subsystem, allows the microcontroller unit (MCU) to communicate synchronously with peripheral devices, such as:

- Transistor-transistor logic (TTL) shift registers
- Liquid crystal diode (LCD) display drivers
- Analog-to-digital converter (ADC) subsystems
- Other microprocessors (MCUs)

The SPI is also capable of inter-processor communication in a multiple master system. The SPI system can be configured as either a master or a slave device with data rates as high as one half of the E-clock rate when configured as master, and as fast as the E-clock rate when configured as slave.

7.2 Functional Description

The central element in the SPI system is the block containing the shift register and the read data buffer. The system is single buffered in the transmit direction and double buffered in the receive direction. This means that new data for transmission cannot be written to the shifter until the previous transfer is complete; however, received data is transferred into a parallel read data buffer so the shifter is free to accept a second serial character. As long as the first character is read out of the read data buffer before the next serial character is ready to be transferred, no overrun condition occurs. A single MCU register address is used for reading data from the read data buffer, and for writing data to the shifter.

The SPI status block represents the SPI status functions (transfer complete, write collision, and mode fault) performed by the serial peripheral status register (SPSR). The SPI control block represents those functions that control the SPI system through the serial peripheral control register (SPCR).

Refer to Figure 7-1, which shows the SPI block diagram.

7.3 SPI Transfer Formats

During an SPI transfer, data is simultaneously transmitted and received. A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slave SPI device; slave devices that are not selected do not interfere with SPI bus activities. On a master SPI device, the select line can optionally be used to indicate a multiple master bus contention. Refer to Figure 7-2.

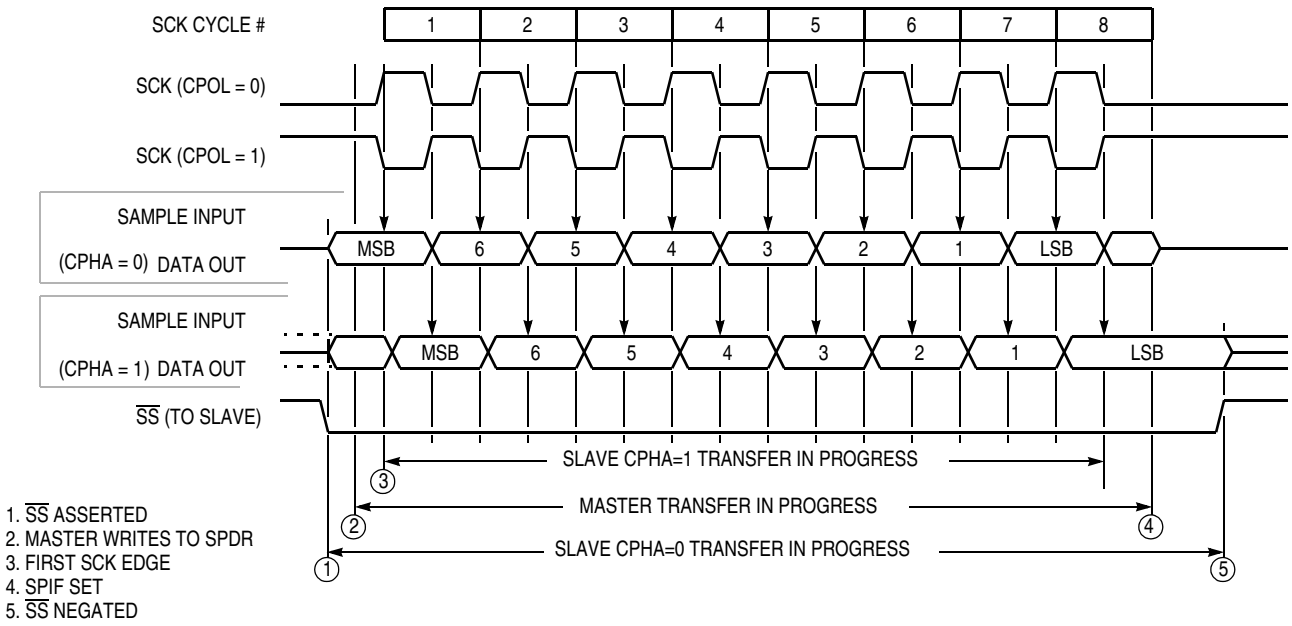


Figure 7-2. SPI Transfer Format

7.4 Clock Phase and Polarity Controls

Software can select one of four combinations of serial clock phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock, and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements.

When CPHA equals 0, the slave select ($\overline{SS}$) line must be negated and reasserted between each successive serial byte. Also, if the slave writes data to the SPI data register (SPDR) while $\overline{SS}$ is active low, a write collision error results.

When CPHA equals 1, the $\overline{SS}$ line can remain low between successive transfers.

7.5 SPI Signals

This subsection contains description of the four SPI signals:

- Master in/slave out (MISO)
- Master out/slave in (MOSI)
- Serial clock (SCK)
- Slave select ($\overline{SS}$)

7.5.1 Master In/Slave Out (MISO)

MISO is one of two unidirectional serial data signals. It is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.

7.5.2 Master Out/Slave In (MOSI)

The MOSI line is the second of the two unidirectional serial data signals. It is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.

7.5.3 Serial Clock (SCK)

SCK, an input to a slave device, is generated by the master device and synchronizes data movement in and out of the device through the MOSI and MISO lines. Master and slave devices are capable of exchanging a byte of information during a sequence of eight clock cycles.

Four possible timing relationships can be chosen by using control bits CPOL and CPHA in the serial peripheral control register (SPCR). Both master and slave devices must operate with the same timing. The SPI clock rate select bits, SPR1 and SPR0, in the SPCR of the master device, select the clock rate. In a slave device, SPR1 and SPR0 have no effect on the operation of the SPI.

7.5.4 Slave Select ($\overline{SS}$)

The $\overline{SS}$ input of a slave device must be externally asserted before a master device can exchange data with the slave device. $\overline{SS}$ must be low before data transactions and must stay low for the duration of the transaction.

The $\overline{SS}$ line of the master must be held high. If it goes low, a mode fault error flag (MODF) is set in the serial peripheral status register (SPSR). To disable the mode fault circuit, write a 1 in bit 5 of the port D data direction register. This sets the $\overline{SS}$ pin to act as a general-purpose output. The other three lines are dedicated to the SPI whenever the serial peripheral interface is on.

The state of the master and slave CPHA bits affects the operation of $\overline{SS}$. CPHA settings should be identical for master and slave. When CPHA = 0, the shift clock is the OR of $\overline{SS}$ with SCK. In this clock phase mode, $\overline{SS}$ must go high between successive characters in an SPI message. When CPHA = 1, $\overline{SS}$ can be left low between successive SPI characters. In cases where there is only one SPI slave MCU, its $\overline{SS}$ line can be tied to V_{SS} as long as only CPHA = 1 clock mode is used.

7.6 SPI System Errors

Two system errors can be detected by the SPI system. The first type of error arises in a multiple-master system when more than one SPI device simultaneously tries to be a master. This error is called a mode fault. The second type of error, write collision, indicates that an attempt was made to write data to the SPDR while a transfer was in progress.

When the SPI system is configured as a master and the $\overline{SS}$ input line goes to active low, a mode fault error has occurred — usually because two devices have attempted to act as master at the same time. In cases where more than one device is concurrently configured as a master, there is a chance of contention between two pin drivers. For push-pull CMOS drivers, this contention can cause permanent damage. The mode fault attempts to protect the device by disabling the drivers. The MSTR control bit in the SPCR and all four DDRD control bits associated with the SPI are cleared. An interrupt is generated subject to masking by the SPIE control bit and the I bit in the CCR.

Other precautions may need to be taken to prevent driver damage. If two devices are made masters at the same time, mode fault does not help protect either one unless one of them selects the other as slave. The amount of damage possible depends on the length of time both devices attempt to act as master.

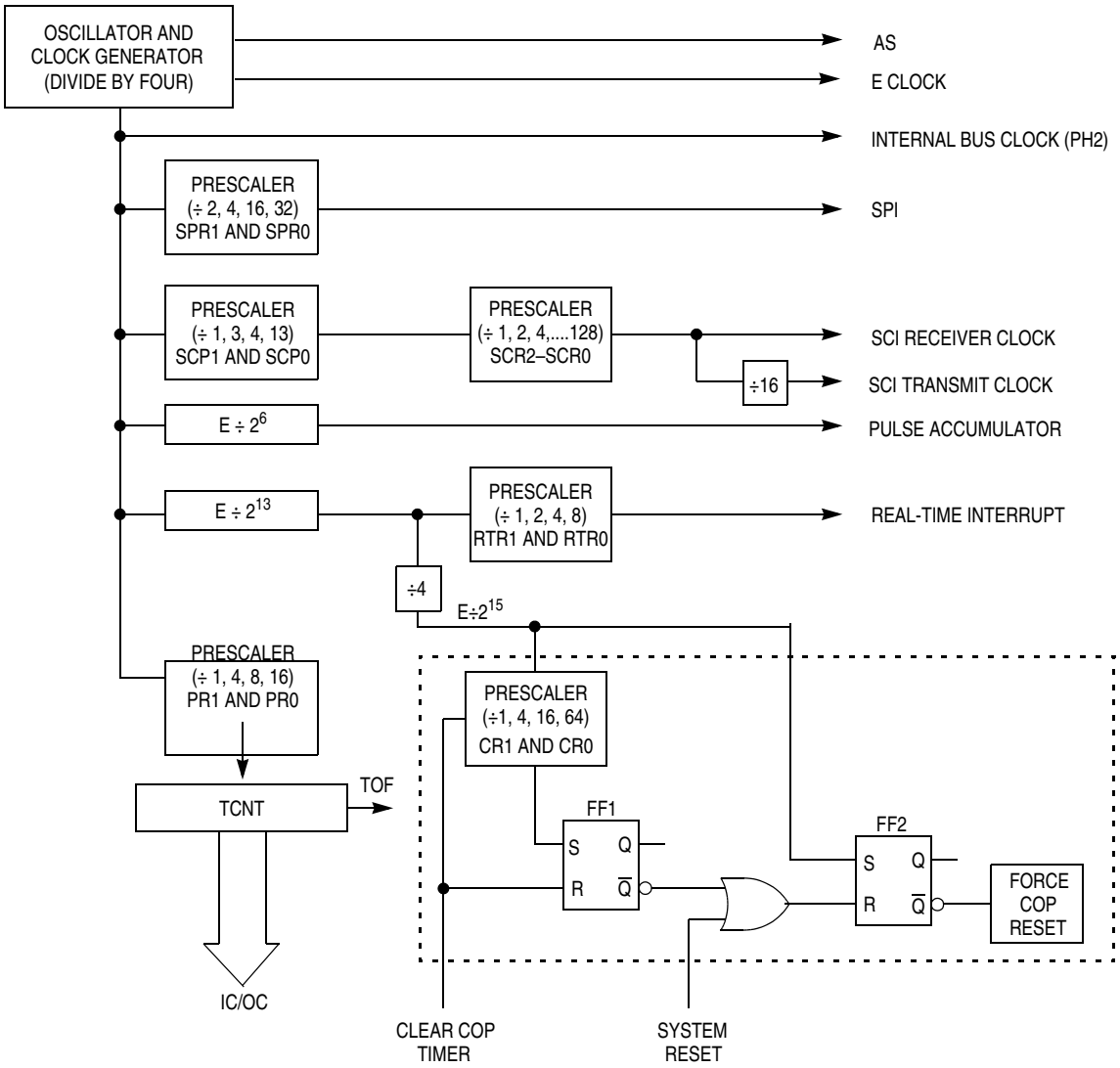


Figure 8-1. Timer Clock Divider Chains

Address:	$0011 — TIC1 (Low)							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Unaffected by reset							
Address:	$0012 — TIC2 (High)							
	Bit 15	14	13	12	11	10	9	Bit 8
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	Unaffected by reset							
Address:	$0013 — TIC2 (Low)							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Unaffected by reset							
Address:	$0014 — TIC3 (High)							
	Bit 15	14	13	12	11	10	9	Bit 8
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	Unaffected by reset							
Address:	$0015 — TIC3 (Low)							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Unaffected by reset							

= Unimplemented

Figure 8-4. Timer Input Capture Registers (TICx) (Continued)

8.3.3 Timer Input Capture 4/Output Compare 5 Register

Use timer input capture 4/output compare 5 (TI4/O5) as either an input capture register or an output compare register, depending on the function chosen for the I4/O5 pin. To enable it as an input capture pin, set the I4/O5 bit in the pulse accumulator control register (PACTL) to logic level 1. To use it as an output compare register, set the I4/O5 bit to a logic level 0. Refer to 8.7 Pulse Accumulator.

Address:	$001E — TI4/O5 (High)							
	Bit 15	14	13	12	11	10	9	Bit 8
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	1	1	1	1	1	1	1	1
Address:	$001F — TI4/O5 (Low)							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	1	1	1	1	1	1	1	1

= Unimplemented

Figure 8-5. Timer Input Capture 4/Output Compare 5 Register (TI4/O5)

Address: $0016 — TOC1 (High)

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1

Address: $0017 — TOC1 (Low)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Address: $0018 — TOC2 (High)

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1

Address: $0019 — TOC2 (Low)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Address: $001A — TOC3 (High)

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1

Address: $001B — TOC3 (Low)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Address: $001C — TOC4 (High)

	Bit 15	14	13	12	11	10	9	Bit 8
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1

Address: $001D — TOC4 (Low)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Figure 8-6. Timer Output Capture Registers (TOCx)

9.3 Functional Operating Temperature Range

Rating	Symbol	Value	Unit
Operating temperature range MC68HC711D3 MC68HC711D3V	T_A	T_L to T_H –40 to +85 –40 to +105	°C

9.4 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Average junction temperature	T_J	$T_A + (P_D \times \Theta_{JA})$	°C
Ambient temperature	T_A	User-determined	°C
Package thermal resistance (junction-to-ambient) 40-pin plastic dual in-line package (DIP) 44-pin plastic leaded chip carrier (PLCC) 44-pin plastic quad flat pack (QFP)	Θ_{JA}	 50 50 85	°C/W
Total power dissipation(1)	P_D	$P_{INT} + P_{I/O}$ $K / T_J + 273°C$	W
Device internal power dissipation	P_{INT}	$I_{DD} \times V_{DD}$	W
I/O pin power dissipation(2)	$P_{I/O}$	User-determined	W
A constant(3)	K	$P_D \times (T_A + 273°C)$ $+ \Theta_{JA} \times P_D^2$	W/°C

1. This is an approximate value, neglecting $P_{I/O}$.
2. For most applications, $P_{I/O} \leq P_{INT}$ and can be neglected.
3. K is a constant pertaining to the device. Solve for K with a known T_A and a measured P_D (at equilibrium). Use this value of K to solve for P_D and T_J, iteratively, for any value of T_A.

9.7 Peripheral Port Timing

Characteristic[1]	Symbol	1.0 MHz		2.0 MHz		3.0 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of operation (E-clock frequency)	f_O	1.0	1.0	2.0	2.0	3.0	3.0	MHz
E-clock period	t_{CYC}	1000	—	500	—	333	—	ns
Peripheral data setup time[2] MCU read of ports A, B, C, and D	t_{PDSU}	100	—	100	—	100	—	ns
Peripheral data hold time[2] MCU read of ports A, B, C, and D	t_{PDH}	50	—	50	—	50	—	ns
Delay time, peripheral data write MCU write to port A MCU writes to ports B, C, and D t_{PWD} = 1/4 t_{cyc} + 150 ns	t_{PWD}	— —	200 350	— —	200 225	— —	200 183	ns

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Port C and D timing is valid for active drive (CWOM and DWOM bits not set in PIOC and SPCR registers respectively).

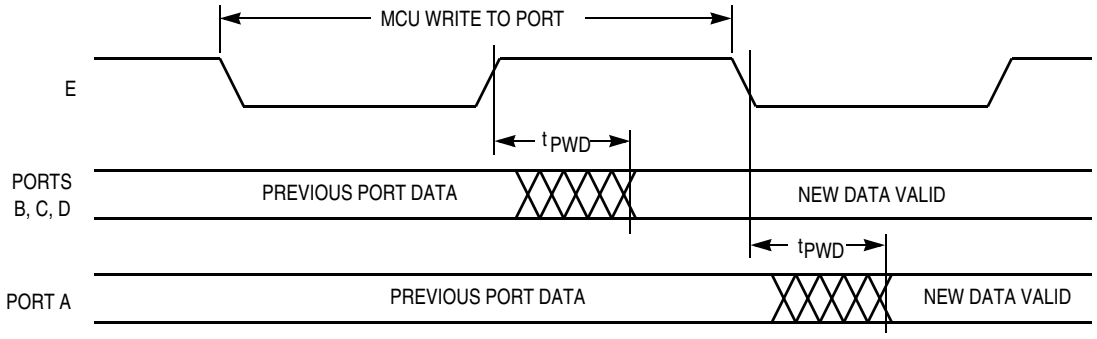


Figure 9-8. Port Write Timing Diagram

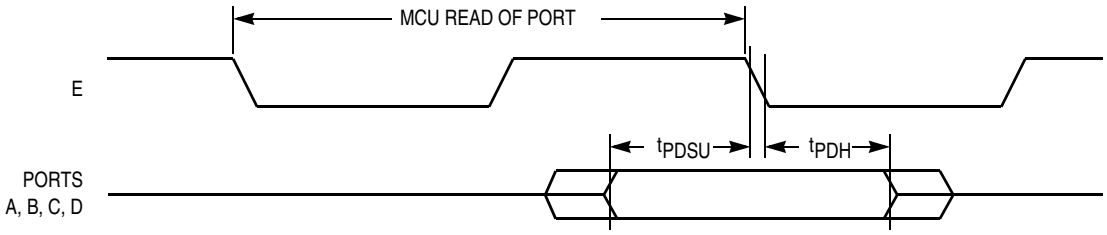
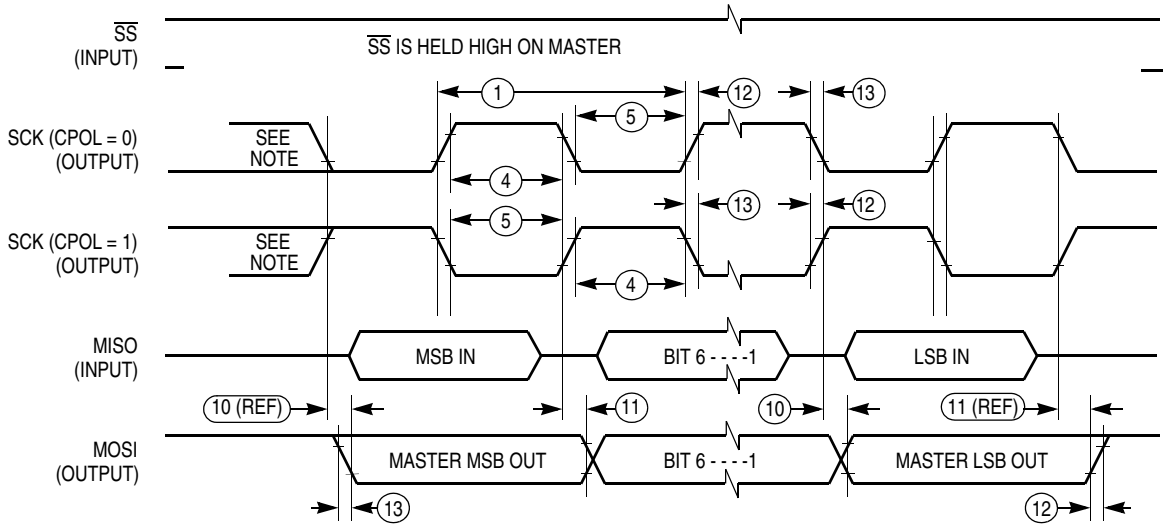
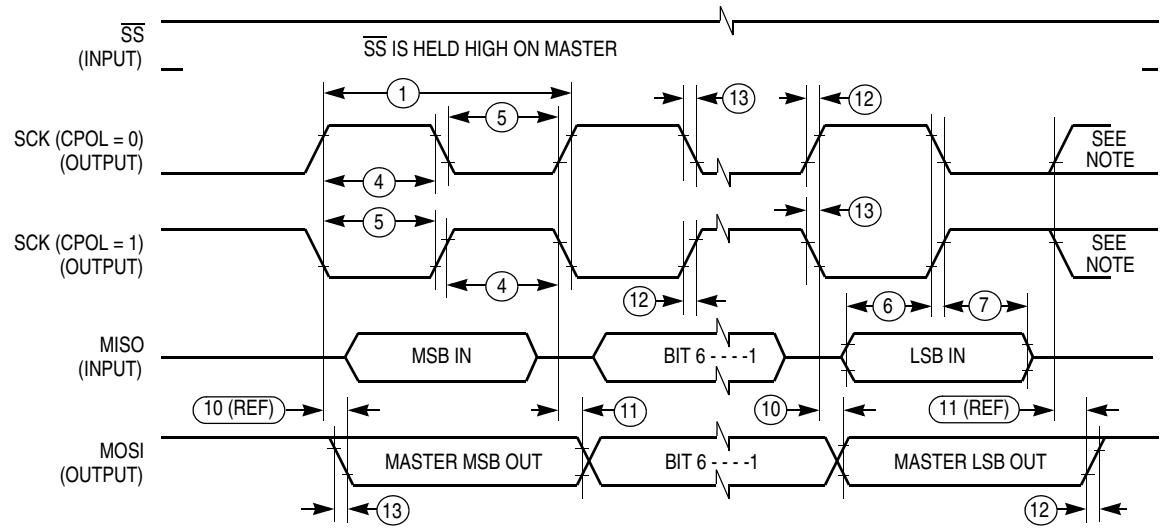


Figure 9-9. Port Read Timing Diagram



Note: This first clock edge is generated internally but is not seen at the SCK pin.

Figure 9-11. SPI Master Timing (CPHA = 0)



Note: This last clock edge is generated internally but is not seen at the SCK pin.

Figure 9-12. SPI Master Timing (CPHA = 1)

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
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Technical Information Center
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