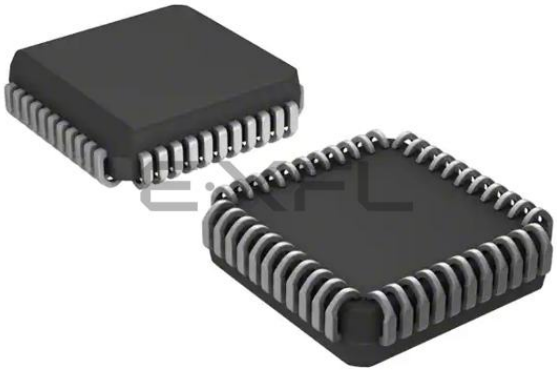

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Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	2MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	26
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68l11d0fne2

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
September, 2003	2	Reformatted to current publications standards	N/A
		Removed references to PROG mode.	Throughout
		Corrected pin assignments for: Figure 1-2. Pin Assignments for 40-Pin Plastic DIP Figure 1-3. Pin Assignments for 44-Pin PLCC Added Figure 1-4. Pin Assignments for 44-Pin QFP	 4 5 6
		1.9 Interrupt Request (IRQ) — Reworked description for clarity.	7
		2.4 Programmable Read-Only Memory (PROM) — Updated with additional data.	13
		Section 10. Ordering Information and Mechanical Specifications — Added mechanical specifications for 44-pin plastic quad flat pack (QFP).	133
		Added the following appendices: Appendix A. MC68HC11D3 and MC68HC11D0 Appendix B. MC68L11D0	 137 143
July, 2005	2.1	Updated to meet Freescale identity guidelines.	Throughout

List of Chapters

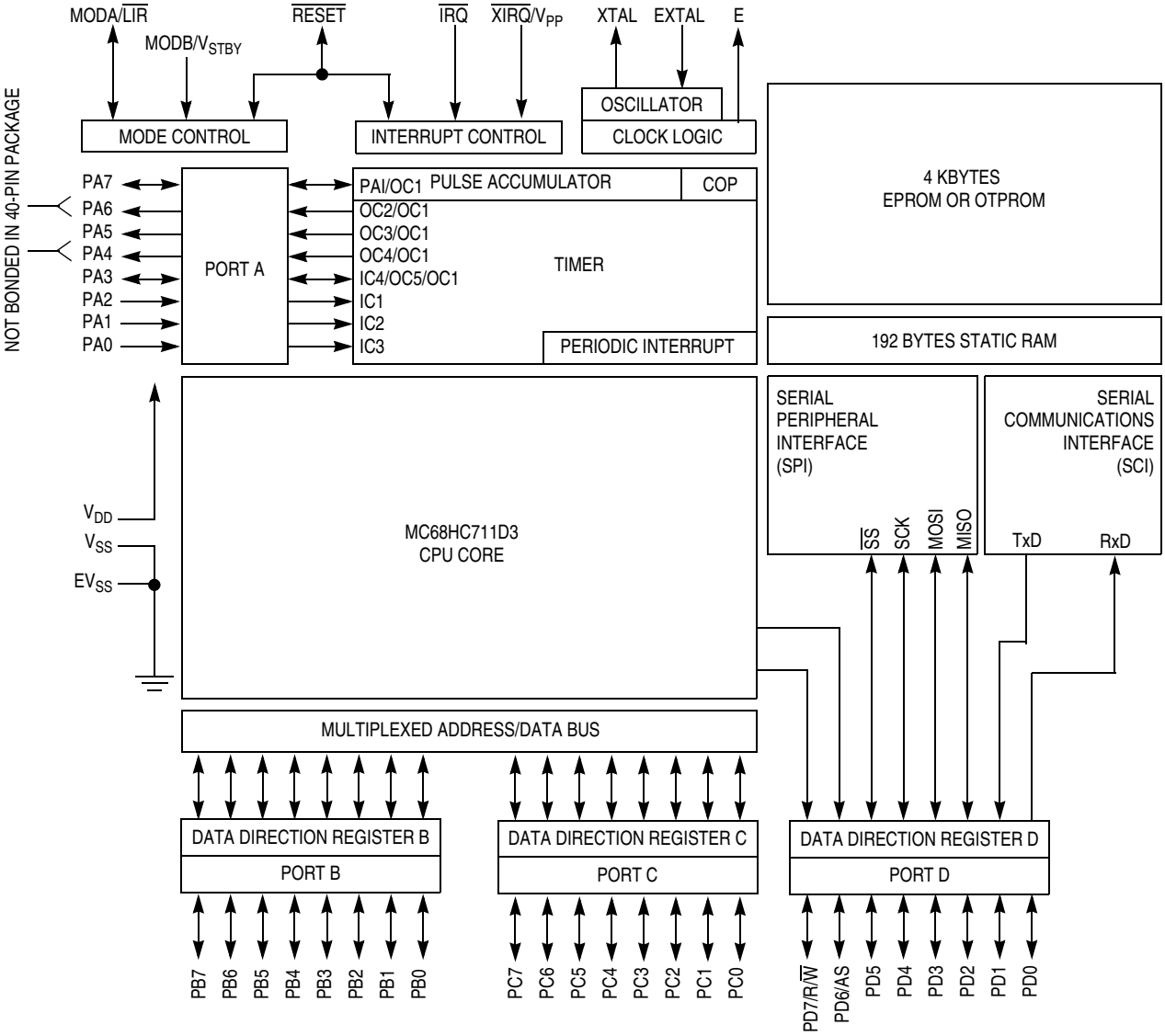

Figure 1-1. MC68HC711D3 Block Diagram

1.4 Pin Descriptions

Refer to Figure 1-2, Figure 1-3, and Figure 1-4 for pin assignments.

If this mode is entered out of reset, the EPROM is located at $7000–$7FFF and vector accesses are from external memory. To be in expanded-multiplexed mode with EPROM located at $F000–$FFFF, it is necessary to start in single-chip mode, executing out of EPROM, and then set the MDA bit of the HPRIO register to switch mode.

NOTE

R/$\overline{W}$, AS, and the high-order address bus (port B) are inputs in single-chip mode. These inputs may need to be pulled up so that off-chip accesses cannot occur while the MCU is in single-chip mode.

2.2.3 Special Bootstrap Mode (BOOT)

This special mode is similar to single-chip mode. The resident bootloader program contains a 256-byte program in a special on-chip read-only memory (ROM). The user downloads a small program into on-board RAM using the SCI port. Program control is passed to RAM when an idle line of at least four characters occurs. In this mode, all interrupt vectors are mapped to RAM (see Table 2-2), so that the user can set up a jump table, if desired.

Bootstrap mode (BOOT) is entered out of reset if the voltage level on both MODA and MODB is low. The programming aspect of bootstrap mode, used to program the one-time programmable ROM (OTPROM) through the MCU, is entered automatically if $\overline{IRQ}$ is low and programming voltage is available on the V_{PP} pin. $\overline{IRQ}$ should be pulled up while in reset with MODA and MODB configured for bootstrap mode to prevent unintentional programming of the EPROM.

This versatile mode (BOOT) can be used for test and diagnostic functions on completed modules and for programming the on-board PROM. The serial receive logic is initialized by software in the bootloader ROM, which provides program control for the SCI baud rate and word format. Mode switching to other modes can occur under program control by writing to the SMOD and MDA bits of the HPRIO register. Two special bootloader functions allow either an immediate jump-to-RAM at memory address $0000 or an immediate jump-to-EPROM at $F000.

Table 2-2. Bootstrap Mode Jump Vectors

Address	Vector
00C4	SCI
00C7	SPI
00CA	Pulse accumulator input edge
00CD	Pulse accumulator overflow
00D0	Timer overflow
00D3	Timer output compare 5/input capture 4
00D6	Timer output compare 4
00D9	Timer output compare 3
00DC	Timer output compare 2
00DF	Timer output compare 1
00E3	Timer input capture 3
00E5	Timer input capture 2
00E8	Timer input capture 1

RAM2–RAM0 (INIT bits 7–4) specify the starting address for the 192 bytes of static RAM. REG3–REG0 (INIT bits 3–0) specify the starting address for the control and status register block. In each case, the four RAM or REG bits become the four upper bits of the 16-bit address of the RAM or register. Since the INIT register is set to $00 by reset, the internal registers begin at $0000 and RAM begins at $0040.

Throughout this document, control and status register addresses are displayed with the high-order digit shown as a bold **0**. This convention indicates that the register block may be relocated to any 4-K memory page, but that its default location is $0000.

RAM and the control and status registers can be relocated independently. If the control and status registers are relocated in such a way as to conflict with PROM, then the register block takes priority, and the EPROM or OTPROM at those locations becomes inaccessible. No harmful conflicts result. Lower priority resources simply become inaccessible. Similarly, if an internal resource conflicts with an external device, no harmful conflict results, since data from the external device is not applied to the internal data bus. Thus, it cannot interfere with the internal read.

NOTE

There are unused register locations in the 64-byte control and status register block. Reads of these unused registers return data from the undriven internal data bus, not from another source that happens to be located at the same address.

2.3.3 Configuration Control Register

The configuration control register (CONFIG) controls the presence of OTPROM or EPROM in the memory map and enables the computer operating properly (COP) watchdog system.

This register is writable only once in expanded and single-chip modes (SMOD = 0). In these mode, the COP watchdog timer is enabled out of reset. In all modes, except normal expanded, EPROM is enabled and located at $F000–$FFFF. In normal expanded mode, EPROM is enabled and located at $7000–$7FFF. Should the user wish to be in expanded mode, but with EPROM mapped at $F000–$FFFF, he must reset in single-chip mode, and write a 1 to the MDA bit in the HPRIO register.

Address: $**0**03F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	0	0	0	0	NOCOP	ROMON	0
Reset:	0	0	0	0	0	U	U	0

U = Unaffected

Figure 2-4. Configuration Control Register (CONFIG)

Bits 7–3 and 0 — Not implemented

Always read 0.

NOCOP — Computer Operating Properly System Disable Bit

This bit is cleared out of reset in normal modes (single chip and expanded), enabling the COP system. It is writable only once after reset in these modes (SMOD = 0). In the special modes (test and bootstrap) (SMOD = 1), this bit comes out of reset set, and is writable any time.

1 = COP system is disabled.

0 = COP system is enabled, reset forced on timeout.

Chapter 3
Central Processor Unit (CPU)

3.1 Introduction

This section presents information on M68HC11 central processor unit (CPU):

- Architecture
- Data types
- Addressing modes
- Instruction set
- Special operations such as subroutine calls and interrupts

The CPU is designed to treat all peripheral, input/output (I/O), and memory locations identically as addresses in the 64-Kbyte memory map. This is referred to as memory-mapped I/O. I/O has no instructions separate from those used by memory. This architecture also allows accessing an operand from an external memory location with no execution time penalty.

3.2 CPU Registers

M68HC11 CPU registers are an integral part of the CPU and are not addressed as if they were memory locations. The seven registers, discussed in the following paragraphs, are shown in Figure 3-1.

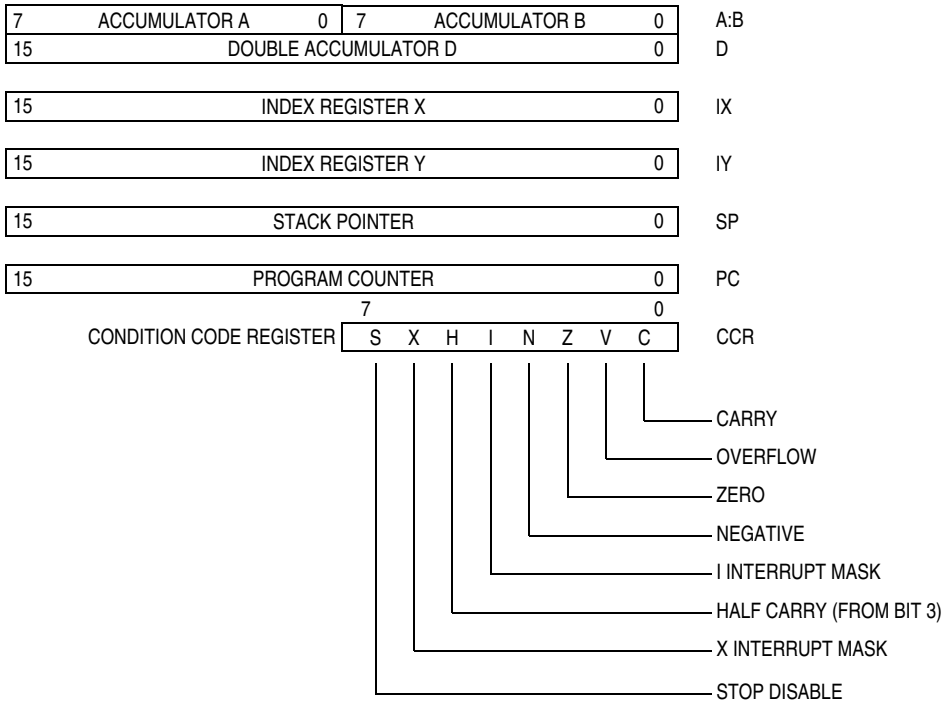

Figure 3-1. Programming Model

5.4 Port C

Port C is an 8-bit, general-purpose I/O port with a data register (PORTC) and a data direction register (DDRC). In the single-chip mode, port C pins are general-purpose I/O pins (PC7–PC0). In the expanded-multiplexed mode, port C pins are configured as multiplexed address/data pins. During the address cycle, bits 7–0 of the address are output on PC7–PC0. During the data cycle, bits 7–0 (PC7–PC0) are bidirectional data pins controlled by the R/$\overline{W}$ signal.

5.4.1 Port C Control Register

Address: $0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	0	CWOM	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 5-4. Port C Control Register (PIOC)

CWOM — Port C Wire-OR Mode Bit

1 = Port C outputs are open drain (to facilitate testing)
0 = Port C operates normally

5.4.2 Port C Data Register

Address: $0003

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Reset:	0	0	0	0	0	0	0	0

Figure 5-5. Port C Data Register (PORTC)

PORTC can be read at any time. Inputs return the sensed levels at the pin, while outputs return the input level of the port C pin drivers. If PORTC is written, the data is stored in an internal latch and can be driven only if port C is configured for general-purpose outputs in single-chip or bootstrap mode.

Port C pins are general-purpose inputs out of reset in single-chip and bootstrap modes. These pins are multiplexed low-order address and data bus lines out of reset in expanded-multiplexed and test modes.

5.4.3 Port C Data Direction Register

Address: $0007

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
Reset:	0	0	0	0	0	0	0	0

Figure 5-6. Data Direction Register for Port C (DDRC)

DDC7–DDC0 — Data Direction Bits for Port C

1 = Corresponding port C pin is configured as output
0 = Corresponding port C pin is configured for input only

5.5 Port D

Port D is an 8-bit, general-purpose I/O port with a data register (PORTD) and a data direction register (DDRD). The eight port D bits (D7–D0) can be used for general-purpose I/O, for the serial communications interface (SCI) and serial peripheral interface (SPI) subsystems, or for bus data direction control

5.5.1 Port D Data Register

Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Reset:	0	0	0	0	0	0	0	0

Figure 5-7. Port D Data Register (PORTD)

PORTD can be read at any time and inputs return the sensed levels at the pin; whereas, outputs return the input level of the port D pin drivers. If PORTD is written, the data is stored in an internal latch, and can be driven only if port D is configured as general-purpose output. This port shares functions with the on-chip SCI and SPI subsystems, while bits 6 and 7 control the direction of data flow on the bus in expanded and special test modes.

5.5.2 Port D Data Direction Register

Address: $0009

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
Reset:	0	0	0	0	0	0	0	0

Figure 5-8. Data Direction Register for Port D (DDRD)

DDD7–DDD0 — Data Direction for Port D

When port D is a general-purpose I/O port, the DDRD register controls the direction of the I/O pins as follows:

0 = Configures the corresponding port D pin for input only
1 = Configures the corresponding port D pin for output

In expanded and test modes, bits 6 and 7 are dedicated AS and R/$\overline{W}$.

When port D is functioning with the SPI system enabled, bit 5 is dedicated as the slave select ($\overline{SS}$) input. In SPI slave mode, DDD5 has no meaning or effect. In SPI master mode, DDD5 affects port D bit 5 as follows:

0 = Port D bit 5 is an error-detect input to the SPI.
1 = Port D bit 5 is configured as a general-purpose output line.

If the SPI is enabled and expects port D bits 2, 3, and 4 (MISO, MOSI, and SCK) to be inputs, then they are inputs, regardless of the state of DDRD bits 2, 3, and 4. If the SPI expects port D bits 2, 3, and 4 to be outputs, they are outputs only if DDRD bits 2, 3, and 4 are set.

SCP1 and SCP0 — SCI Baud Rate Prescaler Select Bits

These two bits select a prescale factor for the SCI baud rate generator that determines the highest possible baud rate.

Table 6-1. Baud Rate Prescale Selects

SCP1 and SCP0	Divide Internal Clock By	Crystal Frequency in MHz			
		4.0 MHz (Baud)	8.0 MHz (Baud)	10.0 MHz (Baud)	12.0 MHz (Baud)
0 0	1	62.50 K	125.0 K	156.25 K	187.5 K
0 1	3	20.83 K	41.67 K	52.08 K	62.5 K
1 0	4	15.625 K	31.25 K	38.4 K	46.88 K
1 1	13	4800	9600	12.02 K	14.42 K

SCR2–SCR0 — SCI Baud Rate Select Bits

These three bits select receiver and transmitter bit rate based on output from baud rate prescaler stage.

Table 6-2. Baud Rate Selects

SCR2–SCR0	Divide Prescaler By	Highest Baud Rate (Prescaler Output from Table 6-1)		
		4800	9600	38.4 K
0 0 0	1	4800	9600	38.4 K
0 0 1	2	2400	4800	19.2 K
0 1 0	4	1200	2400	9600
0 1 1	8	600	1200	4800
1 0 0	16	300	600	2400
1 0 1	32	150	300	1200
1 1 0	64	—	150	600
1 1 1	128	—	—	300

The prescale bits, SCP1 and SCP0, determine the highest baud rate and the SCR2–SCR0 bits select an additional binary submultiple (÷1, ÷2, ÷4, through ÷128) of this highest baud rate. The result of these two dividers in series is the 16 X receiver baud rate clock. The SCR2–SCR0 bits are not affected by reset and can be changed at any time, although they should not be changed when any SCI transfer is in progress.

Figure 6-8 illustrates the SCI baud rate timing chain. The prescale select bits determine the highest baud rate. The rate select bits determine additional divide by two stages to arrive at the receiver timing (RT) clock rate. The baud rate clock is the result of dividing the RT clock by 16.

7.5.2 Master Out/Slave In (MOSI)

The MOSI line is the second of the two unidirectional serial data signals. It is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.

7.5.3 Serial Clock (SCK)

SCK, an input to a slave device, is generated by the master device and synchronizes data movement in and out of the device through the MOSI and MISO lines. Master and slave devices are capable of exchanging a byte of information during a sequence of eight clock cycles.

Four possible timing relationships can be chosen by using control bits CPOL and CPHA in the serial peripheral control register (SPCR). Both master and slave devices must operate with the same timing. The SPI clock rate select bits, SPR1 and SPR0, in the SPCR of the master device, select the clock rate. In a slave device, SPR1 and SPR0 have no effect on the operation of the SPI.

7.5.4 Slave Select ($\overline{SS}$)

The $\overline{SS}$ input of a slave device must be externally asserted before a master device can exchange data with the slave device. $\overline{SS}$ must be low before data transactions and must stay low for the duration of the transaction.

The $\overline{SS}$ line of the master must be held high. If it goes low, a mode fault error flag (MODF) is set in the serial peripheral status register (SPSR). To disable the mode fault circuit, write a 1 in bit 5 of the port D data direction register. This sets the $\overline{SS}$ pin to act as a general-purpose output. The other three lines are dedicated to the SPI whenever the serial peripheral interface is on.

The state of the master and slave CPHA bits affects the operation of $\overline{SS}$. CPHA settings should be identical for master and slave. When CPHA = 0, the shift clock is the OR of $\overline{SS}$ with SCK. In this clock phase mode, $\overline{SS}$ must go high between successive characters in an SPI message. When CPHA = 1, $\overline{SS}$ can be left low between successive SPI characters. In cases where there is only one SPI slave MCU, its $\overline{SS}$ line can be tied to V_{SS} as long as only CPHA = 1 clock mode is used.

7.6 SPI System Errors

Two system errors can be detected by the SPI system. The first type of error arises in a multiple-master system when more than one SPI device simultaneously tries to be a master. This error is called a mode fault. The second type of error, write collision, indicates that an attempt was made to write data to the SPDR while a transfer was in progress.

When the SPI system is configured as a master and the $\overline{SS}$ input line goes to active low, a mode fault error has occurred — usually because two devices have attempted to act as master at the same time. In cases where more than one device is concurrently configured as a master, there is a chance of contention between two pin drivers. For push-pull CMOS drivers, this contention can cause permanent damage. The mode fault attempts to protect the device by disabling the drivers. The MSTR control bit in the SPCR and all four DDRD control bits associated with the SPI are cleared. An interrupt is generated subject to masking by the SPIE control bit and the I bit in the CCR.

Other precautions may need to be taken to prevent driver damage. If two devices are made masters at the same time, mode fault does not help protect either one unless one of them selects the other as slave. The amount of damage possible depends on the length of time both devices attempt to act as master.

CPOL — Clock Polarity Bit

When the clock polarity bit is cleared and data is not being transferred, the SCK pin of the master device has a steady state low value. When CPOL is set, SCK idles high. Refer to Figure 7-2 and 7.4 Clock Phase and Polarity Controls.

CPHA — Clock Phase Bit

The clock phase bit, in conjunction with the CPOL bit, controls the clock-data relationship between master and slave. The CPHA bit selects one of two different clocking protocols. Refer to Figure 7-2 and 7.4 Clock Phase and Polarity Controls.

SPR1 and SPR0 — SPI Clock Rate Select Bits

These two serial peripheral rate bits select one of four baud rates to be used as SCK if the device is a master; however, they have no effect in the slave mode.

Table 7-1. SPI Clock Rates

SPR1 and SPR0	E Clock Divide By	Frequency at E = 2 MHz (Baud)
0 0	2	1.0 MHz
0 1	4	500 kHz
1 0	16	125 kHz
1 1	32	62.5 kHz

7.7.2 SPI Status Register

Address: $0029

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIF	WCOL	0	MODF	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 7-4. SPI Status Register (SPSR)

SPIF — SPI Transfer Complete Flag

SPIF is set upon completion of data transfer between the processor and the external device. If SPIF goes high, and if SPIE is set, a serial peripheral interrupt is generated. To clear the SPIF bit, read the SPSR with SPIF set, then access the SPDR. Unless SPSR is read (with SPIF set) first, attempts to write SPDR are inhibited.

WCOL — Write Collision Bit

Clearing the WCOL bit is accomplished by reading the SPSR (with WCOL set) followed by an access of SPDR. Refer to 7.5.4 Slave Select (SS) and 7.6 SPI System Errors.

0 = No write collision
1 = Write collision

Bit 5 — Not implemented

Always reads 0.

MODF — Mode Fault Bit

To clear the MODF bit, read the SPSR (with MODF set), then write to the SPCR. Refer to 7.5.4 Slave Select (SS) and 7.6 SPI System Errors.

0 = No mode fault
1 = Mode fault

Table 8-1. Timer Summary

Control Bits	XTAL Frequencies			
	4.0 MHz	**8.0 MHz**	**12.0 MHz**	**Other Rates**
	1.0 MHz	**2.0 MHz**	**3.0 MHz**	**(E)**
	1000 ns	**500 ns**	**333 ns**	**(1/E)**
PR1 and PR0	**Main Timer Count Rates**			
0 0 1 count — overflow —	1.0 µs 65.536 ms	500 ns 32.768 ms	333 ns 21.845 ms	(E/1) ($E/2^{16}$)
0 1 1 count — overflow —	4.0 µs 262.14 ms	2.0 µs 131.07 ms	1.333 µs 87.381 ms	(E/4) ($E/2^{18}$)
1 0 1 count — overflow —	8.0 µs 524.29 ms	4.0 µs 262.14 ms	2.667 µs 174.76 ms	(E/8) ($E/2^{19}$)
1 1 1 count — overflow —	16.0 µs 1.049 s	8.0 µs 524.29 ms	5.333 µs 349.52 ms	(E/16) ($E/2^{20}$)

8.2 Timer Structure

Figure 8-2 shows the capture/compare system block diagram. The port A pin control block includes logic for timer functions and for general-purpose input/output (I/O). For pins PA2, PA1, and PA0, this block contains both the edge-detection logic and the control logic that enables the selection of which edge triggers an input capture. The digital level on PA2–PA0 can be read at any time (read PORTA register), even if the pin is being used for the input capture function. Pins PA6–PA4 are used for either general-purpose output or as output compare pins. Pin PA3 can be used for general-purpose I/O, input capture 4, output compare 5, or output compare 1. When one of these pins is being used for an output compare function, it cannot be written directly as if it were a general-purpose output. Each of the output compare functions (OC5–OC2) is related to one of the port A output pins. Output compare 1 (OC1) has extra control logic, allowing it optional control of any combination of the PA7–PA3 pins. The PA7 pin can be used as a general-purpose I/O pin, as an input to the pulse accumulator, or as an OC1 output pin.

8.3 Input Capture

The input capture function records the time an external event occurs by latching the value of the free-running counter when a selected edge is detected at the associated timer input pin. Software can store latched values and use them to compute the periodicity and duration of events. For example, by storing the times of successive edges of an incoming signal, software can determine the period and pulse width of a signal. To measure period, two successive edges of the same polarity are captured. To measure pulse width, two alternate polarity edges are captured.

In most cases, input capture edges are asynchronous to the internal timer counter, which is clocked relative to the PH2 clock. These asynchronous capture requests are synchronized to PH2 so that the latching occurs on the opposite half cycle of PH2 from when the timer counter is being incremented. This synchronization process introduces a delay from when the edge occurs to when the counter value is detected. Because these delays offset each other when the time between two edges is being measured, the delay can be ignored. When an input capture is being used with an output compare, there is a similar delay between the actual compare point and when the output pin changes state.

8.4.4 Output Compare 1 Data Register

Use this register with OC1 to specify the data that is to be stored on the affected pin of port A after a successful OC1 compare. When a successful OC1 compare occurs, a data bit in OC1D is stored in the corresponding bit of port A for each bit that is set in OC1M.

Address: $000D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 8-9. Output Compare 1 Data Register (OC1D)

If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1 compares.

Bits 2–0 — Not implemented; always read 0.

8.4.5 Timer Counter Register

The 16-bit read-only timer count register (TCNT) contains the prescaled value of the 16-bit timer. A full counter read addresses the most significant byte (MSB) first. A read of this address causes the least significant byte (LSB) to be latched into a buffer for the next CPU cycle so that a double-byte read returns the full 16-bit state of the counter at the time of the MSB read cycle.

Address: $000E — TCNT High

	Bit 15	14	13	12	11	10	9	Bit 8
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 08
Write:								
Reset:	0	0	0	0	0	0	0	0

Address: $000F — TCNT Low

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 8-10. Timer Counter Registers (TCNT)

In normal modes, TCNT is read-only.

8.4.8 Timer Interrupt Flag 1 Register

The timer interrupt flag 1 register (TFLG1) bits indicate when timer system events have occurred. Coupled with the bits of TMSK1, the bits of TFLG1 allow the timer subsystem to operate in either a polled or interrupt driven system. Each bit of TFLG1 corresponds to a bit in TMSK1 in the same position.

Address: $0023

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
Reset:	0	0	0	0	0	0	0	0

Figure 8-13. Timer Interrupt Flag 1 Register (TFLG1)

Clear flags by writing a 1 to the corresponding bit position(s).

OC1F–OC5F — Output Compare x Flag
Set each time the counter matches output compare x value

I4/O5F — Input Capture 4/Output Compare 5 Flag
Set by IC4 or OC5, depending on the function enabled by I4/O5 bit in PACTL

IC1F–IC3F — Input Capture x Flag
Set each time a selected active edge is detected on the ICx input line

8.4.9 Timer Interrupt Mask 2 Register

The timer interrupt mask 1 register (TMSK2) is an 8-bit register used to enable or inhibit timer overflow and real-time interrupts. The timer prescaler control bits are included in this register.

Address: $0024

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
Reset:	0	0	0	0	0	0	0	0

Figure 8-14. Timer Interrupt Mask 2 Register (TMSK2)

TOI — Timer Overflow Interrupt Enable Bit
0 = TOF interrupts disabled
1 = Interrupt requested when TOF is set to 1

RTII — Real-Time Interrupt Enable Bit
Refer to 8.5 Real-Time Interrupt.

PAOVI — Pulse Accumulator Overflow Interrupt Enable Bit
Refer to 8.7 Pulse Accumulator.

PAII — Pulse Accumulator Input Edge Interrupt Enable Bit
Refer to 8.7 Pulse Accumulator.

NOTE

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

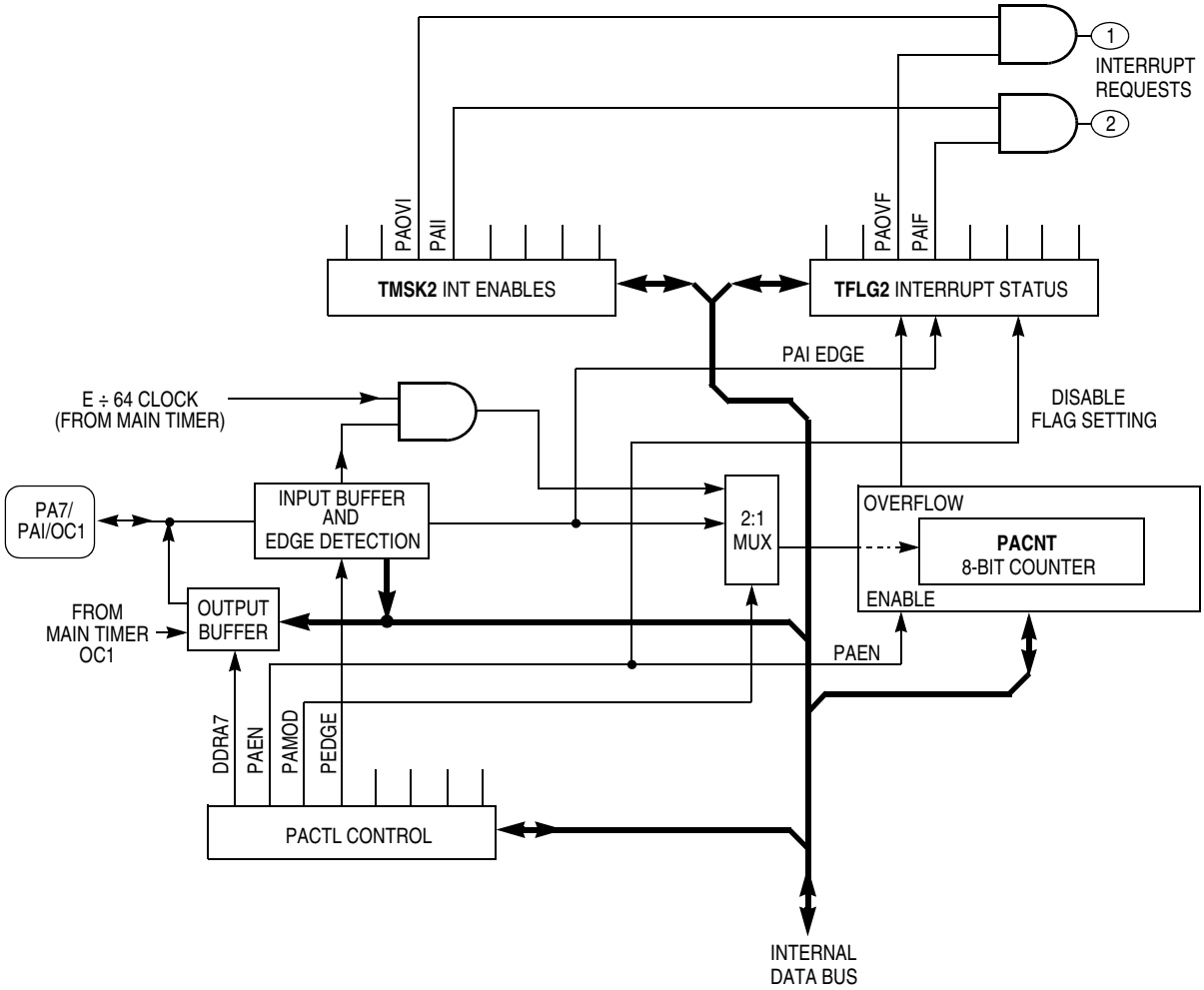

Figure 8-19. Pulse Accumulator

Table 8-7. Pulse Accumulator Timing in Gated Mode

	Selected Crystal	Common XTAL Frequencies		
		4.0 MHz	8.0 MHz	12.0 MHz
CPU Clock	**(E)**	**1.0 MHz**	**2.0 MHz**	**3.0 MHz**
Cycle Time	**(1/E)**	**1000 ns**	**500 ns**	**333 ns**
$(E/2^6)$ $(E/2^{14})$	1 count - overflow -	64.0 µs 16.384 ms	32.0 µs 8.192 ms	21.33 µs 5.461 ms

Chapter 9
Electrical Characteristics

9.1 Introduction

This section contains electrical specifications.

9.2 Maximum Ratings

Maximum ratings are the extreme limits to which the microcontroller unit (MCU) can be exposed without permanently damaging it.

NOTE

This device is not guaranteed to operate properly at the maximum ratings. Refer to 9.5 DC Electrical Characteristics for guaranteed operating conditions.

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Input voltage	V_{In}	–0.3 to +7.0	V
Current drain per pin(1) Excluding V_{DD}, V_{SS}, $V_{RH, and}$ V_{RL}	I_D	25	mA
Storage temperature	T_{STG}	–55 to +150	°C

1. One pin at a time, observing maximum power dissipation limits

NOTE

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{In} and V_{Out} be constrained to the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}).

Appendix A
MC68HC11D3 and MC68HC11D0

A.1 Introduction

The MC68HC11D3 and MC68HC11D0 are read-only memory (ROM) based high-performance microcontrollers (MCU) based on the MC68HC11E9 design. Members of the Dx series are derived from the same mask and feature a high-speed multiplexed bus capable of running at up to 3 MHz and a fully static design that allows operations at frequencies to dc. The only difference between the MCUs in the Dx series is whether the ROM has been tested and guaranteed.

The information contained in this document applies to both the MC68HC11D3 and MC68HC11D0 with the differences given in this appendix.

Features of the MC68HC11D3 and MC68HC11D0 include:

- 4 Kbytes of on-chip ROM (MC68HC11D3)
- 0 bytes of on-chip ROM (MC68HC11D0)
- 192 bytes of on-chip random-access memory (RAM) all saved during standby
- 16-bit timer system:
  - Three input capture (IC) channels
  - Four output compare (OC) channels
  - One IC or OC software-selectable channel
- 32 input/output (I/O) pins:
  - 26 bidirectional I/O pins
  - 3 input-only pins
  - 3 output-only pins
- Available in these packages:
  - 44-pin plastic leaded chip carrier (PLCC)
  - 44-pin quad flat pack (QFP)

A.2 Block Diagram

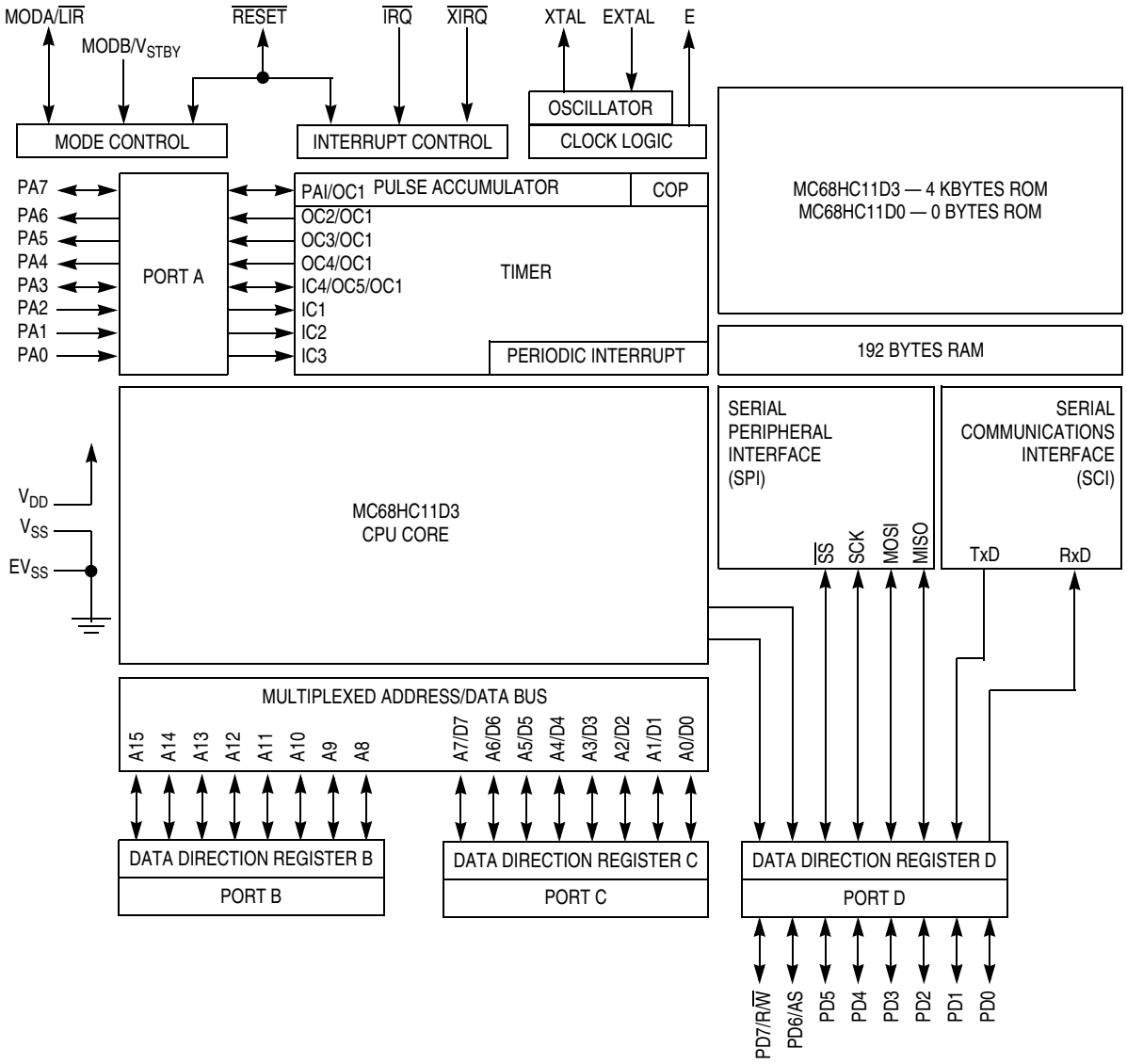

Figure A-1. MC68HC11D3 Block Diagram