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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Active |
| Number of LABs/CLBs | 25391 |
| Number of Logic Elements/Cells | 444343 |
| Total RAM Bits | 19456000 |
| Number of I/O | 468 |
| Number of Gates | - |
| Voltage - Supply | 0.922V ~ 0.979V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 784-BFBGA, FCCSP |
| Supplier Device Package | 784-FCCSPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcku035-2sfva784e |

Summary of Features

Processing System Overview

UltraScale+ MPSoCs feature dual and quad core variants of the ARM Cortex-A53 (APU) with dual-core ARM Cortex-R5 (RPU) processing system (PS). Some devices also include a dedicated ARM Mali™-400 MP2 graphics processing unit (GPU). See [Table 2](#).

Table 2: Zynq UltraScale+ MPSoC Device Features

| | CG Devices | EG Devices | EV Devices |
|-----|--------------------------|--------------------------|--------------------------|
| APU | Dual-core ARM Cortex-A53 | Quad-core ARM Cortex-A53 | Quad-core ARM Cortex-A53 |
| RPU | Dual-core ARM Cortex-R5 | Dual-core ARM Cortex-R5 | Dual-core ARM Cortex-R5 |
| GPU | – | Mali-400MP2 | Mali-400MP2 |
| VCU | – | – | H.264/H.265 |

To support the processors' functionality, a number of peripherals with dedicated functions are included in the PS. For interfacing to external memories for data or configuration storage, the PS includes a multi-protocol dynamic memory controller, a DMA controller, a NAND controller, an SD/eMMC controller and a Quad SPI controller. In addition to interfacing to external memories, the APU also includes a Level-1 (L1) and Level-2 (L2) cache hierarchy; the RPU includes an L1 cache and Tightly Coupled memory subsystem. Each has access to a 256KB on-chip memory.

For high-speed interfacing, the PS includes 4 channels of transmit (TX) and receive (RX) pairs of transceivers, called PS-GTR transceivers, supporting data rates of up to 6.0Gb/s. These transceivers can interface to the high-speed peripheral blocks to support PCIe Gen2 root complex or end point in x1, x2, or x4 configurations; Serial-ATA (SATA) at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates; and up to two lanes of Display Port at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s data rates. The PS-GTR transceivers can also interface to components over USB 3.0 and Serial Gigabit Media Independent Interface (SGMII).

For general connectivity, the PS includes: a pair of USB 2.0 controllers, which can be configured as host, device, or On-The-Go (OTG); an I2C controller; a UART; and a CAN2.0B controller that conforms to ISO11898-1. There are also four triple speed Ethernet MACs and 128 bits of GPIO, of which 78 bits are available through the MIO and 96 through the EMIO.

High-bandwidth connectivity based on the ARM AMBA® AXI4 protocol connects the processing units with the peripherals and provides interface between the PS and the programmable logic (PL).

For additional information, go to: [DS891](#), *Zynq UltraScale+ MPSoC Overview*.

I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken

Data is transported on and off chip through a combination of the high-performance parallel SelectIO™ interface and high-speed serial transceiver connectivity. I/O blocks provide support for cutting-edge memory interface and network protocols through flexible I/O standard and voltage support. The serial transceivers in the UltraScale architecture-based devices transfer data up to 32.75Gb/s, enabling 25G+ backplane designs with dramatically lower power per bit than previous generation transceivers. All transceivers, except the PS-GTR, support the required data rates for PCIe Gen3, and Gen4 (rev 0.5), and integrated blocks for PCIe enable UltraScale devices to support up to Gen4 x8 and Gen3 x16 Endpoint and Root Port designs. Integrated blocks for 150Gb/s Interlaken and 100Gb/s Ethernet (100G MAC/PCS) extend the capabilities of UltraScale devices, enabling simple, reliable support for Nx100G switch and bridge applications. Virtex UltraScale+ HBM devices include Cache Coherent Interconnect for Accelerators (CCIX) ports for coherently sharing data with different processors.

Clocks and Memory Interfaces

UltraScale devices contain powerful clock management circuitry, including clock synthesis, buffering, and routing components that together provide a highly capable framework to meet design requirements. The clock network allows for extremely flexible distribution of clocks to minimize the skew, power consumption, and delay associated with clock signals. The clock management technology is tightly integrated with dedicated memory interface circuitry to enable support for high-performance external memories, including DDR4. In addition to parallel memory interfaces, UltraScale devices support serial memories, such as hybrid memory cube (HMC).

Routing, SSI, Logic, Storage, and Signal Processing

Configurable Logic Blocks (CLBs) containing 6-input look-up tables (LUTs) and flip-flops, DSP slices with 27x18 multipliers, 36Kb block RAMs with built-in FIFO and ECC support, and 4Kx72 UltraRAM blocks (in UltraScale+ devices) are all connected with an abundance of high-performance, low-latency interconnect. In addition to logical functions, the CLB provides shift register, multiplexer, and carry logic functionality as well as the ability to configure the LUTs as distributed memory to complement the highly capable and configurable block RAMs. The DSP slice, with its 96-bit-wide XOR functionality, 27-bit pre-adder, and 30-bit A input, performs numerous independent functions including multiply accumulate, multiply add, and pattern detect. In addition to the device interconnect, in devices using SSI technology, signals can cross between super-logic regions (SLRs) using dedicated, low-latency interface tiles. These combined routing resources enable easy support for next-generation bus data widths. Virtex UltraScale+ HBM devices include up to 8GB of high bandwidth memory.

Configuration, Encryption, and System Monitoring

The configuration and encryption block performs numerous device-level functions critical to the successful operation of the FPGA or MPSoC. This high-performance configuration block enables device configuration from external media through various protocols, including PCIe, often with no requirement to use multi-function I/O pins during configuration. The configuration block also provides 256-bit AES-GCM decryption capability at the same performance as unencrypted configuration. Additional features include SEU detection and correction, partial reconfiguration support, and battery-backed RAM or eFUSE technology for AES key storage to provide additional security. The System Monitor enables the monitoring of the physical environment via on-chip temperature and supply sensors and can also monitor up to 17 external analog inputs. With UltraScale+ MPSoCs, the device is booted via the Configuration and Security Unit (CSU), which supports secure boot via the 256-bit AES-GCM and SHA/384 blocks. The cryptographic engines in the CSU can be used in the MPSoC after boot for user encryption.

Kintex UltraScale+ FPGA Feature Summary

Table 5: Kintex UltraScale+ FPGA Feature Summary

| | KU3P | KU5P | KU9P | KU11P | KU13P | KU15P |
|---|---------|---------|---------|---------|---------|-----------|
| System Logic Cells | 355,950 | 474,600 | 599,550 | 653,100 | 746,550 | 1,143,450 |
| CLB Flip-Flops | 325,440 | 433,920 | 548,160 | 597,120 | 682,560 | 1,045,440 |
| CLB LUTs | 162,720 | 216,960 | 274,080 | 298,560 | 341,280 | 522,720 |
| Max. Distributed RAM (Mb) | 4.7 | 6.1 | 8.8 | 9.1 | 11.3 | 9.8 |
| Block RAM Blocks | 360 | 480 | 912 | 600 | 744 | 984 |
| Block RAM (Mb) | 12.7 | 16.9 | 32.1 | 21.1 | 26.2 | 34.6 |
| UltraRAM Blocks | 48 | 64 | 0 | 80 | 112 | 128 |
| UltraRAM (Mb) | 13.5 | 18.0 | 0 | 22.5 | 31.5 | 36.0 |
| CMTs (1 MMCM and 2 PLLs) | 4 | 4 | 4 | 8 | 4 | 11 |
| Max. HP I/O ⁽¹⁾ | 208 | 208 | 208 | 416 | 208 | 572 |
| Max. HD I/O ⁽²⁾ | 96 | 96 | 96 | 96 | 96 | 96 |
| DSP Slices | 1,368 | 1,824 | 2,520 | 2,928 | 3,528 | 1,968 |
| System Monitor | 1 | 1 | 1 | 1 | 1 | 1 |
| GTH Transceiver 16.3Gb/s | 0 | 0 | 28 | 32 | 28 | 44 |
| GTY Transceivers 32.75Gb/s ⁽³⁾ | 16 | 16 | 0 | 20 | 0 | 32 |
| Transceiver Fractional PLLs | 8 | 8 | 14 | 26 | 14 | 38 |
| PCIe Gen3 x16 and Gen4 x8 | 1 | 1 | 0 | 4 | 0 | 5 |
| 150G Interlaken | 0 | 0 | 0 | 1 | 0 | 4 |
| 100G Ethernet w/RS-FEC | 0 | 1 | 0 | 2 | 0 | 4 |

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTY transceiver line rates are package limited: SFVB784 to 12.5Gb/s; FFVA676, FFVD900, and FFVA1156 to 16.3Gb/s. See [Table 6](#).

Virtex UltraScale FPGA Feature Summary

Table 7: Virtex UltraScale FPGA Feature Summary

| | VU065 | VU080 | VU095 | VU125 | VU160 | VU190 | VU440 |
|--------------------------------|---------|---------|-----------|-----------|-----------|-----------|-----------|
| System Logic Cells | 783,300 | 975,000 | 1,176,000 | 1,566,600 | 2,026,500 | 2,349,900 | 5,540,850 |
| CLB Flip-Flops | 716,160 | 891,424 | 1,075,200 | 1,432,320 | 1,852,800 | 2,148,480 | 5,065,920 |
| CLB LUTs | 358,080 | 445,712 | 537,600 | 716,160 | 926,400 | 1,074,240 | 2,532,960 |
| Maximum Distributed RAM (Mb) | 4.8 | 3.9 | 4.8 | 9.7 | 12.7 | 14.5 | 28.7 |
| Block RAM Blocks | 1,260 | 1,421 | 1,728 | 2,520 | 3,276 | 3,780 | 2,520 |
| Block RAM (Mb) | 44.3 | 50.0 | 60.8 | 88.6 | 115.2 | 132.9 | 88.6 |
| CMT (1 MMCM, 2 PLLs) | 10 | 16 | 16 | 20 | 28 | 30 | 30 |
| I/O DLLs | 40 | 64 | 64 | 80 | 120 | 120 | 120 |
| Maximum HP I/Os ⁽¹⁾ | 468 | 780 | 780 | 780 | 650 | 650 | 1,404 |
| Maximum HR I/Os ⁽²⁾ | 52 | 52 | 52 | 104 | 52 | 52 | 52 |
| DSP Slices | 600 | 672 | 768 | 1,200 | 1,560 | 1,800 | 2,880 |
| System Monitor | 1 | 1 | 1 | 2 | 3 | 3 | 3 |
| PCIe Gen3 x8 | 2 | 4 | 4 | 4 | 4 | 6 | 6 |
| 150G Interlaken | 3 | 6 | 6 | 6 | 8 | 9 | 0 |
| 100G Ethernet | 3 | 4 | 4 | 6 | 9 | 9 | 3 |
| GTH 16.3Gb/s Transceivers | 20 | 32 | 32 | 40 | 52 | 60 | 48 |
| GTY 30.5Gb/s Transceivers | 20 | 32 | 32 | 40 | 52 | 60 | 0 |
| Transceiver Fractional PLLs | 10 | 16 | 16 | 20 | 26 | 30 | 0 |

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

Virtex UltraScale Device-Package Combinations and Maximum I/Os

Table 8: Virtex UltraScale Device-Package Combinations and Maximum I/Os

| Package ⁽¹⁾⁽²⁾⁽³⁾ | Package Dimensions (mm) | VU065 | VU080 | VU095 | VU125 | VU160 | VU190 | VU440 |
|------------------------------|-------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| | | HR, HP GTH, GTY | HR, HP GTH, GTY | HR, HP GTH, GTY | HR, HP GTH, GTY | HR, HP GTH, GTY | HR, HP GTH, GTY | HR, HP GTH, GTY |
| FFVC1517 | 40x40 | 52, 468 20, 20 | 52, 468 20, 20 | 52, 468 20, 20 | | | | |
| FFVD1517 | 40x40 | | 52, 286 32, 32 | 52, 286 32, 32 | | | | |
| FLVD1517 | 40x40 | | | | 52, 286 40, 32 | | | |
| FFVB1760 | 42.5x42.5 | | 52, 650 32, 16 | 52, 650 32, 16 | | | | |
| FLVB1760 | 42.5x42.5 | | | | 52, 650 36, 16 | | | |
| FFVA2104 | 47.5x47.5 | | 52, 780 28, 24 | 52, 780 28, 24 | | | | |
| FLVA2104 | 47.5x47.5 | | | | 52, 780 28, 24 | | | |
| FFVB2104 | 47.5x47.5 | | 52, 650 32, 32 | 52, 650 32, 32 | | | | |
| FLVB2104 | 47.5x47.5 | | | | 52, 650 40, 36 | | | |
| FLGB2104 | 47.5x47.5 | | | | | 52, 650 40, 36 | 52, 650 40, 36 | |
| FFVC2104 | 47.5x47.5 | | | 52, 364 32, 32 | | | | |
| FLVC2104 | 47.5x47.5 | | | | 52, 364 40, 40 | | | |
| FLGC2104 | 47.5x47.5 | | | | | 52, 364 52, 52 | 52, 364 52, 52 | |
| FLGB2377 | 50x50 | | | | | | | 52, 1248 36, 0 |
| FLGA2577 | 52.5x52.5 | | | | | | 0, 448 60, 60 | |
| FLGA2892 | 55x55 | | | | | | | 52, 1404 48, 0 |

Notes:

1. Go to [Ordering Information](#) for package designation details.
2. All packages have 1.0mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.

Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 10: Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

| Package (1)(2)(3) | Package Dimensions (mm) | VU3P | VU5P | VU7P | VU9P | VU11P | VU13P | VU31P | VU33P | VU35P | VU37P |
|----------------------|-------------------------------|---------|---------|---------|----------|---------|----------|---------|---------|---------|---------|
| | | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY |
| FFVC1517 | 40x40 | 520, 40 | | | | | | | | | |
| FLGF1924(4) | 45x45 | | | | | 624, 64 | | | | | |
| FLVA2104 | 47.5x47.5 | | 832, 52 | 832, 52 | | | | | | | |
| FLGA2104 | 47.5x47.5 | | | | 832, 52 | | | | | | |
| FHGA2104 | 52.5x52.5(5) | | | | | | 832, 52 | | | | |
| FLVB2104 | 47.5x47.5 | | 702, 76 | 702, 76 | | | | | | | |
| FLGB2104 | 47.5x47.5 | | | | 702, 76 | 572, 76 | | | | | |
| FHGB2104 | 52.5x52.5(5) | | | | | | 702, 76 | | | | |
| FLVC2104 | 47.5x47.5 | | 416, 80 | 416, 80 | | | | | | | |
| FLGC2104 | 47.5x47.5 | | | | 416, 104 | 416, 96 | | | | | |
| FHGC2104 | 52.5x52.5(5) | | | | | | 416, 104 | | | | |
| FSGD2104 | 47.5x47.5 | | | | 676, 76 | 572, 76 | | | | | |
| FIGD2104 | 52.5x52.5(5) | | | | | | 676, 76 | | | | |
| FLGA2577 | 52.5x52.5 | | | | 448, 120 | 448, 96 | 448, 128 | | | | |
| FSVH1924 | 45x45 | | | | | | | 208, 32 | | | |
| FSVH2104 | 47.5x47.5 | | | | | | | | 208, 32 | 416, 64 | |
| FSVH2892 | 55x55 | | | | | | | | | 416, 64 | 624, 96 |

Notes:

- Go to [Ordering Information](#) for package designation details.
- All packages have 1.0mm ball pitch.
- Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.
- GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s.
- These 52.5x52.5mm overhang packages have the same PCB ball footprint as the corresponding 47.5x47.5mm packages (i.e., the same last letter and number sequence) and are footprint compatible.

Zynq UltraScale+: CG Device Feature Summary

Table 11: Zynq UltraScale+: CG Device Feature Summary

| | ZU2CG | ZU3CG | ZU4CG | ZU5CG | ZU6CG | ZU7CG | ZU9CG |
|---|---|---------|---------|---------|---------|---------|---------|
| Application Processing Unit | Dual-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache | | | | | | |
| Real-Time Processing Unit | Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM | | | | | | |
| Embedded and External Memory | 256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC | | | | | | |
| General Connectivity | 214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters | | | | | | |
| High-Speed Connectivity | 4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII | | | | | | |
| System Logic Cells | 103,320 | 154,350 | 192,150 | 256,200 | 469,446 | 504,000 | 599,550 |
| CLB Flip-Flops | 94,464 | 141,120 | 175,680 | 234,240 | 429,208 | 460,800 | 548,160 |
| CLB LUTs | 47,232 | 70,560 | 87,840 | 117,120 | 214,604 | 230,400 | 274,080 |
| Distributed RAM (Mb) | 1.2 | 1.8 | 2.6 | 3.5 | 6.9 | 6.2 | 8.8 |
| Block RAM Blocks | 150 | 216 | 128 | 144 | 714 | 312 | 912 |
| Block RAM (Mb) | 5.3 | 7.6 | 4.5 | 5.1 | 25.1 | 11.0 | 32.1 |
| UltraRAM Blocks | 0 | 0 | 48 | 64 | 0 | 96 | 0 |
| UltraRAM (Mb) | 0 | 0 | 14.0 | 18.0 | 0 | 27.0 | 0 |
| DSP Slices | 240 | 360 | 728 | 1,248 | 1,973 | 1,728 | 2,520 |
| CMTs | 3 | 3 | 4 | 4 | 4 | 8 | 4 |
| Max. HP I/O ⁽¹⁾ | 156 | 156 | 156 | 156 | 208 | 416 | 208 |
| Max. HD I/O ⁽²⁾ | 96 | 96 | 96 | 96 | 120 | 48 | 120 |
| System Monitor | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| GTH Transceiver 16.3Gb/s ⁽³⁾ | 0 | 0 | 16 | 16 | 24 | 24 | 24 |
| GTY Transceivers 32.75Gb/s | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Transceiver Fractional PLLs | 0 | 0 | 8 | 8 | 12 | 12 | 12 |
| PCIe Gen3 x16 and Gen4 x8 | 0 | 0 | 2 | 2 | 0 | 2 | 0 |
| 150G Interlaken | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 100G Ethernet w/ RS-FEC | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 12](#).

Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

Table 14: Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

| Package (1)(2)(3)(4)(5) | Package Dimensions (mm) | ZU2EG | ZU3EG | ZU4EG | ZU5EG | ZU6EG | ZU7EG | ZU9EG | ZU11EG | ZU15EG | ZU17EG | ZU19EG |
|----------------------------|-------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| | | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY |
| SBVA484(6) | 19x19 | 24, 58 0, 0 | 24, 58 0, 0 | | | | | | | | | |
| SFVA625 | 21x21 | 24, 156 0, 0 | 24, 156 0, 0 | | | | | | | | | |
| SFVC784(7) | 23x23 | 96, 156 0, 0 | 96, 156 0, 0 | 96, 156 4, 0 | 96, 156 4, 0 | | | | | | | |
| FBVB900 | 31x31 | | | 48, 156 16, 0 | 48, 156 16, 0 | | 48, 156 16, 0 | | | | | |
| FFVC900 | 31x31 | | | | | 48, 156 16, 0 | | 48, 156 16, 0 | | 48, 156 16, 0 | | |
| FFVB1156 | 35x35 | | | | | 120, 208 24, 0 | | 120, 208 24, 0 | | 120, 208 24, 0 | | |
| FFVC1156 | 35x35 | | | | | | 48, 312 20, 0 | | 48, 312 20, 0 | | | |
| FFVB1517 | 40x40 | | | | | | | | 72, 416 16, 0 | | 72, 572 16, 0 | 72, 572 16, 0 |
| FFVF1517 | 40x40 | | | | | | 48, 416 24, 0 | | 48, 416 32, 0 | | | |
| FFVC1760 | 42.5x42.5 | | | | | | | | 96, 416 32, 16 | | 96, 416 32, 16 | 96, 416 32, 16 |
| FFVD1760 | 42.5x42.5 | | | | | | | | | | 48, 260 44, 28 | 48, 260 44, 28 |
| FFVE1924 | 45x45 | | | | | | | | | | 96, 572 44, 0 | 96, 572 44, 0 |

Notes:

- Go to [Ordering Information](#) for package designation details.
- FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
- All device package combinations bond out 4 PS-GTR transceivers.
- All device package combinations bond out 214 PS I/O except ZU2EG and ZU3EG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
- Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
- All 58 HP I/O pins are powered by the same V_{CCO} supply.
- GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

Graphics Processing Unit (GPU)

The dedicated ARM Mali-400 MP2 GPU in the PS supports 2D and 3D graphics acceleration up to 1080p resolution. The Mali-400 supports OpenGL ES 1.1 and 2.0 for 3D graphics and Open VG 1.1 standards for 2D vector graphics. It has a geometry processor (GP) and 2 pixel processors to perform tile rendering operations in parallel. It has dedicated Memory management units for GP and pixel processors, which supports 4 KB page size. The GPU also has 64KB level-2 (L2) read-only cache. It supports 4X and 16X Full scene Anti-Aliasing (FSAA). It is fully autonomous, enabling maximum parallelization between APU and GPU. It has built-in hardware texture decompression, allowing the texture to remain compressed (in ETC format) in graphics hardware and decompress the required samples on the fly. It also supports efficient alpha blending of multiple layers in hardware without additional bandwidth consumption. It has a pixel fill rate of 2Mpixel/sec/MHz and a triangle rate of 0.1Mvertex/sec/MHz. The GPU supports extensive texture format for RGBA 8888, 565, and 1556 in Mono 8, 16, and YUV formats. For power sensitive applications, the GPU supports clock and power gating for each GP, pixel processors, and L2 cache. During power gating, GPU does not consume any static or dynamic power; during clock gating, it only consumes static power.

Video Codec Unit (VCU)

The video codec unit (VCU) provides multi-standard video encoding and decoding capabilities, including: High Efficiency Video Coding (HEVC), i.e., H.265; and Advanced Video Coding (AVC), i.e., H.264 standards. The VCU is capable of simultaneous encode and decode at rates up to 4Kx2K at 60 frames per second (fps) (approx. 600Mpixel/sec) or 8Kx4K at a reduced frame rate (~15fps).

Input/Output

All UltraScale devices, whether FPGA or MPSoC, have I/O pins for communicating to external components. In addition, in the MPSoC's PS, there are another 78 I/Os that the I/O peripherals use to communicate to external components, referred to as multiplexed I/O (MIO). If more than 78 pins are required by the I/O peripherals, the I/O pins in the PL can be used to extend the MPSoC interfacing capability, referred to as extended MIO (EMIO).

The number of I/O pins in UltraScale FPGAs and in the programmable logic of UltraScale+ MPSoCs varies depending on device and package. Each I/O is configurable and can comply with a large number of I/O standards. The I/Os are classed as high-range (HR), high-performance (HP), or high-density (HD). The HR I/Os offer the widest range of voltage support, from 1.2V to 3.3V. The HP I/Os are optimized for highest performance operation, from 1.0V to 1.8V. The HD I/Os are reduced-feature I/Os organized in banks of 24, providing voltage support from 1.2V to 3.3V.

All I/O pins are organized in banks, with 52 HP or HR pins per bank or 24 HD pins per bank. Each bank has one common V_{CCO} output buffer power supply, which also powers certain input buffers. In addition, HR banks can be split into two half-banks, each with their own V_{CCO} supply. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). V_{REF} pins can be driven directly from the PCB or internally generated using the internal V_{REF} generator circuitry present in each bank.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100Ω internal resistor. All UltraScale devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. UltraScale+ families add support for MIPI with a dedicated D-PHY in the I/O bank.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

High-Speed Serial Transceivers

Serial data transmission between devices on the same PCB, over backplanes, and across even longer distances is becoming increasingly important for scaling to 100Gb/s and 400Gb/s line cards. Specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues are required at these high data rates.

Three types of transceivers are used in the UltraScale architecture: GTH and GTY in FPGAs and MPSoC PL, and PS-GTR in the MPSoC PS. All transceivers are arranged in groups of four, known as a transceiver Quad. Each serial transceiver is a combined transmitter and receiver. [Table 17](#) compares the available transceivers.

Table 17: Transceiver Information

| | Kintex UltraScale | | Kintex UltraScale+ | | Virtex UltraScale | | Virtex UltraScale+ | Zynq UltraScale+ | | |
|----------------|---|---|---|---|---|---|---|--|---|---|
| Type | GTH | GTY | GTH | GTY | GTH | GTY | GTY | PS-GTR | GTH | GTY |
| Qty | 16–64 | 0–32 | 20–60 | 0–60 | 20–60 | 0–60 | 40–128 | 4 | 0–44 | 0–28 |
| Max. Data Rate | 16.3Gb/s | 16.3Gb/s | 16.3Gb/s | 32.75Gb/s | 16.3Gb/s | 30.5Gb/s | 32.75Gb/s | 6.0Gb/s | 16.3Gb/s | 32.75Gb/s |
| Min. Data Rate | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 1.25Gb/s | 0.5Gb/s | 0.5Gb/s |
| Key Apps | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC | <ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC | <ul style="list-style-type: none"> PCIe Gen2 USB Ethernet | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC |

The following information in this section pertains to the GTH and GTY only.

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally “auto-adapt” to automatically learn and compensate for different interconnect characteristics. This enables even more margin for 10G+ and 25G+ backplanes.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

Integrated Interface Blocks for PCI Express Designs

The UltraScale architecture includes integrated blocks for PCIe technology that can be configured as an Endpoint or Root Port. UltraScale devices are compliant to the PCI Express Base Specification Revision 3.0. UltraScale+ devices are compliant to the PCI Express Base Specification Revision 3.1 for Gen3 and lower data rates, and compatible with the PCI Express Base Specification Revision 4.0 (rev 0.5) for Gen4 data rates.

The Root Port can be used to build the basis for a compatible Root Complex, to allow custom chip-to-chip communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the FPGA or MPSoC.

This block is highly configurable to system design requirements and can operate up to the maximum lane widths and data rates listed in [Table 18](#).

Table 18: PCIe Maximum Configurations

| | Kintex UltraScale | Kintex UltraScale+ | Virtex UltraScale | Virtex UltraScale+ | Zynq UltraScale+ |
|------------------------------|----------------------|-----------------------|----------------------|-----------------------|---------------------|
| Gen1 (2.5Gb/s) | x8 | x16 | x8 | x16 | x16 |
| Gen2 (5Gb/s) | x8 | x16 | x8 | x16 | x16 |
| Gen3 (8Gb/s) | x8 | x16 | x8 | x16 | x16 |
| Gen4 (16Gb/s) ⁽¹⁾ | | x8 | | x8 | x8 |

Notes:

1. Transceivers in Kintex UltraScale and Virtex UltraScale devices are capable of operating at Gen4 data rates.

For high-performance applications, advanced buffering techniques of the block offer a flexible maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block for PCIe, the transceivers, block RAM, and clocking resources) into an Endpoint or Root Port solution. The system designer has control over many configurable parameters: link width and speed, maximum payload size, FPGA or MPSoC logic interface speeds, reference clock frequency, and base address register decoding and filtering.

Cache Coherent Interconnect for Accelerators (CCIX)

CCIX is a chip-to-chip interconnect operating at data rates up to 25Gb/s that allows two or more devices to share memory in a cache coherent manner. Using PCIe for the transport layer, CCIX can operate at several standard data rates (2.5, 5, 8, and 16Gb/s) with an additional high-speed 25Gb/s option. The specification employs a subset of full coherency protocols and ensures that FPGAs used as accelerators can coherently share data with processors using different instruction set architectures.

Virtex UltraScale+ HBM devices support CCIX data rates up to 16Gb/s and contain four CCIX ports and at least four integrated blocks for PCIe. Each CCIX port requires the use of one integrated block for PCIe. If not used with a CCIX port, the integrated blocks for PCIe can still be used for PCIe communication.

Integrated Block for Interlaken

Some UltraScale architecture-based devices include integrated blocks for Interlaken. Interlaken is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gb/s to 150Gb/s. The Interlaken integrated block in the UltraScale architecture is compliant to revision 1.2 of the Interlaken specification with data striping and de-striping across 1 to 12 lanes. Permitted configurations are: 1 to 12 lanes at up to 12.5Gb/s and 1 to 6 lanes at up to 25.78125Gb/s, enabling flexible support for up to 150Gb/s per integrated block. With multiple Interlaken blocks, certain UltraScale devices enable easy, reliable Interlaken switches and bridges.

Integrated Block for 100G Ethernet

Compliant to the IEEE Std 802.3ba, the 100G Ethernet integrated blocks in the UltraScale architecture provide low latency 100Gb/s Ethernet ports with a wide range of user customization and statistics gathering. With support for 10 x 10.3125Gb/s (CAUI) and 4 x 25.78125Gb/s (CAUI-4) configurations, the integrated block includes both the 100G MAC and PCS logic with support for IEEE Std 1588v2 1-step and 2-step hardware timestamping.

In UltraScale+ devices, the 100G Ethernet blocks contain a Reed Solomon Forward Error Correction (RS-FEC) block, compliant to IEEE Std 802.3bj, that can be used with the Ethernet block or stand alone in user applications. These families also support OTN mapping mode in which the PCS can be operated without using the MAC.

The MMCM can have a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of 1/8 and can thus increase frequency synthesis capabilities by a factor of 8. The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency. At 1,600MHz, the phase-shift timing increment is 11.2ps.

PLL

With fewer features than the MMCM, the two PLLs in a clock management tile are primarily present to provide the necessary clocks to the dedicated memory interface circuitry. The circuit at the center of the PLLs is similar to the MMCM, with PFD feeding a VCO and programmable M, D, and O counters. There are two divided outputs to the device fabric per PLL as well as one clock plus one enable signal to the memory interface circuitry.

UltraScale+ MPSoCs are equipped with five additional PLLs in the PS for independently configuring the four primary clock domains with the PS: the APU, the RPU, the DDR controller, and the I/O peripherals.

Clock Distribution

Clocks are distributed throughout UltraScale devices via buffers that drive a number of vertical and horizontal tracks. There are 24 horizontal clock routes per clock region and 24 vertical clock routes per clock region with 24 additional vertical clock routes adjacent to the MMCM and PLL. Within a clock region, clock signals are routed to the device logic (CLBs, etc.) via 16 gateable leaf clocks.

Several types of clock buffers are available. The BUFGCE and BUFCE_LEAF buffers provide clock gating at the global and leaf levels, respectively. BUFGCTRL provides glitchless clock muxing and gating capability. BUFGCE_DIV has clock gating capability and can divide a clock by 1 to 8. BUFG_GT performs clock division from 1 to 8 for the transceiver clocks. In MPSoCs, clocks can be transferred from the PS to the PL using dedicated buffers.

Memory Interfaces

Memory interface data rates continue to increase, driving the need for dedicated circuitry that enables high performance, reliable interfacing to current and next-generation memory technologies. Every UltraScale device includes dedicated physical interfaces (PHY) blocks located between the CMT and I/O columns that support implementation of high-performance PHY blocks to external memories such as DDR4, DDR3, QDRII+, and RLDRAM3. The PHY blocks in each I/O bank generate the address/control and data bus signaling protocols as well as the precision clock/data alignment required to reliably communicate with a variety of high-performance memory standards. Multiple I/O banks can be used to create wider memory interfaces.

As well as external parallel memory interfaces, UltraScale FPGAs and MPSoCs can communicate to external serial memories, such as Hybrid Memory Cube (HMC), via the high-speed serial transceivers. All transceivers in the UltraScale architecture support the HMC protocol, up to 15Gb/s line rates. UltraScale devices support the highest bandwidth HMC configuration of 64 lanes with a single FPGA.

Block RAM

Every UltraScale architecture-based device contains a number of 36 Kb block RAMs, each with two completely independent ports that share only the stored data. Each block RAM can be configured as one 36Kb RAM or two independent 18Kb RAMs. Each memory access, read or write, is controlled by the clock. Connections in every block RAM column enable signals to be cascaded between vertically adjacent block RAMs, providing an easy method to create large, fast memory arrays, and FIFOs with greatly reduced power consumption.

All inputs, data, address, clock enables, and write enables are registered. The input address is always clocked (unless address latching is turned off), retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency. During a write operation, the data output can reflect either the previously stored data or the newly written data, or it can remain unchanged. Block RAM sites that remain unused in the user design are automatically powered down to reduce total power consumption. There is an additional pin on every block RAM to control the dynamic power gating feature.

Programmable Data Width

Each port can be configured as $32K \times 1$; $16K \times 2$; $8K \times 4$; $4K \times 9$ (or 8); $2K \times 18$ (or 16); $1K \times 36$ (or 32); or 512×72 (or 64). Whether configured as block RAM or FIFO, the two ports can have different aspect ratios without any constraints. Each block RAM can be divided into two completely independent 18Kb block RAMs that can each be configured to any aspect ratio from $16K \times 1$ to 512×36 . Everything described previously for the full 36Kb block RAM also applies to each of the smaller 18Kb block RAMs. Only in simple dual-port (SDP) mode can data widths of greater than 18bits (18Kb RAM) or 36 bits (36Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72. Both sides of the dual-port 36Kb RAM can be of variable width.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

Each block RAM can be configured as a 36Kb FIFO or an 18Kb FIFO. The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, programmable full, and programmable empty. The programmable flags allow the user to specify the FIFO counter values that make these flags go active. The FIFO width and depth are programmable with support for different read port and write port widths on a single FIFO. A dedicated cascade path allows for easy creation of deeper FIFOs.

Ordering Information

Table 21 shows the speed and temperature grades available in the different device families. V_{CCINT} supply voltage is listed in parentheses.

Table 21: Speed Grade and Temperature Grade

| Device Family | Devices | Speed Grade and Temperature Grade | | | |
|--------------------|--|-----------------------------------|---------------------------|--------------------------------------|--------------------------------------|
| | | Commercial (C) | Extended (E) | | Industrial (I) |
| | | 0°C to +85°C | 0°C to +100°C | 0°C to +110°C | –40°C to +100°C |
| Kintex UltraScale | All | | -3E ⁽¹⁾ (1.0V) | | |
| | | | -2E (0.95V) | | -2I (0.95V) |
| | | -1C (0.95V) | | | -1I (0.95V) |
| | | | | | -1LI ⁽¹⁾ (0.95V or 0.90V) |
| Kintex UltraScale+ | All | | -3E (0.90V) | | |
| | | | -2E (0.85V) | | -2I (0.85V) |
| | | | | -2LE ⁽²⁾ (0.85V or 0.72V) | |
| | | | -1E (0.85V) | | -1I (0.85V) |
| | | | | | -1LI (0.85V or 0.72V) |
| Virtex UltraScale | VU065 VU080 VU095 VU125 VU160 VU190 | | -3E (1.0V) | | |
| | | | -2E (0.95V) | | -2I (0.95V) |
| | | | -1HE (0.95V or 1.0V) | | -1I (0.95V) |
| | | | | | |
| | VU440 | | -3E (1.0V) | | |
| | | | -2E (0.95V) | | -2I (0.95V) |
| | | -1C (0.95V) | | | -1I (0.95V) |
| Virtex UltraScale+ | VU3P VU5P VU7P VU9P VU11P VU13P | | -3E (0.90V) | | |
| | | | -2E (0.85V) | | -2I (0.85V) |
| | | | | -2LE ⁽²⁾ (0.85V or 0.72V) | |
| | | | -1E (0.85V) | | -1I (0.85V) |
| | | | | | |
| | | | | | |
| | VU31P VU33P VU35P VU37P | | -3E (0.90V) | | |
| | | | -2E (0.85V) | | |
| | | | | -2LE ⁽²⁾ (0.85V or 0.72V) | |
| | | | -1E (0.85V) | | |

The ordering information shown in Figure 4 applies to all packages in the Kintex UltraScale+ and Virtex UltraScale+ FPGAs, and Figure 5 applies to Zynq UltraScale+.

The -1L and -2L speed grades in the UltraScale+ families can run at one of two different V_{CCINT} operating voltages. At 0.72V, they operate at similar performance to the Kintex UltraScale and Virtex UltraScale devices with up to 30% reduction in power consumption. At 0.85V, they consume similar power to the Kintex UltraScale and Virtex UltraScale devices, but operate over 30% faster.

For UltraScale+ devices, the information in this document is pre-release, provided ahead of silicon ordering availability. Please contact your Xilinx sales representative for more information on Early Access Programs.

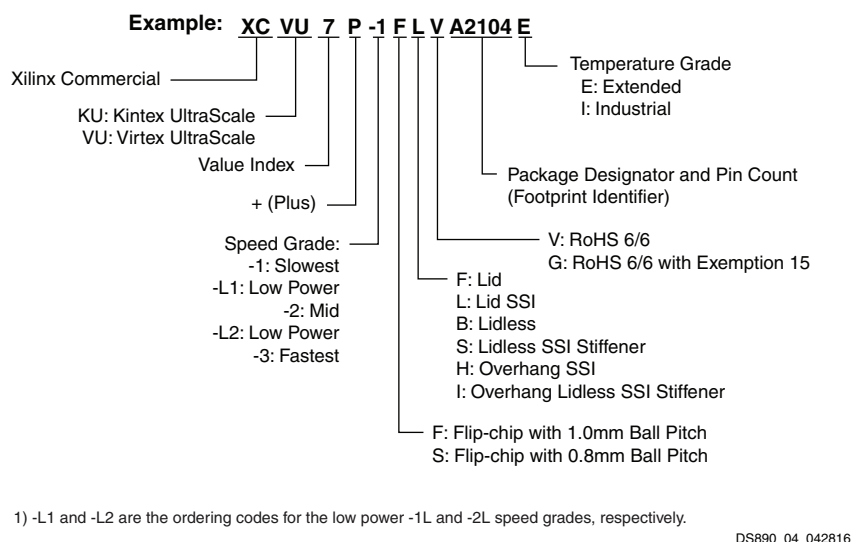


Figure 4: UltraScale+ FPGA Ordering Information



Figure 5: Zynq UltraScale+ Ordering Information

Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|------------|---------|--|
| 02/15/2017 | 2.11 | Updated Table 1 , Table 9 : Converted HBM from Gb to GB. Updated Table 11 , Table 13 , and Table 15 : Updated DSP count for Zynq UltraScale+ MPSoCs. Updated Cache Coherent Interconnect for Accelerators (CCIX) . Updated High Bandwidth Memory (HBM) . Updated Table 21 : Added -2E speed grade to all UltraScale+ devices. Removed -3E from XCZU2 and XCZU3. |
| 11/09/2016 | 2.10 | Updated Table 1 . Added HBM devices to Table 9 , Table 10 , Table 19 and new High Bandwidth Memory (HBM) section. Added Cache Coherent Interconnect for Accelerators (CCIX) section. |
| 09/27/2016 | 2.9 | Updated Table 5 , Table 12 , Table 13 , and Table 14 . |
| 06/03/2016 | 2.8 | Added Zynq UltraScale+ MPSoC CG devices: Added Table 2 . Updated Table 11 , Table 12 , Table 21 , and Figure 5 . Created separate tables for EG and EV devices: Table 13 , Table 14 , Table 15 , and Table 16 . Updated Table 1 , Table 3 , Table 5 and notes, Table 6 and notes, Table 7 , Table 9 , Table 10 , Processing System Overview , and Processing System (PS) details. |
| 02/17/2016 | 2.7 | Added Migrating Devices . Updated Table 4 , Table 5 , Table 6 , Table 10 , Table 11 , Table 12 , and Figure 4 . |
| 12/15/2015 | 2.6 | Updated Table 1 , Table 5 , Table 6 , Table 9 , Table 12 , and Configuration . |
| 11/24/2015 | 2.5 | Updated Configuration, Encryption, and System Monitoring , Table 5 , Table 9 , Table 11 , and Table 21 . |
| 10/15/2015 | 2.4 | Updated Table 1 , Table 3 , Table 5 , Table 7 , Table 9 , and Table 11 with System Logic Cells. Updated Figure 3 . Updated Table 19 . |
| 09/29/2015 | 2.3 | Added A1156 to KU095 in Table 4 . Updated Table 5 . Updated Max. Distributed RAM in Table 9 . Updated Distributed RAM in Table 11 . Added Table 19 . Updated Table 21 . Updated Figure 3 . |
| 08/14/2015 | 2.2 | Updated Table 1 . Added XCKU025 to Table 3 , Table 4 , and Table 21 . Updated Table 7 , Table 9 , Table 11 , Table 12 , Table 18 . Updated System Monitor . Added voltage information to Table 21 . |
| 04/27/2015 | 2.1 | Updated Table 1 , Table 3 , Table 4 , Table 5 , Table 6 , Table 7 , Table 10 , Table 11 , Table 12 , Table 17 , I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken, Integrated Interface Blocks for PCI Express Designs , USB 3.0/2.0, Clock Management, System Monitor, and Figure 3 . |
| 02/23/2015 | 2.0 | UltraScale+ device information (Kintex UltraScale+ FPGA, Virtex UltraScale+ FPGA, and Zynq UltraScale+ MPSoC) added throughout document. |
| 12/16/2014 | 1.6 | Updated Table 1 ; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 3 , Table 7 ; Table 8 ; and Table 17 . |
| 11/17/2014 | 1.5 | Updated I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 1 ; Table 4 ; Table 7 ; Table 8 ; Table 17 ; Input/Output ; and Figure 3 . |
| 09/16/2014 | 1.4 | Updated Logic Cell information in Table 1 . Updated Table 3 ; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 7 ; Table 8 ; Integrated Block for 100G Ethernet ; and Figure 3 . |
| 05/20/2014 | 1.3 | Updated Table 8 . |
| 05/13/2014 | 1.2 | Added Ordering Information . Updated Table 1 , Clocks and Memory Interfaces , Table 3 , Table 7 (removed XCVU145; added XCVU190), Table 8 (removed XCVU145; removed FLVD1924 from XCVU160; added XCVU190; updated Table Notes), Table 17 , Integrated Interface Blocks for PCI Express Designs , and Integrated Block for Interlaken , and Memory Interfaces . |

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