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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |   |
|--------------------------------|---|
| Product Status                 | Active  |
| Number of LABs/CLBs            | 30300   |
| Number of Logic Elements/Cells | 530250  |
| Total RAM Bits                 | 21606000  |
| Number of I/O                  | 312   |
| Number of Gates                | -   |
| Voltage - Supply               | 0.922V ~ 0.979V   |
| Mounting Type                  | Surface Mount   |
| Operating Temperature          | -40°C ~ 100°C (TJ)  |
| Package / Case                 | 676-BBGA, FCBGA   |
| Supplier Device Package        | 676-FCBGA (27x27)   |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/xilinx/xcku040-2fbva676i">https://www.e-xfl.com/product-detail/xilinx/xcku040-2fbva676i</a> |

# Summary of Features

## Processing System Overview

UltraScale+ MPSoCs feature dual and quad core variants of the ARM Cortex-A53 (APU) with dual-core ARM Cortex-R5 (RPU) processing system (PS). Some devices also include a dedicated ARM Mali™-400 MP2 graphics processing unit (GPU). See [Table 2](#).

*Table 2: Zynq UltraScale+ MPSoC Device Features*

|     | CG Devices               | EG Devices               | EV Devices               |
|-----|--------------------------|--------------------------|--------------------------|
| APU | Dual-core ARM Cortex-A53 | Quad-core ARM Cortex-A53 | Quad-core ARM Cortex-A53 |
| RPU | Dual-core ARM Cortex-R5  | Dual-core ARM Cortex-R5  | Dual-core ARM Cortex-R5  |
| GPU | –                        | Mali-400MP2              | Mali-400MP2              |
| VCU | –                        | –                        | H.264/H.265              |

To support the processors' functionality, a number of peripherals with dedicated functions are included in the PS. For interfacing to external memories for data or configuration storage, the PS includes a multi-protocol dynamic memory controller, a DMA controller, a NAND controller, an SD/eMMC controller and a Quad SPI controller. In addition to interfacing to external memories, the APU also includes a Level-1 (L1) and Level-2 (L2) cache hierarchy; the RPU includes an L1 cache and Tightly Coupled memory subsystem. Each has access to a 256KB on-chip memory.

For high-speed interfacing, the PS includes 4 channels of transmit (TX) and receive (RX) pairs of transceivers, called PS-GTR transceivers, supporting data rates of up to 6.0Gb/s. These transceivers can interface to the high-speed peripheral blocks to support PCIe Gen2 root complex or end point in x1, x2, or x4 configurations; Serial-ATA (SATA) at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates; and up to two lanes of Display Port at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s data rates. The PS-GTR transceivers can also interface to components over USB 3.0 and Serial Gigabit Media Independent Interface (SGMII).

For general connectivity, the PS includes: a pair of USB 2.0 controllers, which can be configured as host, device, or On-The-Go (OTG); an I2C controller; a UART; and a CAN2.0B controller that conforms to ISO11898-1. There are also four triple speed Ethernet MACs and 128 bits of GPIO, of which 78 bits are available through the MIO and 96 through the EMIO.

High-bandwidth connectivity based on the ARM AMBA® AXI4 protocol connects the processing units with the peripherals and provides interface between the PS and the programmable logic (PL).

For additional information, go to: [DS891](#), *Zynq UltraScale+ MPSoC Overview*.

## I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken

Data is transported on and off chip through a combination of the high-performance parallel SelectIO™ interface and high-speed serial transceiver connectivity. I/O blocks provide support for cutting-edge memory interface and network protocols through flexible I/O standard and voltage support. The serial transceivers in the UltraScale architecture-based devices transfer data up to 32.75Gb/s, enabling 25G+ backplane designs with dramatically lower power per bit than previous generation transceivers. All transceivers, except the PS-GTR, support the required data rates for PCIe Gen3, and Gen4 (rev 0.5), and integrated blocks for PCIe enable UltraScale devices to support up to Gen4 x8 and Gen3 x16 Endpoint and Root Port designs. Integrated blocks for 150Gb/s Interlaken and 100Gb/s Ethernet (100G MAC/PCS) extend the capabilities of UltraScale devices, enabling simple, reliable support for Nx100G switch and bridge applications. Virtex UltraScale+ HBM devices include Cache Coherent Interconnect for Accelerators (CCIX) ports for coherently sharing data with different processors.

## Clocks and Memory Interfaces

UltraScale devices contain powerful clock management circuitry, including clock synthesis, buffering, and routing components that together provide a highly capable framework to meet design requirements. The clock network allows for extremely flexible distribution of clocks to minimize the skew, power consumption, and delay associated with clock signals. The clock management technology is tightly integrated with dedicated memory interface circuitry to enable support for high-performance external memories, including DDR4. In addition to parallel memory interfaces, UltraScale devices support serial memories, such as hybrid memory cube (HMC).

## Routing, SSI, Logic, Storage, and Signal Processing

Configurable Logic Blocks (CLBs) containing 6-input look-up tables (LUTs) and flip-flops, DSP slices with 27x18 multipliers, 36Kb block RAMs with built-in FIFO and ECC support, and 4Kx72 UltraRAM blocks (in UltraScale+ devices) are all connected with an abundance of high-performance, low-latency interconnect. In addition to logical functions, the CLB provides shift register, multiplexer, and carry logic functionality as well as the ability to configure the LUTs as distributed memory to complement the highly capable and configurable block RAMs. The DSP slice, with its 96-bit-wide XOR functionality, 27-bit pre-adder, and 30-bit A input, performs numerous independent functions including multiply accumulate, multiply add, and pattern detect. In addition to the device interconnect, in devices using SSI technology, signals can cross between super-logic regions (SLRs) using dedicated, low-latency interface tiles. These combined routing resources enable easy support for next-generation bus data widths. Virtex UltraScale+ HBM devices include up to 8GB of high bandwidth memory.

## Configuration, Encryption, and System Monitoring

The configuration and encryption block performs numerous device-level functions critical to the successful operation of the FPGA or MPSoC. This high-performance configuration block enables device configuration from external media through various protocols, including PCIe, often with no requirement to use multi-function I/O pins during configuration. The configuration block also provides 256-bit AES-GCM decryption capability at the same performance as unencrypted configuration. Additional features include SEU detection and correction, partial reconfiguration support, and battery-backed RAM or eFUSE technology for AES key storage to provide additional security. The System Monitor enables the monitoring of the physical environment via on-chip temperature and supply sensors and can also monitor up to 17 external analog inputs. With UltraScale+ MPSoCs, the device is booted via the Configuration and Security Unit (CSU), which supports secure boot via the 256-bit AES-GCM and SHA/384 blocks. The cryptographic engines in the CSU can be used in the MPSoC after boot for user encryption.

## Migrating Devices

UltraScale and UltraScale+ families provide footprint compatibility to enable users to migrate designs from one device or family to another. Any two packages with the same footprint identifier code are footprint compatible. For example, Kintex UltraScale devices in the A1156 packages are footprint compatible with Kintex UltraScale+ devices in the A1156 packages. Likewise, Virtex UltraScale devices in the B2104 packages are compatible with Virtex UltraScale+ devices and Kintex UltraScale devices in the B2104 packages. All valid device/package combinations are provided in the Device-Package Combinations and Maximum I/Os tables in this document. Refer to [UG583](#), *UltraScale Architecture PCB Design User Guide* for more detail on migrating between UltraScale and UltraScale+ devices and packages.

# Kintex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 6: Kintex UltraScale+ Device-Package Combinations and Maximum I/Os

| Package<br>(1)(2)(4) | Package<br>Dimensions<br>(mm) | KU3P               | KU5P               | KU9P               | KU11P              | KU13P              | KU15P              |
|----------------------|-------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
|                      |                               | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY |
| SFVB784(3)           | 23x23                         | 96, 208<br>0, 16   | 96, 208<br>0, 16   |                    |                    |                    |                    |
| FFVA676(3)           | 27x27                         | 48, 208<br>0, 16   | 48, 208<br>0, 16   |                    |                    |                    |                    |
| FFVB676              | 27x27                         | 72, 208<br>0, 16   | 72, 208<br>0, 16   |                    |                    |                    |                    |
| FFVD900(3)           | 31x31                         | 96, 208<br>0, 16   | 96, 208<br>0, 16   |                    | 96, 312<br>16, 0   |                    |                    |
| FFVE900              | 31x31                         |                    |                    | 96, 208<br>28, 0   |                    | 96, 208<br>28, 0   |                    |
| FFVA1156(3)          | 35x35                         |                    |                    |                    | 48, 416<br>20, 8   |                    | 48, 468<br>20, 8   |
| FFVE1517             | 40x40                         |                    |                    |                    | 96, 416<br>32, 20  |                    | 96, 416<br>32, 24  |
| FFVA1760             | 42.5x42.5                     |                    |                    |                    |                    |                    | 96, 416<br>44, 32  |
| FFVE1760             | 42.5x42.5                     |                    |                    |                    |                    |                    | 96, 572<br>32, 24  |

## Notes:

1. Go to [Ordering Information](#) for package designation details.
2. FF packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. GTY transceiver line rates are package limited: SFVB784 to 12.5Gb/s; FFVA676, FFVD900, and FFVA1156 to 16.3Gb/s.
4. Packages with the same last letter and number sequence, e.g., A676, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.

# Virtex UltraScale+ FPGA Feature Summary

Table 9: Virtex UltraScale+ FPGA Feature Summary

|   | VU3P    | VU5P      | VU7P      | VU9P      | VU11P     | VU13P     | VU31P   | VU33P   | VU35P     | VU37P     |
|---|---------|-----------|-----------|-----------|-----------|-----------|---------|---------|-----------|-----------|
| System Logic Cells                        | 862,050 | 1,313,763 | 1,724,100 | 2,586,150 | 2,835,000 | 3,780,000 | 961,800 | 961,800 | 1,906,800 | 2,851,800 |
| CLB Flip-Flops                            | 788,160 | 1,201,154 | 1,576,320 | 2,364,480 | 2,592,000 | 3,456,000 | 879,360 | 879,360 | 1,743,360 | 2,607,360 |
| CLB LUTs                                  | 394,080 | 600,577   | 788,160   | 1,182,240 | 1,296,000 | 1,728,000 | 439,680 | 439,680 | 871,680   | 1,303,680 |
| Max. Distributed RAM (Mb)                 | 12.0    | 18.3      | 24.1      | 36.1      | 36.2      | 48.3      | 12.5    | 12.5    | 24.6      | 36.7      |
| Block RAM Blocks                          | 720     | 1,024     | 1,440     | 2,160     | 2,016     | 2,688     | 672     | 672     | 1,344     | 2,016     |
| Block RAM (Mb)                            | 25.3    | 36.0      | 50.6      | 75.9      | 70.9      | 94.5      | 23.6    | 23.6    | 47.3      | 70.9      |
| UltraRAM Blocks                           | 320     | 470       | 640       | 960       | 960       | 1,280     | 320     | 320     | 640       | 960       |
| UltraRAM (Mb)                             | 90.0    | 132.2     | 180.0     | 270.0     | 270.0     | 360.0     | 90.0    | 90.0    | 180.0     | 270.0     |
| HBM DRAM (GB)                             | –       | –         | –         | –         | –         | –         | 4       | 8       | 8         | 8         |
| CMTs (1 MMCM and 2 PLLs)                  | 10      | 20        | 20        | 30        | 12        | 16        | 4       | 4       | 8         | 12        |
| Max. HP I/O <sup>(1)</sup>                | 520     | 832       | 832       | 832       | 624       | 832       | 208     | 208     | 416       | 624       |
| DSP Slices                                | 2,280   | 3,474     | 4,560     | 6,840     | 9,216     | 12,288    | 2,880   | 2,880   | 5,952     | 9,024     |
| System Monitor                            | 1       | 2         | 2         | 3         | 3         | 4         | 1       | 1       | 2         | 3         |
| GTY Transceivers 32.75Gb/s <sup>(2)</sup> | 40      | 80        | 80        | 120       | 96        | 128       | 32      | 32      | 64        | 96        |
| Transceiver Fractional PLLs               | 20      | 40        | 40        | 60        | 48        | 64        | 16      | 16      | 32        | 48        |
| PCIe Gen3 x16 and Gen4 x8                 | 2       | 4         | 4         | 6         | 3         | 4         | 4       | 4       | 5         | 6         |
| CCIX Ports <sup>(3)</sup>                 | –       | –         | –         | –         | –         | –         | 4       | 4       | 4         | 4         |
| 150G Interlaken                           | 3       | 4         | 6         | 9         | 6         | 8         | 0       | 0       | 2         | 4         |
| 100G Ethernet w/RS-FEC                    | 3       | 4         | 6         | 9         | 9         | 12        | 2       | 2       | 5         | 8         |

## Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s. See [Table 10](#).
3. A CCIX port requires the use of a PCIe Gen3 x16 / Gen4 x8 block.

# Zynq UltraScale+: CG Device Feature Summary

Table 11: Zynq UltraScale+: CG Device Feature Summary

|   | ZU2CG   | ZU3CG   | ZU4CG   | ZU5CG   | ZU6CG   | ZU7CG   | ZU9CG   |
|---|---|---------|---------|---------|---------|---------|---------|
| Application Processing Unit             | Dual-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache |         |         |         |         |         |         |
| Real-Time Processing Unit               | Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM                     |         |         |         |         |         |         |
| Embedded and External Memory            | 256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC                           |         |         |         |         |         |         |
| General Connectivity                    | 214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters                     |         |         |         |         |         |         |
| High-Speed Connectivity                 | 4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII   |         |         |         |         |         |         |
| System Logic Cells                      | 103,320   | 154,350 | 192,150 | 256,200 | 469,446 | 504,000 | 599,550 |
| CLB Flip-Flops                          | 94,464  | 141,120 | 175,680 | 234,240 | 429,208 | 460,800 | 548,160 |
| CLB LUTs                                | 47,232  | 70,560  | 87,840  | 117,120 | 214,604 | 230,400 | 274,080 |
| Distributed RAM (Mb)                    | 1.2   | 1.8     | 2.6     | 3.5     | 6.9     | 6.2     | 8.8     |
| Block RAM Blocks                        | 150   | 216     | 128     | 144     | 714     | 312     | 912     |
| Block RAM (Mb)                          | 5.3   | 7.6     | 4.5     | 5.1     | 25.1    | 11.0    | 32.1    |
| UltraRAM Blocks                         | 0   | 0       | 48      | 64      | 0       | 96      | 0       |
| UltraRAM (Mb)                           | 0   | 0       | 14.0    | 18.0    | 0       | 27.0    | 0       |
| DSP Slices                              | 240   | 360     | 728     | 1,248   | 1,973   | 1,728   | 2,520   |
| CMTs                                    | 3   | 3       | 4       | 4       | 4       | 8       | 4       |
| Max. HP I/O <sup>(1)</sup>              | 156   | 156     | 156     | 156     | 208     | 416     | 208     |
| Max. HD I/O <sup>(2)</sup>              | 96  | 96      | 96      | 96      | 120     | 48      | 120     |
| System Monitor                          | 2   | 2       | 2       | 2       | 2       | 2       | 2       |
| GTH Transceiver 16.3Gb/s <sup>(3)</sup> | 0   | 0       | 16      | 16      | 24      | 24      | 24      |
| GTY Transceivers 32.75Gb/s              | 0   | 0       | 0       | 0       | 0       | 0       | 0       |
| Transceiver Fractional PLLs             | 0   | 0       | 8       | 8       | 12      | 12      | 12      |
| PCIe Gen3 x16 and Gen4 x8               | 0   | 0       | 2       | 2       | 0       | 2       | 0       |
| 150G Interlaken                         | 0   | 0       | 0       | 0       | 0       | 0       | 0       |
| 100G Ethernet w/ RS-FEC                 | 0   | 0       | 0       | 0       | 0       | 0       | 0       |

## Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 12](#).

# Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

Table 14: Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

| Package<br>(1)(2)(3)(4)(5) | Package<br>Dimensions<br>(mm) | ZU2EG              | ZU3EG              | ZU4EG              | ZU5EG              | ZU6EG              | ZU7EG              | ZU9EG              | ZU11EG             | ZU15EG             | ZU17EG             | ZU19EG             |
|----------------------------|-------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
|                            |                               | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY |
| SBVA484(6)                 | 19x19                         | 24, 58<br>0, 0     | 24, 58<br>0, 0     |                    |                    |                    |                    |                    |                    |                    |                    |                    |
| SFVA625                    | 21x21                         | 24, 156<br>0, 0    | 24, 156<br>0, 0    |                    |                    |                    |                    |                    |                    |                    |                    |                    |
| SFVC784(7)                 | 23x23                         | 96, 156<br>0, 0    | 96, 156<br>0, 0    | 96, 156<br>4, 0    | 96, 156<br>4, 0    |                    |                    |                    |                    |                    |                    |                    |
| FBVB900                    | 31x31                         |                    |                    | 48, 156<br>16, 0   | 48, 156<br>16, 0   |                    | 48, 156<br>16, 0   |                    |                    |                    |                    |                    |
| FFVC900                    | 31x31                         |                    |                    |                    |                    | 48, 156<br>16, 0   |                    | 48, 156<br>16, 0   |                    | 48, 156<br>16, 0   |                    |                    |
| FFVB1156                   | 35x35                         |                    |                    |                    |                    | 120, 208<br>24, 0  |                    | 120, 208<br>24, 0  |                    | 120, 208<br>24, 0  |                    |                    |
| FFVC1156                   | 35x35                         |                    |                    |                    |                    |                    | 48, 312<br>20, 0   |                    | 48, 312<br>20, 0   |                    |                    |                    |
| FFVB1517                   | 40x40                         |                    |                    |                    |                    |                    |                    |                    | 72, 416<br>16, 0   |                    | 72, 572<br>16, 0   | 72, 572<br>16, 0   |
| FFVF1517                   | 40x40                         |                    |                    |                    |                    |                    | 48, 416<br>24, 0   |                    | 48, 416<br>32, 0   |                    |                    |                    |
| FFVC1760                   | 42.5x42.5                     |                    |                    |                    |                    |                    |                    |                    | 96, 416<br>32, 16  |                    | 96, 416<br>32, 16  | 96, 416<br>32, 16  |
| FFVD1760                   | 42.5x42.5                     |                    |                    |                    |                    |                    |                    |                    |                    |                    | 48, 260<br>44, 28  | 48, 260<br>44, 28  |
| FFVE1924                   | 45x45                         |                    |                    |                    |                    |                    |                    |                    |                    |                    | 96, 572<br>44, 0   | 96, 572<br>44, 0   |

## Notes:

- Go to [Ordering Information](#) for package designation details.
- FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
- All device package combinations bond out 4 PS-GTR transceivers.
- All device package combinations bond out 214 PS I/O except ZU2EG and ZU3EG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
- Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
- All 58 HP I/O pins are powered by the same V<sub>CCO</sub> supply.
- GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.



contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. Figure 2 is a representation of an FPGA divided into regions.



Figure 2: Column-Based FPGA Divided into Clock Regions

## Processing System (PS)

Zynq UltraScale+ MPSoCs consist of a PS coupled with programmable logic. The contents of the PS varies between the different Zynq UltraScale+ devices. All devices contain an APU, an RPU, and many peripherals for connecting the multiple processing engines to external components. The EG and EV devices contain a GPU and the EV devices contain a video codec unit (VCU). The components of the PS are connected together and to the PL through a multi-layered ARM AMBA AXI non-blocking interconnect that supports multiple simultaneous master-slave transactions. Traffic through the interconnect can be regulated by the quality of service (QoS) block in the interconnect. Twelve dedicated AXI 32-bit, 64-bit, or 128-bit ports connect the PL to high-speed interconnect and DDR in the PS via a FIFO interface.

There are four independently controllable power domains: the PL plus three within the PS (full power, lower power, and battery power domains). Additionally, many peripherals support clock gating and power gating to further reduce dynamic and static power consumption.

## Application Processing Unit (APU)

The APU has a feature-rich dual-core or quad-core ARM Cortex-A53 processor. Cortex-A53 cores are 32-bit/64-bit application processors based on ARM-v8A architecture, offering the best performance-to-power ratio. The ARMv8 architecture supports hardware virtualization. Each of the Cortex-A53 cores has: 32KB of instruction and data L1 caches, with parity and ECC protection respectively; a NEON SIMD engine; and a single and double precision floating point unit. In addition to these blocks, the APU consists of a snoop control unit and a 1MB L2 cache with ECC protection to enhance system-level performance. The snoop control unit keeps the L1 caches coherent thus eliminating the need of spending software bandwidth for coherency. The APU also has a built-in interrupt controller supporting virtual interrupts. The APU communicates to the rest of the PS through 128-bit AXI coherent extension (ACE) port via Cache Coherent Interconnect (CCI) block, using the System Memory Management Unit (SMMU). The APU is also connected to the Programmable Logic (PL), through the 128-bit accelerator coherency port

(ACP), providing a low latency coherent port for accelerators in the PL. To support real-time debug and trace, each core also has an Embedded Trace Macrocell (ETM) that communicates with the ARM CoreSight™ Debug System.

## Real-Time Processing Unit (RPU)

The RPU in the PS contains a dual-core ARM Cortex-R5 PS. Cortex-R5 cores are 32-bit real-time processor cores based on ARM-v7R architecture. Each of the Cortex-R5 cores has 32KB of level-1 (L1) instruction and data cache with ECC protection. In addition to the L1 caches, each of the Cortex-R5 cores also has a 128KB tightly coupled memory (TCM) interface for real-time single cycle access. The RPU also has a dedicated interrupt controller. The RPU can operate in either split or lock-step mode. In split mode, both processors run independently of each other. In lock-step mode, they run in parallel with each other, with integrated comparator logic, and the TCMs are used as 256KB unified memory. The RPU communicates with the rest of the PS via the 128-bit AXI-4 ports connected to the low power domain switch. It also communicates directly with the PL through 128-bit low latency AXI-4 ports. To support real-time debug and trace each core also has an embedded trace macrocell (ETM) that communicates with the ARM CoreSight Debug System.

## External Memory

The PS can interface to many types of external memories through dedicated memory controllers. The dynamic memory controller supports DDR3, DDR3L, DDR4, LPDDR3, and LPDDR4 memories. The multi-protocol DDR memory controller can be configured to access a 2GB address space in 32-bit addressing mode and up to 32GB in 64-bit addressing mode using a single or dual rank configuration of 8-bit, 16-bit, or 32-bit DRAM memories. Both 32-bit and 64-bit bus access modes are protected by ECC using extra bits.

The SD/eMMC controller supports 1 and 4 bit data interfaces at low, default, high-speed, and ultra-high-speed (UHS) clock rates. This controller also supports 1-, 4-, or 8-bit-wide eMMC interfaces that are compliant to the eMMC 4.51 specification. eMMC is one of the primary boot and configuration modes for Zynq UltraScale+ MPSoCs and supports boot from managed NAND devices. The controller has a built-in DMA for enhanced performance.

The Quad-SPI controller is one of the primary boot and configuration devices. It supports 4-byte and 3-byte addressing modes. In both addressing modes, single, dual-stacked, and dual-parallel configurations are supported. Single mode supports a quad serial NOR flash memory, while in double stacked and double parallel modes, it supports two quad serial NOR flash memories.

The NAND controller is based on ONFI3.1 specification. It has an 8-pin interface and provides 200Mb/s of bandwidth in synchronous mode. It supports 24 bits of ECC thus enabling support for SLC NAND memories. It has two chip-selects to support deeper memory and a built-in DMA for enhanced performance.

## General Connectivity

There are many peripherals in the PS for connecting to external devices over industry standard protocols, including CAN2.0B, USB, Ethernet, I2C, and UART. Many of the peripherals support clock gating and power gating modes to reduce dynamic and static power consumption.

### **USB 3.0/2.0**

The pair of USB controllers can be configured as host, device, or On-The-Go (OTG). The core is compliant to USB 3.0 specification and supports super, high, full, and low speed modes in all configurations. In host mode, the USB controller is compliant with the Intel XHCI specification. In device mode, it supports up to 12 end points. While operating in USB 3.0 mode, the controller uses the serial transceiver and operates up to 5.0Gb/s. In USB 2.0 mode, the Universal Low Peripheral Interface (ULPI) is used to connect the controller to an external PHY operating up to 480Mb/s. The ULPI is also connected in USB 3.0 mode to support high-speed operations.

### **Ethernet MAC**

The four tri-speed ethernet MACs support 10Mb/s, 100Mb/s, and 1Gb/s operations. The MACs support jumbo frames and time stamping through the interfaces based on IEEE Std 1588v2. The ethernet MACs can be connected through the serial transceivers (SGMII), the MIO (RGMII), or through EMIO (GMII). The GMII interface can be converted to a different interface within the PL.

## High-Speed Connectivity

The PS includes four PS-GTR transceivers (transmit and receive), supporting data rates up to 6.0Gb/s and can interface to the peripherals for communication over PCIe, SATA, USB 3.0, SGMII, and DisplayPort.

### **PCIe**

The integrated block for PCIe is compliant with PCI Express base specification 2.1 and supports x1, x2, and x4 configurations as root complex or end point, compliant to transaction ordering rules in both configurations. It has built-in DMA, supports one virtual channel and provides fully configurable base address registers.

### **SATA**

Users can connect up to two external devices using the two SATA host port interfaces compliant to the SATA 3.1 specification. The SATA interfaces can operate at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates and are compliant with advanced host controller interface (AHCI) version 1.3 supporting partial and slumber power modes.

### **DisplayPort**

The DisplayPort controller supports up to two lanes of source-only DisplayPort compliant with VESA DisplayPort v1.2a specification (source only) at 1.62Gb/s, 2.7Gb/s, and 5.4Gb/s data rates. The controller supports single stream transport (SST); video resolution up to 4Kx2K at a 30Hz frame rate; video formats Y-only, YCbCr444, YCbCr422, YCbCr420, RGB, YUV444, YUV422, xvYCC, and pixel color depth of 6, 8, 10, and 12 bits per color component.

## I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards  $V_{CCO}$  or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a  $100\Omega$  internal resistor. All UltraScale devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. UltraScale+ families add support for MIPI with a dedicated D-PHY in the I/O bank.

### ***3-State Digitally Controlled Impedance and Low Power I/O Features***

The 3-state Digitally Controlled Impedance (T\_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to  $V_{CCO}$  or split (Thevenin) termination to  $V_{CCO}/2$ . This allows users to eliminate off-chip termination for signals using T\_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

## I/O Logic

### ***Input and Output Delay***

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

### ***ISERDES and OSERDES***

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

## Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

## Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally “auto-adapt” to automatically learn and compensate for different interconnect characteristics. This enables even more margin for 10G+ and 25G+ backplanes.

## Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

The MMCM can have a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of 1/8 and can thus increase frequency synthesis capabilities by a factor of 8. The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency. At 1,600MHz, the phase-shift timing increment is 11.2ps.

## PLL

With fewer features than the MMCM, the two PLLs in a clock management tile are primarily present to provide the necessary clocks to the dedicated memory interface circuitry. The circuit at the center of the PLLs is similar to the MMCM, with PFD feeding a VCO and programmable M, D, and O counters. There are two divided outputs to the device fabric per PLL as well as one clock plus one enable signal to the memory interface circuitry.

UltraScale+ MPSoCs are equipped with five additional PLLs in the PS for independently configuring the four primary clock domains with the PS: the APU, the RPU, the DDR controller, and the I/O peripherals.

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## Clock Distribution

Clocks are distributed throughout UltraScale devices via buffers that drive a number of vertical and horizontal tracks. There are 24 horizontal clock routes per clock region and 24 vertical clock routes per clock region with 24 additional vertical clock routes adjacent to the MMCM and PLL. Within a clock region, clock signals are routed to the device logic (CLBs, etc.) via 16 gateable leaf clocks.

Several types of clock buffers are available. The BUFGCE and BUFCE\_LEAF buffers provide clock gating at the global and leaf levels, respectively. BUFGCTRL provides glitchless clock muxing and gating capability. BUFGCE\_DIV has clock gating capability and can divide a clock by 1 to 8. BUFG\_GT performs clock division from 1 to 8 for the transceiver clocks. In MPSoCs, clocks can be transferred from the PS to the PL using dedicated buffers.

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## Memory Interfaces

Memory interface data rates continue to increase, driving the need for dedicated circuitry that enables high performance, reliable interfacing to current and next-generation memory technologies. Every UltraScale device includes dedicated physical interfaces (PHY) blocks located between the CMT and I/O columns that support implementation of high-performance PHY blocks to external memories such as DDR4, DDR3, QDRII+, and RLDRAM3. The PHY blocks in each I/O bank generate the address/control and data bus signaling protocols as well as the precision clock/data alignment required to reliably communicate with a variety of high-performance memory standards. Multiple I/O banks can be used to create wider memory interfaces.

As well as external parallel memory interfaces, UltraScale FPGAs and MPSoCs can communicate to external serial memories, such as Hybrid Memory Cube (HMC), via the high-speed serial transceivers. All transceivers in the UltraScale architecture support the HMC protocol, up to 15Gb/s line rates. UltraScale devices support the highest bandwidth HMC configuration of 64 lanes with a single FPGA.

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## UltraRAM

UltraRAM is a high-density, dual-port, synchronous memory block available in UltraScale+ devices. Both of the ports share the same clock and can address all of the 4K x 72 bits. Each port can independently read from or write to the memory array. UltraRAM supports two types of write enable schemes. The first mode is consistent with the block RAM byte write enable mode. The second mode allows gating the data and parity byte writes separately. UltraRAM blocks can be connected together to create larger memory arrays. Dedicated routing in the UltraRAM column enables the entire column height to be connected together. If additional density is required, all the UltraRAM columns in an SLR can be connected together with a few fabric resources to create single instances of RAM approximately 100Mb in size. This makes UltraRAM an ideal solution for replacing external memories such as SRAM. Cascadable anywhere from 288Kb to 100Mb, UltraRAM provides the flexibility to fulfill many different memory requirements.

## Error Detection and Correction

Each 64-bit-wide UltraRAM can generate, store and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process.

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## High Bandwidth Memory (HBM)

Virtex UltraScale+ HBM devices incorporate 4GB HBM stacks adjacent to the FPGA die. Using stacked silicon interconnect technology, the FPGA communicates to the HBM stacks through memory controllers that connect to dedicated low-inductance interconnect in the silicon interposer. Each Virtex UltraScale+ HBM FPGA contains one or two HBM stacks, resulting in up to 8GB of HBM per FPGA.

The FPGA has 32 HBM AXI interfaces used to communicate with the HBM. Through a built-in switch mechanism, any of the 32 HBM AXI interfaces can access any memory address on either one or both of the HBM stacks due to the flexible addressing feature. This flexible connection between the FPGA and the HBM stacks results in easy floorplanning and timing closure. The memory controllers perform read and write reordering to improve bus efficiency. Data integrity is ensured through error checking and correction (ECC) circuitry.

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## Configurable Logic Block

Every Configurable Logic Block (CLB) in the UltraScale architecture contains 8 LUTs and 16 flip-flops. The LUTs can be configured as either one 6-input LUT with one output, or as two 5-input LUTs with separate outputs but common inputs. Each LUT can optionally be registered in a flip-flop. In addition to the LUTs and flip-flops, the CLB contains arithmetic carry logic and multiplexers to create wider logic functions.

Each CLB contains one slice. There are two types of slices: SLICEL and SLICEM. LUTs in the SLICEM can be configured as 64-bit RAM, as 32-bit shift registers (SRL32), or as two SRL16s. CLBs in the UltraScale architecture have increased routing and connectivity compared to CLBs in previous-generation Xilinx devices. They also have additional control signals to enable superior register packing, resulting in overall higher device utilization.



Zynq UltraScale+ MPSoCs contain an additional System Monitor block in the PS. See [Table 20](#).

**Table 20: Key System Monitor Features**

|            | <b>Kintex UltraScale<br/>Virtex UltraScale</b> | <b>Kintex UltraScale+<br/>Virtex UltraScale+<br/>Zynq UltraScale+ MPSoC PL</b> | <b>Zynq UltraScale+ MPSoC PS</b> |
|------------|--|--|----------------------------------|
| ADC        | 10-bit 200kSPS                                 | 10-bit 200kSPS   | 10-bit 1MSPS                     |
| Interfaces | JTAG, I2C, DRP                                 | JTAG, I2C, DRP, PMBus  | APB                              |

In FPGAs and the MPSoC PL, sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, PMBus, or I2C interfaces. The I2C interface and PMBus allow the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

The System Monitor in the MPSoC PS uses a 10-bit, 1 mega-sample-per-second (MSPS) ADC to digitize the sensor outputs. The measurements are stored in registers and are accessed via the Advanced Peripheral Bus (APB) interface by the processors and the platform management unit (PMU) in the PS.

## Configuration

The UltraScale architecture-based devices store their customized configuration in SRAM-type internal latches. The configuration storage is volatile and must be reloaded whenever the device is powered up. This storage can also be reloaded at any time. Several methods and data formats for loading configuration are available, determined by the mode pins, with more dedicated configuration datapath pins to simplify the configuration process.

UltraScale architecture-based devices support secure and non-secure boot with optional Advanced Encryption Standard - Galois/Counter Mode (AES-GCM) decryption and authentication logic. If only authentication is required, the UltraScale architecture provides an alternative form of authentication in the form of RSA algorithms. For RSA authentication support in the Kintex UltraScale and Virtex UltraScale families, go to [UG570](#), *UltraScale Architecture Configuration User Guide*.

UltraScale architecture-based devices also have the ability to select between multiple configurations, and support robust field-update methodologies. This is especially useful for updates to a design after the end product has been shipped. Designers can release their product with an early version of the design, thus getting their product to market faster. This feature allows designers to keep their customers current with the most up-to-date design while the product is already deployed in the field.

## Booting MPSoCs

Zynq UltraScale+ MPSoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the AES-GCM, SHA-3/384 decryption/authentication, and 4096-bit RSA blocks decrypt and authenticate the image.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NAND, Quad-SPI, SD, eMMC, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. One of the CPUs, Cortex-A53 or Cortex-R5, executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip memory (OCM).



After copying the FSBL to OCM, the processor executes the FSBL. Xilinx supplies example FSBLs or users can create their own. The FSBL initiates the boot of the PS and can load and configure the PL, or configuration of the PL can be deferred to a later stage. The FSBL typically loads either a user application or an optional second stage boot loader (SSBL) such as U-Boot. Users obtain example SSBL from Xilinx or a third party, or they can create their own SSBL. The SSBL continues the boot process by loading code from any of the primary boot devices or from other sources such as USB, Ethernet, etc. If the FSBL did not configure the PL, the SSBL can do so, or again, the configuration can be deferred to a later stage.

The static memory interface controller (NAND, eMMC, or Quad-SPI) is configured using default settings. To improve device configuration speed, these settings can be modified by information provided in the boot image header. The ROM boot image is not user readable or executable after boot.

## Configuring FPGAs

The SPI (serial NOR) interface (x1, x2, x4, and dual x4 modes) and the BPI (parallel NOR) interface (x8 and x16 modes) are two common methods used for configuring the FPGA. Users can directly connect an SPI or BPI flash to the FPGA, and the FPGA's internal configuration logic reads the bitstream out of the flash and configures itself, eliminating the need for an external controller. The FPGA automatically detects the bus width on the fly, eliminating the need for any external controls or switches. Bus widths supported are x1, x2, x4, and dual x4 for SPI, and x8 and x16 for BPI. The larger bus widths increase configuration speed and reduce the amount of time it takes for the FPGA to start up after power-on.

In master mode, the FPGA can drive the configuration clock from an internally generated clock, or for higher speed configuration, the FPGA can use an external configuration clock source. This allows high-speed configuration with the ease of use characteristic of master mode. Slave modes up to 32 bits wide that are especially useful for processor-driven configuration are also supported by the FPGA. In addition, the new media configuration access port (MCAP) provides a direct connection between the integrated block for PCIe and the configuration logic to simplify configuration over PCIe.

SEU detection and mitigation (SEM) IP, RSA authentication, post-configuration CRC, and Security Monitor (SecMon) IP are not supported in the KU025 FPGA.

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## Packaging

The UltraScale devices are available in a variety of organic flip-chip and lidless flip-chip packages supporting different quantities of I/Os and transceivers. Maximum supported performance can depend on the style of package and its material. Always refer to the specific device data sheet for performance specifications by package type.

In flip-chip packages, the silicon device is attached to the package substrate using a high-performance flip-chip process. Decoupling capacitors are mounted on the package substrate to optimize signal integrity under simultaneous switching of outputs (SSO) conditions.

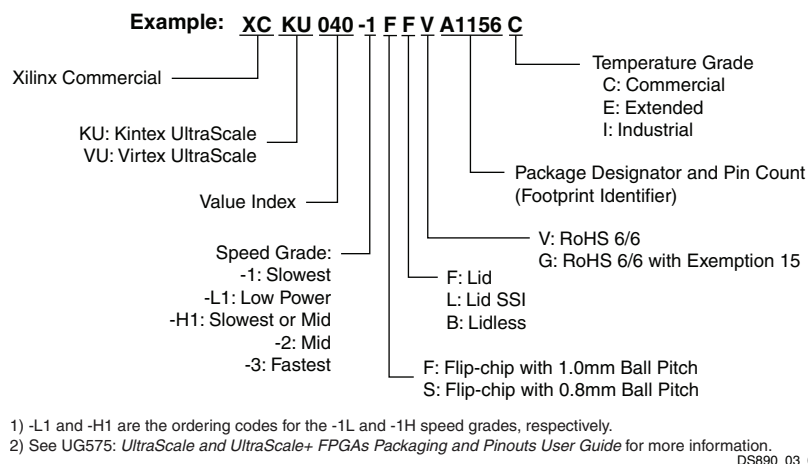
Table 21: Speed Grade and Temperature Grade (Cont'd)

| Device Family    | Devices   | Speed Grade and Temperature Grade |               |   |                                      |
|------------------|---|-----------------------------------|---------------|---|--------------------------------------|
|                  |   | Commercial (C)                    | Extended (E)  |   | Industrial (I)                       |
|                  |   | 0°C to +85°C                      | 0°C to +100°C | 0°C to +110°C                           | –40°C to +100°C                      |
| Zynq UltraScale+ | CG Devices  |                                   | -2E (0.85V)   |   | -2I (0.85V)                          |
|                  |   |                                   |               | -2LE <sup>(2)(3)</sup> (0.85V or 0.72V) |                                      |
|                  |   |                                   | -1E (0.85V)   |   | -1I (0.85V)                          |
|                  |   |                                   |               |   | -1LI <sup>(3)</sup> (0.85V or 0.72V) |
|                  | ZU2EG<br>ZU3EG  |                                   | -2E (0.85V)   |   | -2I (0.85V)                          |
|                  |   |                                   |               | -2LE <sup>(2)(3)</sup> (0.85V or 0.72V) |                                      |
|                  |   |                                   | -1E (0.85V)   |   | -1I (0.85V)                          |
|                  |   |                                   |               |   | -1LI <sup>(3)</sup> (0.85V or 0.72V) |
|                  | ZU4EG<br>ZU5EG<br>ZU6EG<br>ZU7EG<br>ZU9EG<br>ZU11EG<br>ZU15EG<br>ZU17EG<br>ZU19EG |                                   | -3E (0.90V)   |   |                                      |
|                  |   |                                   | -2E (0.85V)   |   | -2I (0.85V)                          |
|                  |   |                                   |               | -2LE <sup>(2)(3)</sup> (0.85V or 0.72V) |                                      |
|                  |   |                                   | -1E (0.85V)   |   | -1I (0.85V)                          |
|                  |   |                                   |               |   | -1LI <sup>(3)</sup> (0.85V or 0.72V) |
|                  |   |                                   |               |   |                                      |
|                  |   |                                   |               |   |                                      |
|                  |   |                                   |               |   |                                      |
|                  | EV Devices  |                                   | -3E (0.90V)   |   |                                      |
|                  |   |                                   | -2E (0.85V)   |   | -2I (0.85V)                          |
|                  |   |                                   |               | -2LE <sup>(2)(3)</sup> (0.85V or 0.72V) |                                      |
|                  |   |                                   | -1E (0.85V)   |   | -1I (0.85V)                          |
|                  |   |                                   |               |   | -1LI <sup>(3)</sup> (0.85V or 0.72V) |

**Notes:**

1. KU025 and KU095 are not available in -3E or -1LI speed/temperature grades.
2. In -2LE speed/temperature grade, devices can operate for a limited time with junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal at 0.85V or low voltage at 0.72V). Operation at 110°C Tj is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of device lifetime.
3. In Zynq UltraScale+ MPSoCs, when operating the PL at low voltage (0.72V), the PS operates at nominal voltage (0.85V).

The ordering information shown in [Figure 3](#) applies to all packages in the Kintex UltraScale and Virtex UltraScale FPGAs. Refer to the Package Marking section of [UG575, UltraScale and UltraScale+ FPGAs Packaging and Pinouts User Guide](#) for a more detailed explanation of the device markings.



**Figure 3: Kintex UltraScale and Virtex UltraScale FPGA Ordering Information**

# Revision History

The following table shows the revision history for this document:

| Date       | Version | Description of Revisions   |
|------------|---------|--|
| 02/15/2017 | 2.11    | Updated <a href="#">Table 1</a> , <a href="#">Table 9</a> : Converted HBM from Gb to GB. Updated <a href="#">Table 11</a> , <a href="#">Table 13</a> , and <a href="#">Table 15</a> : Updated DSP count for Zynq UltraScale+ MPSoCs. Updated <a href="#">Cache Coherent Interconnect for Accelerators (CCIX)</a> . Updated <a href="#">High Bandwidth Memory (HBM)</a> . Updated <a href="#">Table 21</a> : Added -2E speed grade to all UltraScale+ devices. Removed -3E from XCZU2 and XCZU3.  |
| 11/09/2016 | 2.10    | Updated <a href="#">Table 1</a> . Added HBM devices to <a href="#">Table 9</a> , <a href="#">Table 10</a> , <a href="#">Table 19</a> and new <a href="#">High Bandwidth Memory (HBM)</a> section. Added <a href="#">Cache Coherent Interconnect for Accelerators (CCIX)</a> section.   |
| 09/27/2016 | 2.9     | Updated <a href="#">Table 5</a> , <a href="#">Table 12</a> , <a href="#">Table 13</a> , and <a href="#">Table 14</a> .   |
| 06/03/2016 | 2.8     | Added Zynq UltraScale+ MPSoC CG devices: Added <a href="#">Table 2</a> . Updated <a href="#">Table 11</a> , <a href="#">Table 12</a> , <a href="#">Table 21</a> , and <a href="#">Figure 5</a> . Created separate tables for EG and EV devices: <a href="#">Table 13</a> , <a href="#">Table 14</a> , <a href="#">Table 15</a> , and <a href="#">Table 16</a> .<br>Updated <a href="#">Table 1</a> , <a href="#">Table 3</a> , <a href="#">Table 5</a> and notes, <a href="#">Table 6</a> and notes, <a href="#">Table 7</a> , <a href="#">Table 9</a> , <a href="#">Table 10</a> , <a href="#">Processing System Overview</a> , and <a href="#">Processing System (PS)</a> details. |
| 02/17/2016 | 2.7     | Added <a href="#">Migrating Devices</a> . Updated <a href="#">Table 4</a> , <a href="#">Table 5</a> , <a href="#">Table 6</a> , <a href="#">Table 10</a> , <a href="#">Table 11</a> , <a href="#">Table 12</a> , and <a href="#">Figure 4</a> .  |
| 12/15/2015 | 2.6     | Updated <a href="#">Table 1</a> , <a href="#">Table 5</a> , <a href="#">Table 6</a> , <a href="#">Table 9</a> , <a href="#">Table 12</a> , and <a href="#">Configuration</a> .   |
| 11/24/2015 | 2.5     | Updated <a href="#">Configuration, Encryption, and System Monitoring</a> , <a href="#">Table 5</a> , <a href="#">Table 9</a> , <a href="#">Table 11</a> , and <a href="#">Table 21</a> .   |
| 10/15/2015 | 2.4     | Updated <a href="#">Table 1</a> , <a href="#">Table 3</a> , <a href="#">Table 5</a> , <a href="#">Table 7</a> , <a href="#">Table 9</a> , and <a href="#">Table 11</a> with System Logic Cells. Updated <a href="#">Figure 3</a> . Updated <a href="#">Table 19</a> .  |
| 09/29/2015 | 2.3     | Added A1156 to KU095 in <a href="#">Table 4</a> . Updated <a href="#">Table 5</a> . Updated Max. Distributed RAM in <a href="#">Table 9</a> . Updated Distributed RAM in <a href="#">Table 11</a> . Added <a href="#">Table 19</a> . Updated <a href="#">Table 21</a> . Updated <a href="#">Figure 3</a> .   |
| 08/14/2015 | 2.2     | Updated <a href="#">Table 1</a> . Added XCKU025 to <a href="#">Table 3</a> , <a href="#">Table 4</a> , and <a href="#">Table 21</a> . Updated <a href="#">Table 7</a> , <a href="#">Table 9</a> , <a href="#">Table 11</a> , <a href="#">Table 12</a> , <a href="#">Table 18</a> . Updated <a href="#">System Monitor</a> . Added voltage information to <a href="#">Table 21</a> .  |
| 04/27/2015 | 2.1     | Updated <a href="#">Table 1</a> , <a href="#">Table 3</a> , <a href="#">Table 4</a> , <a href="#">Table 5</a> , <a href="#">Table 6</a> , <a href="#">Table 7</a> , <a href="#">Table 10</a> , <a href="#">Table 11</a> , <a href="#">Table 12</a> , <a href="#">Table 17</a> , I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken, <a href="#">Integrated Interface Blocks for PCI Express Designs</a> , USB 3.0/2.0, Clock Management, System Monitor, and <a href="#">Figure 3</a> .  |
| 02/23/2015 | 2.0     | UltraScale+ device information (Kintex UltraScale+ FPGA, Virtex UltraScale+ FPGA, and Zynq UltraScale+ MPSoC) added throughout document.   |
| 12/16/2014 | 1.6     | Updated <a href="#">Table 1</a> ; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; <a href="#">Table 3</a> , <a href="#">Table 7</a> ; <a href="#">Table 8</a> ; and <a href="#">Table 17</a> .   |
| 11/17/2014 | 1.5     | Updated I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; <a href="#">Table 1</a> ; <a href="#">Table 4</a> ; <a href="#">Table 7</a> ; <a href="#">Table 8</a> ; <a href="#">Table 17</a> ; <a href="#">Input/Output</a> ; and <a href="#">Figure 3</a> .   |
| 09/16/2014 | 1.4     | Updated Logic Cell information in <a href="#">Table 1</a> . Updated <a href="#">Table 3</a> ; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; <a href="#">Table 7</a> ; <a href="#">Table 8</a> ; <a href="#">Integrated Block for 100G Ethernet</a> ; and <a href="#">Figure 3</a> .  |
| 05/20/2014 | 1.3     | Updated <a href="#">Table 8</a> .  |
| 05/13/2014 | 1.2     | Added <a href="#">Ordering Information</a> . Updated <a href="#">Table 1</a> , <a href="#">Clocks and Memory Interfaces</a> , <a href="#">Table 3</a> , <a href="#">Table 7</a> (removed XCVU145; added XCVU190), <a href="#">Table 8</a> (removed XCVU145; removed FLVD1924 from XCVU160; added XCVU190; updated Table Notes), <a href="#">Table 17</a> , <a href="#">Integrated Interface Blocks for PCI Express Designs</a> , and <a href="#">Integrated Block for Interlaken</a> , and <a href="#">Memory Interfaces</a> .   |

| <b>Date</b> | <b>Version</b> | <b>Description of Revisions</b>   |
|-------------|----------------|---|
| 02/06/2014  | 1.1            | Updated PCIe information in <a href="#">Table 1</a> and <a href="#">Table 3</a> . Added FFVJ1924 package to <a href="#">Table 8</a> . |
| 12/10/2013  | 1.0            | Initial Xilinx release.   |