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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	30300
Number of Logic Elements/Cells	530250
Total RAM Bits	21606000
Number of I/O	468
Number of Gates	-
Voltage - Supply	0.922V ~ 0.979V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA, FCBGA
Supplier Device Package	900-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcku040-2fbva900i

Summary of Features

Processing System Overview

UltraScale+ MPSoCs feature dual and quad core variants of the ARM Cortex-A53 (APU) with dual-core ARM Cortex-R5 (RPU) processing system (PS). Some devices also include a dedicated ARM Mali™-400 MP2 graphics processing unit (GPU). See [Table 2](#).

Table 2: Zynq UltraScale+ MPSoC Device Features

	CG Devices	EG Devices	EV Devices
APU	Dual-core ARM Cortex-A53	Quad-core ARM Cortex-A53	Quad-core ARM Cortex-A53
RPU	Dual-core ARM Cortex-R5	Dual-core ARM Cortex-R5	Dual-core ARM Cortex-R5
GPU	–	Mali-400MP2	Mali-400MP2
VCU	–	–	H.264/H.265

To support the processors' functionality, a number of peripherals with dedicated functions are included in the PS. For interfacing to external memories for data or configuration storage, the PS includes a multi-protocol dynamic memory controller, a DMA controller, a NAND controller, an SD/eMMC controller and a Quad SPI controller. In addition to interfacing to external memories, the APU also includes a Level-1 (L1) and Level-2 (L2) cache hierarchy; the RPU includes an L1 cache and Tightly Coupled memory subsystem. Each has access to a 256KB on-chip memory.

For high-speed interfacing, the PS includes 4 channels of transmit (TX) and receive (RX) pairs of transceivers, called PS-GTR transceivers, supporting data rates of up to 6.0Gb/s. These transceivers can interface to the high-speed peripheral blocks to support PCIe Gen2 root complex or end point in x1, x2, or x4 configurations; Serial-ATA (SATA) at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates; and up to two lanes of Display Port at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s data rates. The PS-GTR transceivers can also interface to components over USB 3.0 and Serial Gigabit Media Independent Interface (SGMII).

For general connectivity, the PS includes: a pair of USB 2.0 controllers, which can be configured as host, device, or On-The-Go (OTG); an I2C controller; a UART; and a CAN2.0B controller that conforms to ISO11898-1. There are also four triple speed Ethernet MACs and 128 bits of GPIO, of which 78 bits are available through the MIO and 96 through the EMIO.

High-bandwidth connectivity based on the ARM AMBA® AXI4 protocol connects the processing units with the peripherals and provides interface between the PS and the programmable logic (PL).

For additional information, go to: [DS891](#), *Zynq UltraScale+ MPSoC Overview*.

Migrating Devices

UltraScale and UltraScale+ families provide footprint compatibility to enable users to migrate designs from one device or family to another. Any two packages with the same footprint identifier code are footprint compatible. For example, Kintex UltraScale devices in the A1156 packages are footprint compatible with Kintex UltraScale+ devices in the A1156 packages. Likewise, Virtex UltraScale devices in the B2104 packages are compatible with Virtex UltraScale+ devices and Kintex UltraScale devices in the B2104 packages. All valid device/package combinations are provided in the Device-Package Combinations and Maximum I/Os tables in this document. Refer to [UG583](#), *UltraScale Architecture PCB Design User Guide* for more detail on migrating between UltraScale and UltraScale+ devices and packages.

Kintex UltraScale Device-Package Combinations and Maximum I/Os

Table 4: Kintex UltraScale Device-Package Combinations and Maximum I/Os

Package (1)(2)(3)	Package Dimensions (mm)	KU025	KU035	KU040	KU060	KU085	KU095	KU115
		HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH, GTY ⁽⁴⁾	HR, HP GTH
SFVA784 ⁽⁵⁾	23x23		104, 364 8	104, 364 8				
FBVA676 ⁽⁵⁾	27x27		104, 208 16	104, 208 16				
FBVA900 ⁽⁵⁾	31x31		104, 364 16	104, 364 16				
FFVA1156	35x35	104, 208 12	104, 416 16	104, 416 20	104, 416 28		52, 468 20, 8	
FFVA1517	40x40				104, 520 32			
FLVA1517	40x40					104, 520 48		104, 520 48
FFVC1517	40x40						52, 468 20, 20	
FLVD1517	40x40							104, 234 64
FFVB1760	42.5x42.5						52, 650 32, 16	
FLVB1760	42.5x42.5					104, 572 44		104, 598 52
FLVD1924	45x45							156, 676 52
FLVF1924	45x45					104, 520 56		104, 624 64
FLVA2104	47.5x47.5							156, 676 52
FFVB2104	47.5x47.5						52, 650 32, 32	
FLVB2104	47.5x47.5							104, 598 64

Notes:

- Go to [Ordering Information](#) for package designation details.
- FB/FF/FL packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
- Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.
- GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s.
- GTH transceivers in SF/FB packages support data rates up to 12.5Gb/s.

Virtex UltraScale Device-Package Combinations and Maximum I/Os

Table 8: Virtex UltraScale Device-Package Combinations and Maximum I/Os

Package ⁽¹⁾⁽²⁾⁽³⁾	Package Dimensions (mm)	VU065	VU080	VU095	VU125	VU160	VU190	VU440
		HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY
FFVC1517	40x40	52, 468 20, 20	52, 468 20, 20	52, 468 20, 20				
FFVD1517	40x40		52, 286 32, 32	52, 286 32, 32				
FLVD1517	40x40				52, 286 40, 32			
FFVB1760	42.5x42.5		52, 650 32, 16	52, 650 32, 16				
FLVB1760	42.5x42.5				52, 650 36, 16			
FFVA2104	47.5x47.5		52, 780 28, 24	52, 780 28, 24				
FLVA2104	47.5x47.5				52, 780 28, 24			
FFVB2104	47.5x47.5		52, 650 32, 32	52, 650 32, 32				
FLVB2104	47.5x47.5				52, 650 40, 36			
FLGB2104	47.5x47.5					52, 650 40, 36	52, 650 40, 36	
FFVC2104	47.5x47.5			52, 364 32, 32				
FLVC2104	47.5x47.5				52, 364 40, 40			
FLGC2104	47.5x47.5					52, 364 52, 52	52, 364 52, 52	
FLGB2377	50x50							52, 1248 36, 0
FLGA2577	52.5x52.5						0, 448 60, 60	
FLGA2892	55x55							52, 1404 48, 0

Notes:

- Go to [Ordering Information](#) for package designation details.
- All packages have 1.0mm ball pitch.
- Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.

Virtex UltraScale+ FPGA Feature Summary

Table 9: Virtex UltraScale+ FPGA Feature Summary

	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
System Logic Cells	862,050	1,313,763	1,724,100	2,586,150	2,835,000	3,780,000	961,800	961,800	1,906,800	2,851,800
CLB Flip-Flops	788,160	1,201,154	1,576,320	2,364,480	2,592,000	3,456,000	879,360	879,360	1,743,360	2,607,360
CLB LUTs	394,080	600,577	788,160	1,182,240	1,296,000	1,728,000	439,680	439,680	871,680	1,303,680
Max. Distributed RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	12.5	12.5	24.6	36.7
Block RAM Blocks	720	1,024	1,440	2,160	2,016	2,688	672	672	1,344	2,016
Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	23.6	23.6	47.3	70.9
UltraRAM Blocks	320	470	640	960	960	1,280	320	320	640	960
UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	90.0	90.0	180.0	270.0
HBM DRAM (GB)	–	–	–	–	–	–	4	8	8	8
CMTs (1 MMCM and 2 PLLs)	10	20	20	30	12	16	4	4	8	12
Max. HP I/O ⁽¹⁾	520	832	832	832	624	832	208	208	416	624
DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	2,880	2,880	5,952	9,024
System Monitor	1	2	2	3	3	4	1	1	2	3
GTY Transceivers 32.75Gb/s ⁽²⁾	40	80	80	120	96	128	32	32	64	96
Transceiver Fractional PLLs	20	40	40	60	48	64	16	16	32	48
PCIe Gen3 x16 and Gen4 x8	2	4	4	6	3	4	4	4	5	6
CCIX Ports ⁽³⁾	–	–	–	–	–	–	4	4	4	4
150G Interlaken	3	4	6	9	6	8	0	0	2	4
100G Ethernet w/RS-FEC	3	4	6	9	9	12	2	2	5	8

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s. See [Table 10](#).
3. A CCIX port requires the use of a PCIe Gen3 x16 / Gen4 x8 block.

Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 10: Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

Package (1)(2)(3)	Package Dimensions (mm)	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
		HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY
FFVC1517	40x40	520, 40									
FLGF1924(4)	45x45					624, 64					
FLVA2104	47.5x47.5		832, 52	832, 52							
FLGA2104	47.5x47.5				832, 52						
FHGA2104	52.5x52.5(5)						832, 52				
FLVB2104	47.5x47.5		702, 76	702, 76							
FLGB2104	47.5x47.5				702, 76	572, 76					
FHGB2104	52.5x52.5(5)						702, 76				
FLVC2104	47.5x47.5		416, 80	416, 80							
FLGC2104	47.5x47.5				416, 104	416, 96					
FHGC2104	52.5x52.5(5)						416, 104				
FSGD2104	47.5x47.5				676, 76	572, 76					
FIGD2104	52.5x52.5(5)						676, 76				
FLGA2577	52.5x52.5				448, 120	448, 96	448, 128				
FSVH1924	45x45							208, 32			
FSVH2104	47.5x47.5								208, 32	416, 64	
FSVH2892	55x55									416, 64	624, 96

Notes:

- Go to [Ordering Information](#) for package designation details.
- All packages have 1.0mm ball pitch.
- Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.
- GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s.
- These 52.5x52.5mm overhang packages have the same PCB ball footprint as the corresponding 47.5x47.5mm packages (i.e., the same last letter and number sequence) and are footprint compatible.

Zynq UltraScale+: CG Device-Package Combinations and Maximum I/Os

Table 12: Zynq UltraScale+: CG Device-Package Combinations and Maximum I/Os

Package (1)(2)(3)(4)(5)	Package Dimensions (mm)	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SBVA484(6)	19x19	24, 58 0, 0	24, 58 0, 0					
SFVA625	21x21	24, 156 0, 0	24, 156 0, 0					
SFVC784(7)	23x23	96, 156 0, 0	96, 156 0, 0	96, 156 4, 0	96, 156 4, 0			
FBVB900	31x31			48, 156 16, 0	48, 156 16, 0		48, 156 16, 0	
FFVC900	31x31					48, 156 16, 0		48, 156 16, 0
FFVB1156	35x35					120, 208 24, 0		120, 208 24, 0
FFVC1156	35x35						48, 312 20, 0	
FFVF1517	40x40						48, 416 24, 0	

Notes:

1. Go to [Ordering Information](#) for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. All device package combinations bond out 214 PS I/O except ZU2CG and ZU3CG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
5. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
6. All 58 HP I/O pins are powered by the same V_{CCO} supply.
7. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

Table 14: Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

Package (1)(2)(3)(4)(5)	Package Dimensions (mm)	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SBVA484(6)	19x19	24, 58 0, 0	24, 58 0, 0									
SFVA625	21x21	24, 156 0, 0	24, 156 0, 0									
SFVC784(7)	23x23	96, 156 0, 0	96, 156 0, 0	96, 156 4, 0	96, 156 4, 0							
FBVB900	31x31			48, 156 16, 0	48, 156 16, 0		48, 156 16, 0					
FFVC900	31x31					48, 156 16, 0		48, 156 16, 0		48, 156 16, 0		
FFVB1156	35x35					120, 208 24, 0		120, 208 24, 0		120, 208 24, 0		
FFVC1156	35x35						48, 312 20, 0		48, 312 20, 0			
FFVB1517	40x40								72, 416 16, 0		72, 572 16, 0	72, 572 16, 0
FFVF1517	40x40						48, 416 24, 0		48, 416 32, 0			
FFVC1760	42.5x42.5								96, 416 32, 16		96, 416 32, 16	96, 416 32, 16
FFVD1760	42.5x42.5										48, 260 44, 28	48, 260 44, 28
FFVE1924	45x45										96, 572 44, 0	96, 572 44, 0

Notes:

- Go to [Ordering Information](#) for package designation details.
- FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
- All device package combinations bond out 4 PS-GTR transceivers.
- All device package combinations bond out 214 PS I/O except ZU2EG and ZU3EG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
- Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
- All 58 HP I/O pins are powered by the same V_{CCO} supply.
- GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

Table 16: Zynq UltraScale+: EV Device-Package Combinations and Maximum I/Os

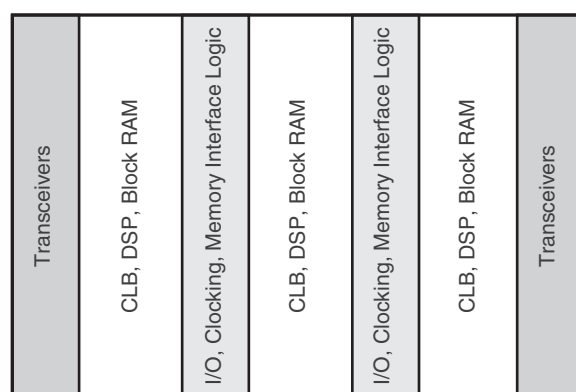
Package (1)(2)(3)(4)	Package Dimensions (mm)	ZU4EV	ZU5EV	ZU7EV
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SFVC784 ⁽⁵⁾	23x23	96, 156 4, 0	96, 156 4, 0	
FBVB900	31x31	48, 156 16, 0	48, 156 16, 0	48, 156 16, 0
FFVC1156	35x35			48, 312 20, 0
FFVF1517	40x40			48, 416 24, 0

Notes:

1. Go to [Ordering Information](#) for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.
5. Packages with the same last letter and number sequence, e.g., B900, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.

Device Layout

UltraScale devices are arranged in a column-and-grid layout. Columns of resources are combined in different ratios to provide the optimum capability for the device density, target market or application, and device cost. At the core of UltraScale+ MPSoCs is the processing system that displaces some of the full or partial columns of programmable logic resources. [Figure 1](#) shows a device-level view with resources grouped together. For simplicity, certain resources such as the processing system, integrated blocks for PCIe, configuration logic, and System Monitor are not shown.



DS890_01_101712

Figure 1: FPGA with Columnar Resources

Resources within the device are divided into segmented clock regions. The height of a clock region is 60 CLBs. A bank of 52 I/Os, 24 DSP slices, 12 block RAMs, or 4 transceiver channels also matches the height of a clock region. The width of a clock region is essentially the same in all cases, regardless of device size or the mix of resources in the region, enabling repeatable timing results. Each segmented clock region

(ACP), providing a low latency coherent port for accelerators in the PL. To support real-time debug and trace, each core also has an Embedded Trace Macrocell (ETM) that communicates with the ARM CoreSight™ Debug System.

Real-Time Processing Unit (RPU)

The RPU in the PS contains a dual-core ARM Cortex-R5 PS. Cortex-R5 cores are 32-bit real-time processor cores based on ARM-v7R architecture. Each of the Cortex-R5 cores has 32KB of level-1 (L1) instruction and data cache with ECC protection. In addition to the L1 caches, each of the Cortex-R5 cores also has a 128KB tightly coupled memory (TCM) interface for real-time single cycle access. The RPU also has a dedicated interrupt controller. The RPU can operate in either split or lock-step mode. In split mode, both processors run independently of each other. In lock-step mode, they run in parallel with each other, with integrated comparator logic, and the TCMs are used as 256KB unified memory. The RPU communicates with the rest of the PS via the 128-bit AXI-4 ports connected to the low power domain switch. It also communicates directly with the PL through 128-bit low latency AXI-4 ports. To support real-time debug and trace each core also has an embedded trace macrocell (ETM) that communicates with the ARM CoreSight Debug System.

External Memory

The PS can interface to many types of external memories through dedicated memory controllers. The dynamic memory controller supports DDR3, DDR3L, DDR4, LPDDR3, and LPDDR4 memories. The multi-protocol DDR memory controller can be configured to access a 2GB address space in 32-bit addressing mode and up to 32GB in 64-bit addressing mode using a single or dual rank configuration of 8-bit, 16-bit, or 32-bit DRAM memories. Both 32-bit and 64-bit bus access modes are protected by ECC using extra bits.

The SD/eMMC controller supports 1 and 4 bit data interfaces at low, default, high-speed, and ultra-high-speed (UHS) clock rates. This controller also supports 1-, 4-, or 8-bit-wide eMMC interfaces that are compliant to the eMMC 4.51 specification. eMMC is one of the primary boot and configuration modes for Zynq UltraScale+ MPSoCs and supports boot from managed NAND devices. The controller has a built-in DMA for enhanced performance.

The Quad-SPI controller is one of the primary boot and configuration devices. It supports 4-byte and 3-byte addressing modes. In both addressing modes, single, dual-stacked, and dual-parallel configurations are supported. Single mode supports a quad serial NOR flash memory, while in double stacked and double parallel modes, it supports two quad serial NOR flash memories.

The NAND controller is based on ONFI3.1 specification. It has an 8-pin interface and provides 200Mb/s of bandwidth in synchronous mode. It supports 24 bits of ECC thus enabling support for SLC NAND memories. It has two chip-selects to support deeper memory and a built-in DMA for enhanced performance.

Graphics Processing Unit (GPU)

The dedicated ARM Mali-400 MP2 GPU in the PS supports 2D and 3D graphics acceleration up to 1080p resolution. The Mali-400 supports OpenGL ES 1.1 and 2.0 for 3D graphics and Open VG 1.1 standards for 2D vector graphics. It has a geometry processor (GP) and 2 pixel processors to perform tile rendering operations in parallel. It has dedicated Memory management units for GP and pixel processors, which supports 4 KB page size. The GPU also has 64KB level-2 (L2) read-only cache. It supports 4X and 16X Full scene Anti-Aliasing (FSAA). It is fully autonomous, enabling maximum parallelization between APU and GPU. It has built-in hardware texture decompression, allowing the texture to remain compressed (in ETC format) in graphics hardware and decompress the required samples on the fly. It also supports efficient alpha blending of multiple layers in hardware without additional bandwidth consumption. It has a pixel fill rate of 2Mpixel/sec/MHz and a triangle rate of 0.1Mvertex/sec/MHz. The GPU supports extensive texture format for RGBA 8888, 565, and 1556 in Mono 8, 16, and YUV formats. For power sensitive applications, the GPU supports clock and power gating for each GP, pixel processors, and L2 cache. During power gating, GPU does not consume any static or dynamic power; during clock gating, it only consumes static power.

Video Codec Unit (VCU)

The video codec unit (VCU) provides multi-standard video encoding and decoding capabilities, including: High Efficiency Video Coding (HEVC), i.e., H.265; and Advanced Video Coding (AVC), i.e., H.264 standards. The VCU is capable of simultaneous encode and decode at rates up to 4Kx2K at 60 frames per second (fps) (approx. 600Mpixel/sec) or 8Kx4K at a reduced frame rate (~15fps).

Input/Output

All UltraScale devices, whether FPGA or MPSoC, have I/O pins for communicating to external components. In addition, in the MPSoC's PS, there are another 78 I/Os that the I/O peripherals use to communicate to external components, referred to as multiplexed I/O (MIO). If more than 78 pins are required by the I/O peripherals, the I/O pins in the PL can be used to extend the MPSoC interfacing capability, referred to as extended MIO (EMIO).

The number of I/O pins in UltraScale FPGAs and in the programmable logic of UltraScale+ MPSoCs varies depending on device and package. Each I/O is configurable and can comply with a large number of I/O standards. The I/Os are classed as high-range (HR), high-performance (HP), or high-density (HD). The HR I/Os offer the widest range of voltage support, from 1.2V to 3.3V. The HP I/Os are optimized for highest performance operation, from 1.0V to 1.8V. The HD I/Os are reduced-feature I/Os organized in banks of 24, providing voltage support from 1.2V to 3.3V.

All I/O pins are organized in banks, with 52 HP or HR pins per bank or 24 HD pins per bank. Each bank has one common V_{CCO} output buffer power supply, which also powers certain input buffers. In addition, HR banks can be split into two half-banks, each with their own V_{CCO} supply. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). V_{REF} pins can be driven directly from the PCB or internally generated using the internal V_{REF} generator circuitry present in each bank.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100 Ω internal resistor. All UltraScale devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. UltraScale+ families add support for MIPI with a dedicated D-PHY in the I/O bank.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally “auto-adapt” to automatically learn and compensate for different interconnect characteristics. This enables even more margin for 10G+ and 25G+ backplanes.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

Integrated Interface Blocks for PCI Express Designs

The UltraScale architecture includes integrated blocks for PCIe technology that can be configured as an Endpoint or Root Port. UltraScale devices are compliant to the PCI Express Base Specification Revision 3.0. UltraScale+ devices are compliant to the PCI Express Base Specification Revision 3.1 for Gen3 and lower data rates, and compatible with the PCI Express Base Specification Revision 4.0 (rev 0.5) for Gen4 data rates.

The Root Port can be used to build the basis for a compatible Root Complex, to allow custom chip-to-chip communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the FPGA or MPSoC.

This block is highly configurable to system design requirements and can operate up to the maximum lane widths and data rates listed in [Table 18](#).

Table 18: PCIe Maximum Configurations

	Kintex UltraScale	Kintex UltraScale+	Virtex UltraScale	Virtex UltraScale+	Zynq UltraScale+
Gen1 (2.5Gb/s)	x8	x16	x8	x16	x16
Gen2 (5Gb/s)	x8	x16	x8	x16	x16
Gen3 (8Gb/s)	x8	x16	x8	x16	x16
Gen4 (16Gb/s) ⁽¹⁾		x8		x8	x8

Notes:

1. Transceivers in Kintex UltraScale and Virtex UltraScale devices are capable of operating at Gen4 data rates.

For high-performance applications, advanced buffering techniques of the block offer a flexible maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block for PCIe, the transceivers, block RAM, and clocking resources) into an Endpoint or Root Port solution. The system designer has control over many configurable parameters: link width and speed, maximum payload size, FPGA or MPSoC logic interface speeds, reference clock frequency, and base address register decoding and filtering.

Stacked Silicon Interconnect (SSI) Technology

Many challenges associated with creating high-capacity devices are addressed by Xilinx with the second generation of the pioneering 3D SSI technology. SSI technology enables multiple super-logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders, to create a single device with more than 20,000 low-power inter-SLR connections. Dedicated interface tiles within the SLRs provide ultra-high bandwidth, low latency connectivity to other SLRs. Table 19 shows the number of SLRs in devices that use SSI technology and their dimensions.

Table 19: UltraScale and UltraScale+ 3D IC SLR Count and Dimensions

	Kintex UltraScale		Virtex UltraScale				Virtex UltraScale+								
Device	KU085	KU115	VU125	VU160	VU190	VU440	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
# SLRs	2	2	2	3	3	3	2	2	3	3	4	1	1	2	3
SLR Width (in regions)	6	6	6	6	6	9	6	6	6	8	8	8	8	8	8
SLR Height (in regions)	5	5	5	5	5	5	5	5	5	4	4	4	4	4	4

Clock Management

The clock generation and distribution components in UltraScale devices are located adjacent to the columns that contain the memory interface and input and output circuitry. This tight coupling of clocking and I/O provides low-latency clocking to the I/O for memory interfaces and other I/O protocols. Within every clock management tile (CMT) resides one mixed-mode clock manager (MMCM), two PLLs, clock distribution buffers and routing, and dedicated circuitry for implementing external memory interfaces.

Mixed-Mode Clock Manager

The mixed-mode clock manager (MMCM) can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of the MMCM is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers (D, M, and O) that are programmable by configuration and during normal operation via the Dynamic Reconfiguration Port (DRP). The pre-divider D reduces the input frequency and feeds one input of the phase/frequency comparator. The feedback divider M acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each phase can be selected to drive one of the output dividers, and each divider is programmable by configuration to divide by any integer from 1 to 128.

The MMCM has three input-jitter filter options: low bandwidth, high bandwidth, or optimized mode. Low-Bandwidth mode has the best jitter attenuation. High-Bandwidth mode has the best phase offset. Optimized mode allows the tools to find the best setting.

After copying the FSBL to OCM, the processor executes the FSBL. Xilinx supplies example FSBLs or users can create their own. The FSBL initiates the boot of the PS and can load and configure the PL, or configuration of the PL can be deferred to a later stage. The FSBL typically loads either a user application or an optional second stage boot loader (SSBL) such as U-Boot. Users obtain example SSBL from Xilinx or a third party, or they can create their own SSBL. The SSBL continues the boot process by loading code from any of the primary boot devices or from other sources such as USB, Ethernet, etc. If the FSBL did not configure the PL, the SSBL can do so, or again, the configuration can be deferred to a later stage.

The static memory interface controller (NAND, eMMC, or Quad-SPI) is configured using default settings. To improve device configuration speed, these settings can be modified by information provided in the boot image header. The ROM boot image is not user readable or executable after boot.

Configuring FPGAs

The SPI (serial NOR) interface (x1, x2, x4, and dual x4 modes) and the BPI (parallel NOR) interface (x8 and x16 modes) are two common methods used for configuring the FPGA. Users can directly connect an SPI or BPI flash to the FPGA, and the FPGA's internal configuration logic reads the bitstream out of the flash and configures itself, eliminating the need for an external controller. The FPGA automatically detects the bus width on the fly, eliminating the need for any external controls or switches. Bus widths supported are x1, x2, x4, and dual x4 for SPI, and x8 and x16 for BPI. The larger bus widths increase configuration speed and reduce the amount of time it takes for the FPGA to start up after power-on.

In master mode, the FPGA can drive the configuration clock from an internally generated clock, or for higher speed configuration, the FPGA can use an external configuration clock source. This allows high-speed configuration with the ease of use characteristic of master mode. Slave modes up to 32 bits wide that are especially useful for processor-driven configuration are also supported by the FPGA. In addition, the new media configuration access port (MCAP) provides a direct connection between the integrated block for PCIe and the configuration logic to simplify configuration over PCIe.

SEU detection and mitigation (SEM) IP, RSA authentication, post-configuration CRC, and Security Monitor (SecMon) IP are not supported in the KU025 FPGA.

Packaging

The UltraScale devices are available in a variety of organic flip-chip and lidless flip-chip packages supporting different quantities of I/Os and transceivers. Maximum supported performance can depend on the style of package and its material. Always refer to the specific device data sheet for performance specifications by package type.

In flip-chip packages, the silicon device is attached to the package substrate using a high-performance flip-chip process. Decoupling capacitors are mounted on the package substrate to optimize signal integrity under simultaneous switching of outputs (SSO) conditions.

Ordering Information

Table 21 shows the speed and temperature grades available in the different device families. V_{CCINT} supply voltage is listed in parentheses.

Table 21: Speed Grade and Temperature Grade

Device Family	Devices	Speed Grade and Temperature Grade			
		Commercial (C)	Extended (E)		Industrial (I)
		0°C to +85°C	0°C to +100°C	0°C to +110°C	–40°C to +100°C
Kintex UltraScale	All		-3E ⁽¹⁾ (1.0V)		
			-2E (0.95V)		-2I (0.95V)
		-1C (0.95V)			-1I (0.95V)
					-1LI ⁽¹⁾ (0.95V or 0.90V)
Kintex UltraScale+	All		-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE ⁽²⁾ (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI (0.85V or 0.72V)
Virtex UltraScale	VU065 VU080 VU095 VU125 VU160 VU190		-3E (1.0V)		
			-2E (0.95V)		-2I (0.95V)
			-1HE (0.95V or 1.0V)		-1I (0.95V)
	VU440		-3E (1.0V)		
			-2E (0.95V)		-2I (0.95V)
		-1C (0.95V)			-1I (0.95V)
Virtex UltraScale+	VU3P VU5P VU7P VU9P VU11P VU13P		-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE ⁽²⁾ (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
	VU31P VU33P VU35P VU37P		-3E (0.90V)		
			-2E (0.85V)		
				-2LE ⁽²⁾ (0.85V or 0.72V)	
			-1E (0.85V)		

The ordering information shown in [Figure 3](#) applies to all packages in the Kintex UltraScale and Virtex UltraScale FPGAs. Refer to the Package Marking section of [UG575, UltraScale and UltraScale+ FPGAs Packaging and Pinouts User Guide](#) for a more detailed explanation of the device markings.



Figure 3: Kintex UltraScale and Virtex UltraScale FPGA Ordering Information

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/15/2017	2.11	Updated Table 1 , Table 9 : Converted HBM from Gb to GB. Updated Table 11 , Table 13 , and Table 15 : Updated DSP count for Zynq UltraScale+ MPSoCs. Updated Cache Coherent Interconnect for Accelerators (CCIX) . Updated High Bandwidth Memory (HBM) . Updated Table 21 : Added -2E speed grade to all UltraScale+ devices. Removed -3E from XCZU2 and XCZU3.
11/09/2016	2.10	Updated Table 1 . Added HBM devices to Table 9 , Table 10 , Table 19 and new High Bandwidth Memory (HBM) section. Added Cache Coherent Interconnect for Accelerators (CCIX) section.
09/27/2016	2.9	Updated Table 5 , Table 12 , Table 13 , and Table 14 .
06/03/2016	2.8	Added Zynq UltraScale+ MPSoC CG devices: Added Table 2 . Updated Table 11 , Table 12 , Table 21 , and Figure 5 . Created separate tables for EG and EV devices: Table 13 , Table 14 , Table 15 , and Table 16 . Updated Table 1 , Table 3 , Table 5 and notes, Table 6 and notes, Table 7 , Table 9 , Table 10 , Processing System Overview , and Processing System (PS) details.
02/17/2016	2.7	Added Migrating Devices . Updated Table 4 , Table 5 , Table 6 , Table 10 , Table 11 , Table 12 , and Figure 4 .
12/15/2015	2.6	Updated Table 1 , Table 5 , Table 6 , Table 9 , Table 12 , and Configuration .
11/24/2015	2.5	Updated Configuration, Encryption, and System Monitoring , Table 5 , Table 9 , Table 11 , and Table 21 .
10/15/2015	2.4	Updated Table 1 , Table 3 , Table 5 , Table 7 , Table 9 , and Table 11 with System Logic Cells. Updated Figure 3 . Updated Table 19 .
09/29/2015	2.3	Added A1156 to KU095 in Table 4 . Updated Table 5 . Updated Max. Distributed RAM in Table 9 . Updated Distributed RAM in Table 11 . Added Table 19 . Updated Table 21 . Updated Figure 3 .
08/14/2015	2.2	Updated Table 1 . Added XCKU025 to Table 3 , Table 4 , and Table 21 . Updated Table 7 , Table 9 , Table 11 , Table 12 , Table 18 . Updated System Monitor . Added voltage information to Table 21 .
04/27/2015	2.1	Updated Table 1 , Table 3 , Table 4 , Table 5 , Table 6 , Table 7 , Table 10 , Table 11 , Table 12 , Table 17 , I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken, Integrated Interface Blocks for PCI Express Designs , USB 3.0/2.0, Clock Management, System Monitor, and Figure 3 .
02/23/2015	2.0	UltraScale+ device information (Kintex UltraScale+ FPGA, Virtex UltraScale+ FPGA, and Zynq UltraScale+ MPSoC) added throughout document.
12/16/2014	1.6	Updated Table 1 ; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 3 , Table 7 ; Table 8 ; and Table 17 .
11/17/2014	1.5	Updated I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 1 ; Table 4 ; Table 7 ; Table 8 ; Table 17 ; Input/Output ; and Figure 3 .
09/16/2014	1.4	Updated Logic Cell information in Table 1 . Updated Table 3 ; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 7 ; Table 8 ; Integrated Block for 100G Ethernet ; and Figure 3 .
05/20/2014	1.3	Updated Table 8 .
05/13/2014	1.2	Added Ordering Information . Updated Table 1 , Clocks and Memory Interfaces , Table 3 , Table 7 (removed XCVU145; added XCVU190), Table 8 (removed XCVU145; removed FLVD1924 from XCVU160; added XCVU190; updated Table Notes), Table 17 , Integrated Interface Blocks for PCI Express Designs , and Integrated Block for Interlaken , and Memory Interfaces .

Date	Version	Description of Revisions
02/06/2014	1.1	Updated PCIe information in Table 1 and Table 3 . Added FFVJ1924 package to Table 8 .
12/10/2013	1.0	Initial Xilinx release.