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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	30300
Number of Logic Elements/Cells	530250
Total RAM Bits	21606000
Number of I/O	520
Number of Gates	-
Voltage - Supply	0.880V ~ 0.979V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcku040-l1ffva1156i

Summary of Features

Processing System Overview

UltraScale+ MPSoCs feature dual and quad core variants of the ARM Cortex-A53 (APU) with dual-core ARM Cortex-R5 (RPU) processing system (PS). Some devices also include a dedicated ARM Mali™-400 MP2 graphics processing unit (GPU). See [Table 2](#).

Table 2: Zynq UltraScale+ MPSoC Device Features

	CG Devices	EG Devices	EV Devices
APU	Dual-core ARM Cortex-A53	Quad-core ARM Cortex-A53	Quad-core ARM Cortex-A53
RPU	Dual-core ARM Cortex-R5	Dual-core ARM Cortex-R5	Dual-core ARM Cortex-R5
GPU	–	Mali-400MP2	Mali-400MP2
VCU	–	–	H.264/H.265

To support the processors' functionality, a number of peripherals with dedicated functions are included in the PS. For interfacing to external memories for data or configuration storage, the PS includes a multi-protocol dynamic memory controller, a DMA controller, a NAND controller, an SD/eMMC controller and a Quad SPI controller. In addition to interfacing to external memories, the APU also includes a Level-1 (L1) and Level-2 (L2) cache hierarchy; the RPU includes an L1 cache and Tightly Coupled memory subsystem. Each has access to a 256KB on-chip memory.

For high-speed interfacing, the PS includes 4 channels of transmit (TX) and receive (RX) pairs of transceivers, called PS-GTR transceivers, supporting data rates of up to 6.0Gb/s. These transceivers can interface to the high-speed peripheral blocks to support PCIe Gen2 root complex or end point in x1, x2, or x4 configurations; Serial-ATA (SATA) at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates; and up to two lanes of Display Port at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s data rates. The PS-GTR transceivers can also interface to components over USB 3.0 and Serial Gigabit Media Independent Interface (SGMII).

For general connectivity, the PS includes: a pair of USB 2.0 controllers, which can be configured as host, device, or On-The-Go (OTG); an I2C controller; a UART; and a CAN2.0B controller that conforms to ISO11898-1. There are also four triple speed Ethernet MACs and 128 bits of GPIO, of which 78 bits are available through the MIO and 96 through the EMIO.

High-bandwidth connectivity based on the ARM AMBA® AXI4 protocol connects the processing units with the peripherals and provides interface between the PS and the programmable logic (PL).

For additional information, go to: [DS891](#), *Zynq UltraScale+ MPSoC Overview*.

Migrating Devices

UltraScale and UltraScale+ families provide footprint compatibility to enable users to migrate designs from one device or family to another. Any two packages with the same footprint identifier code are footprint compatible. For example, Kintex UltraScale devices in the A1156 packages are footprint compatible with Kintex UltraScale+ devices in the A1156 packages. Likewise, Virtex UltraScale devices in the B2104 packages are compatible with Virtex UltraScale+ devices and Kintex UltraScale devices in the B2104 packages. All valid device/package combinations are provided in the Device-Package Combinations and Maximum I/Os tables in this document. Refer to [UG583](#), *UltraScale Architecture PCB Design User Guide* for more detail on migrating between UltraScale and UltraScale+ devices and packages.

Kintex UltraScale Device-Package Combinations and Maximum I/Os

Table 4: Kintex UltraScale Device-Package Combinations and Maximum I/Os

Package (1)(2)(3)	Package Dimensions (mm)	KU025	KU035	KU040	KU060	KU085	KU095	KU115
		HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH, GTY ⁽⁴⁾	HR, HP GTH
SFVA784 ⁽⁵⁾	23x23		104, 364 8	104, 364 8				
FBVA676 ⁽⁵⁾	27x27		104, 208 16	104, 208 16				
FBVA900 ⁽⁵⁾	31x31		104, 364 16	104, 364 16				
FFVA1156	35x35	104, 208 12	104, 416 16	104, 416 20	104, 416 28		52, 468 20, 8	
FFVA1517	40x40				104, 520 32			
FLVA1517	40x40					104, 520 48		104, 520 48
FFVC1517	40x40						52, 468 20, 20	
FLVD1517	40x40							104, 234 64
FFVB1760	42.5x42.5						52, 650 32, 16	
FLVB1760	42.5x42.5					104, 572 44		104, 598 52
FLVD1924	45x45							156, 676 52
FLVF1924	45x45					104, 520 56		104, 624 64
FLVA2104	47.5x47.5							156, 676 52
FFVB2104	47.5x47.5						52, 650 32, 32	
FLVB2104	47.5x47.5							104, 598 64

Notes:

- Go to [Ordering Information](#) for package designation details.
- FB/FF/FL packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
- Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.
- GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s.
- GTH transceivers in SF/FB packages support data rates up to 12.5Gb/s.

Virtex UltraScale+ FPGA Feature Summary

Table 9: Virtex UltraScale+ FPGA Feature Summary

	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
System Logic Cells	862,050	1,313,763	1,724,100	2,586,150	2,835,000	3,780,000	961,800	961,800	1,906,800	2,851,800
CLB Flip-Flops	788,160	1,201,154	1,576,320	2,364,480	2,592,000	3,456,000	879,360	879,360	1,743,360	2,607,360
CLB LUTs	394,080	600,577	788,160	1,182,240	1,296,000	1,728,000	439,680	439,680	871,680	1,303,680
Max. Distributed RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	12.5	12.5	24.6	36.7
Block RAM Blocks	720	1,024	1,440	2,160	2,016	2,688	672	672	1,344	2,016
Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	23.6	23.6	47.3	70.9
UltraRAM Blocks	320	470	640	960	960	1,280	320	320	640	960
UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	90.0	90.0	180.0	270.0
HBM DRAM (GB)	–	–	–	–	–	–	4	8	8	8
CMTs (1 MMCM and 2 PLLs)	10	20	20	30	12	16	4	4	8	12
Max. HP I/O ⁽¹⁾	520	832	832	832	624	832	208	208	416	624
DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	2,880	2,880	5,952	9,024
System Monitor	1	2	2	3	3	4	1	1	2	3
GTY Transceivers 32.75Gb/s ⁽²⁾	40	80	80	120	96	128	32	32	64	96
Transceiver Fractional PLLs	20	40	40	60	48	64	16	16	32	48
PCIe Gen3 x16 and Gen4 x8	2	4	4	6	3	4	4	4	5	6
CCIX Ports ⁽³⁾	–	–	–	–	–	–	4	4	4	4
150G Interlaken	3	4	6	9	6	8	0	0	2	4
100G Ethernet w/RS-FEC	3	4	6	9	9	12	2	2	5	8

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s. See [Table 10](#).
3. A CCIX port requires the use of a PCIe Gen3 x16 / Gen4 x8 block.

Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 10: Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

Package (1)(2)(3)	Package Dimensions (mm)	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
		HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY
FFVC1517	40x40	520, 40									
FLGF1924(4)	45x45					624, 64					
FLVA2104	47.5x47.5		832, 52	832, 52							
FLGA2104	47.5x47.5				832, 52						
FHGA2104	52.5x52.5(5)						832, 52				
FLVB2104	47.5x47.5		702, 76	702, 76							
FLGB2104	47.5x47.5				702, 76	572, 76					
FHGB2104	52.5x52.5(5)						702, 76				
FLVC2104	47.5x47.5		416, 80	416, 80							
FLGC2104	47.5x47.5				416, 104	416, 96					
FHGC2104	52.5x52.5(5)						416, 104				
FSGD2104	47.5x47.5				676, 76	572, 76					
FIGD2104	52.5x52.5(5)						676, 76				
FLGA2577	52.5x52.5				448, 120	448, 96	448, 128				
FSVH1924	45x45							208, 32			
FSVH2104	47.5x47.5								208, 32	416, 64	
FSVH2892	55x55									416, 64	624, 96

Notes:

- Go to [Ordering Information](#) for package designation details.
- All packages have 1.0mm ball pitch.
- Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.
- GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s.
- These 52.5x52.5mm overhang packages have the same PCB ball footprint as the corresponding 47.5x47.5mm packages (i.e., the same last letter and number sequence) and are footprint compatible.

Zynq UltraScale+: CG Device-Package Combinations and Maximum I/Os

Table 12: Zynq UltraScale+: CG Device-Package Combinations and Maximum I/Os

Package (1)(2)(3)(4)(5)	Package Dimensions (mm)	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SBVA484(6)	19x19	24, 58 0, 0	24, 58 0, 0					
SFVA625	21x21	24, 156 0, 0	24, 156 0, 0					
SFVC784(7)	23x23	96, 156 0, 0	96, 156 0, 0	96, 156 4, 0	96, 156 4, 0			
FBVB900	31x31			48, 156 16, 0	48, 156 16, 0		48, 156 16, 0	
FFVC900	31x31					48, 156 16, 0		48, 156 16, 0
FFVB1156	35x35					120, 208 24, 0		120, 208 24, 0
FFVC1156	35x35						48, 312 20, 0	
FFVF1517	40x40						48, 416 24, 0	

Notes:

1. Go to [Ordering Information](#) for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. All device package combinations bond out 214 PS I/O except ZU2CG and ZU3CG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
5. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
6. All 58 HP I/O pins are powered by the same V_{CCO} supply.
7. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

Zynq UltraScale+: EG Device Feature Summary

Table 13: Zynq UltraScale+: EG Device Feature Summary

	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Application Processing Unit	Quad-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache										
Real-Time Processing Unit	Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM										
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC										
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters										
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII										
Graphic Processing Unit	ARM Mali-400 MP2; 64KB L2 Cache										
System Logic Cells	103,320	154,350	192,150	256,200	469,446	504,000	599,550	653,100	746,550	926,194	1,143,450
CLB Flip-Flops	94,464	141,120	175,680	234,240	429,208	460,800	548,160	597,120	682,560	846,806	1,045,440
CLB LUTs	47,232	70,560	87,840	117,120	214,604	230,400	274,080	298,560	341,280	423,403	522,720
Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
Block RAM Blocks	150	216	128	144	714	312	912	600	744	796	984
Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
UltraRAM Blocks	0	0	48	64	0	96	0	80	112	102	128
UltraRAM (Mb)	0	0	14.0	18.0	0	27.0	0	22.5	31.5	28.7	36.0
DSP Slices	240	360	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
CMTs	3	3	4	4	4	8	4	8	4	11	11
Max. HP I/O ⁽¹⁾	156	156	156	156	208	416	208	416	208	572	572
Max. HD I/O ⁽²⁾	96	96	96	96	120	48	120	96	120	96	96
System Monitor	2	2	2	2	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s ⁽³⁾	0	0	16	16	24	24	24	32	24	44	44
GTY Transceivers 32.75Gb/s	0	0	0	0	0	0	0	16	0	28	28
Transceiver Fractional PLLs	0	0	8	8	12	12	12	24	12	36	36
PCIe Gen3 x16 and Gen4 x8	0	0	2	2	0	2	0	4	0	4	5
150G Interlaken	0	0	0	0	0	0	0	1	0	2	4
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0	2	0	2	4

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 14](#).

Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

Table 14: Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

Package (1)(2)(3)(4)(5)	Package Dimensions (mm)	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SBVA484(6)	19x19	24, 58 0, 0	24, 58 0, 0									
SFVA625	21x21	24, 156 0, 0	24, 156 0, 0									
SFVC784(7)	23x23	96, 156 0, 0	96, 156 0, 0	96, 156 4, 0	96, 156 4, 0							
FBVB900	31x31			48, 156 16, 0	48, 156 16, 0		48, 156 16, 0					
FFVC900	31x31					48, 156 16, 0		48, 156 16, 0		48, 156 16, 0		
FFVB1156	35x35					120, 208 24, 0		120, 208 24, 0		120, 208 24, 0		
FFVC1156	35x35						48, 312 20, 0		48, 312 20, 0			
FFVB1517	40x40								72, 416 16, 0		72, 572 16, 0	72, 572 16, 0
FFVF1517	40x40						48, 416 24, 0		48, 416 32, 0			
FFVC1760	42.5x42.5								96, 416 32, 16		96, 416 32, 16	96, 416 32, 16
FFVD1760	42.5x42.5										48, 260 44, 28	48, 260 44, 28
FFVE1924	45x45										96, 572 44, 0	96, 572 44, 0

Notes:

- Go to [Ordering Information](#) for package designation details.
- FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
- All device package combinations bond out 4 PS-GTR transceivers.
- All device package combinations bond out 214 PS I/O except ZU2EG and ZU3EG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
- Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
- All 58 HP I/O pins are powered by the same V_{CCO} supply.
- GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

Zynq UltraScale+: EG Device Feature Summary

Table 15: Zynq UltraScale+: EV Device Feature Summary

	ZU4EV	ZU5EV	ZU7EV
Application Processing Unit	Quad-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache		
Real-Time Processing Unit	Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM		
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC		
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters		
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII		
Graphic Processing Unit	ARM Mali-400 MP2; 64KB L2 Cache		
Video Codec	1	1	1
System Logic Cells	192,150	256,200	504,000
CLB Flip-Flops	175,680	234,240	460,800
CLB LUTs	87,840	117,120	230,400
Distributed RAM (Mb)	2.6	3.5	6.2
Block RAM Blocks	128	144	312
Block RAM (Mb)	4.5	5.1	11.0
UltraRAM Blocks	48	64	96
UltraRAM (Mb)	14.0	18.0	27.0
DSP Slices	728	1,248	1,728
CMTs	4	4	8
Max. HP I/O ⁽¹⁾	156	156	416
Max. HD I/O ⁽²⁾	96	96	48
System Monitor	2	2	2
GTH Transceiver 16.3Gb/s ⁽³⁾	16	16	24
GTY Transceivers 32.75Gb/s	0	0	0
Transceiver Fractional PLLs	8	8	12
PCIe Gen3 x16 and Gen4 x8	2	2	2
150G Interlaken	0	0	0
100G Ethernet w/ RS-FEC	0	0	0

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 16](#).

Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

Table 16: Zynq UltraScale+: EV Device-Package Combinations and Maximum I/Os

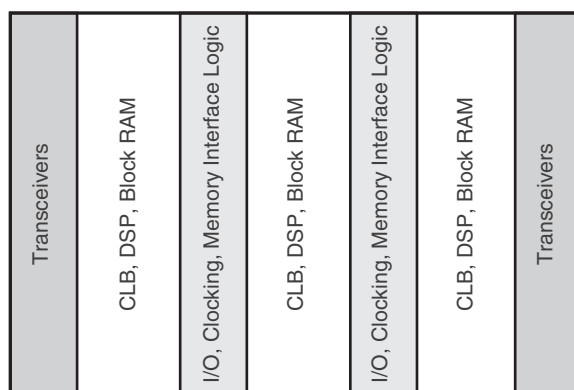
Package (1)(2)(3)(4)	Package Dimensions (mm)	ZU4EV	ZU5EV	ZU7EV
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SFVC784 ⁽⁵⁾	23x23	96, 156 4, 0	96, 156 4, 0	
FBVB900	31x31	48, 156 16, 0	48, 156 16, 0	48, 156 16, 0
FFVC1156	35x35			48, 312 20, 0
FFVF1517	40x40			48, 416 24, 0

Notes:

1. Go to [Ordering Information](#) for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.
5. Packages with the same last letter and number sequence, e.g., B900, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.

Device Layout

UltraScale devices are arranged in a column-and-grid layout. Columns of resources are combined in different ratios to provide the optimum capability for the device density, target market or application, and device cost. At the core of UltraScale+ MPSoCs is the processing system that displaces some of the full or partial columns of programmable logic resources. [Figure 1](#) shows a device-level view with resources grouped together. For simplicity, certain resources such as the processing system, integrated blocks for PCIe, configuration logic, and System Monitor are not shown.



DS890_01_101712

Figure 1: FPGA with Columnar Resources

Resources within the device are divided into segmented clock regions. The height of a clock region is 60 CLBs. A bank of 52 I/Os, 24 DSP slices, 12 block RAMs, or 4 transceiver channels also matches the height of a clock region. The width of a clock region is essentially the same in all cases, regardless of device size or the mix of resources in the region, enabling repeatable timing results. Each segmented clock region

contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. Figure 2 is a representation of an FPGA divided into regions.

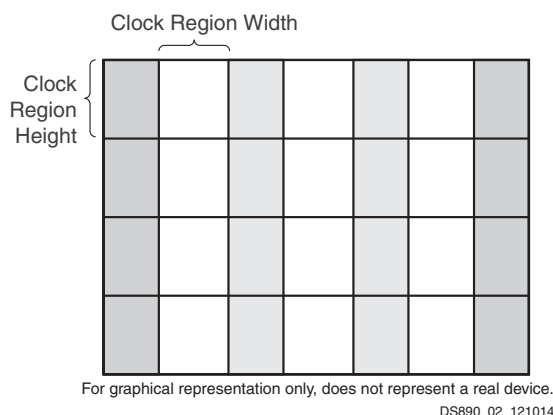


Figure 2: Column-Based FPGA Divided into Clock Regions

Processing System (PS)

Zynq UltraScale+ MPSoCs consist of a PS coupled with programmable logic. The contents of the PS varies between the different Zynq UltraScale+ devices. All devices contain an APU, an RPU, and many peripherals for connecting the multiple processing engines to external components. The EG and EV devices contain a GPU and the EV devices contain a video codec unit (VCU). The components of the PS are connected together and to the PL through a multi-layered ARM AMBA AXI non-blocking interconnect that supports multiple simultaneous master-slave transactions. Traffic through the interconnect can be regulated by the quality of service (QoS) block in the interconnect. Twelve dedicated AXI 32-bit, 64-bit, or 128-bit ports connect the PL to high-speed interconnect and DDR in the PS via a FIFO interface.

There are four independently controllable power domains: the PL plus three within the PS (full power, lower power, and battery power domains). Additionally, many peripherals support clock gating and power gating to further reduce dynamic and static power consumption.

Application Processing Unit (APU)

The APU has a feature-rich dual-core or quad-core ARM Cortex-A53 processor. Cortex-A53 cores are 32-bit/64-bit application processors based on ARM-v8A architecture, offering the best performance-to-power ratio. The ARMv8 architecture supports hardware virtualization. Each of the Cortex-A53 cores has: 32KB of instruction and data L1 caches, with parity and ECC protection respectively; a NEON SIMD engine; and a single and double precision floating point unit. In addition to these blocks, the APU consists of a snoop control unit and a 1MB L2 cache with ECC protection to enhance system-level performance. The snoop control unit keeps the L1 caches coherent thus eliminating the need of spending software bandwidth for coherency. The APU also has a built-in interrupt controller supporting virtual interrupts. The APU communicates to the rest of the PS through 128-bit AXI coherent extension (ACE) port via Cache Coherent Interconnect (CCI) block, using the System Memory Management Unit (SMMU). The APU is also connected to the Programmable Logic (PL), through the 128-bit accelerator coherency port

(ACP), providing a low latency coherent port for accelerators in the PL. To support real-time debug and trace, each core also has an Embedded Trace Macrocell (ETM) that communicates with the ARM CoreSight™ Debug System.

Real-Time Processing Unit (RPU)

The RPU in the PS contains a dual-core ARM Cortex-R5 PS. Cortex-R5 cores are 32-bit real-time processor cores based on ARM-v7R architecture. Each of the Cortex-R5 cores has 32KB of level-1 (L1) instruction and data cache with ECC protection. In addition to the L1 caches, each of the Cortex-R5 cores also has a 128KB tightly coupled memory (TCM) interface for real-time single cycle access. The RPU also has a dedicated interrupt controller. The RPU can operate in either split or lock-step mode. In split mode, both processors run independently of each other. In lock-step mode, they run in parallel with each other, with integrated comparator logic, and the TCMs are used as 256KB unified memory. The RPU communicates with the rest of the PS via the 128-bit AXI-4 ports connected to the low power domain switch. It also communicates directly with the PL through 128-bit low latency AXI-4 ports. To support real-time debug and trace each core also has an embedded trace macrocell (ETM) that communicates with the ARM CoreSight Debug System.

External Memory

The PS can interface to many types of external memories through dedicated memory controllers. The dynamic memory controller supports DDR3, DDR3L, DDR4, LPDDR3, and LPDDR4 memories. The multi-protocol DDR memory controller can be configured to access a 2GB address space in 32-bit addressing mode and up to 32GB in 64-bit addressing mode using a single or dual rank configuration of 8-bit, 16-bit, or 32-bit DRAM memories. Both 32-bit and 64-bit bus access modes are protected by ECC using extra bits.

The SD/eMMC controller supports 1 and 4 bit data interfaces at low, default, high-speed, and ultra-high-speed (UHS) clock rates. This controller also supports 1-, 4-, or 8-bit-wide eMMC interfaces that are compliant to the eMMC 4.51 specification. eMMC is one of the primary boot and configuration modes for Zynq UltraScale+ MPSoCs and supports boot from managed NAND devices. The controller has a built-in DMA for enhanced performance.

The Quad-SPI controller is one of the primary boot and configuration devices. It supports 4-byte and 3-byte addressing modes. In both addressing modes, single, dual-stacked, and dual-parallel configurations are supported. Single mode supports a quad serial NOR flash memory, while in double stacked and double parallel modes, it supports two quad serial NOR flash memories.

The NAND controller is based on ONFI3.1 specification. It has an 8-pin interface and provides 200Mb/s of bandwidth in synchronous mode. It supports 24 bits of ECC thus enabling support for SLC NAND memories. It has two chip-selects to support deeper memory and a built-in DMA for enhanced performance.

General Connectivity

There are many peripherals in the PS for connecting to external devices over industry standard protocols, including CAN2.0B, USB, Ethernet, I2C, and UART. Many of the peripherals support clock gating and power gating modes to reduce dynamic and static power consumption.

USB 3.0/2.0

The pair of USB controllers can be configured as host, device, or On-The-Go (OTG). The core is compliant to USB 3.0 specification and supports super, high, full, and low speed modes in all configurations. In host mode, the USB controller is compliant with the Intel XHCI specification. In device mode, it supports up to 12 end points. While operating in USB 3.0 mode, the controller uses the serial transceiver and operates up to 5.0Gb/s. In USB 2.0 mode, the Universal Low Peripheral Interface (ULPI) is used to connect the controller to an external PHY operating up to 480Mb/s. The ULPI is also connected in USB 3.0 mode to support high-speed operations.

Ethernet MAC

The four tri-speed ethernet MACs support 10Mb/s, 100Mb/s, and 1Gb/s operations. The MACs support jumbo frames and time stamping through the interfaces based on IEEE Std 1588v2. The ethernet MACs can be connected through the serial transceivers (SGMII), the MIO (RGMII), or through EMIO (GMII). The GMII interface can be converted to a different interface within the PL.

High-Speed Connectivity

The PS includes four PS-GTR transceivers (transmit and receive), supporting data rates up to 6.0Gb/s and can interface to the peripherals for communication over PCIe, SATA, USB 3.0, SGMII, and DisplayPort.

PCIe

The integrated block for PCIe is compliant with PCI Express base specification 2.1 and supports x1, x2, and x4 configurations as root complex or end point, compliant to transaction ordering rules in both configurations. It has built-in DMA, supports one virtual channel and provides fully configurable base address registers.

SATA

Users can connect up to two external devices using the two SATA host port interfaces compliant to the SATA 3.1 specification. The SATA interfaces can operate at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates and are compliant with advanced host controller interface (AHCI) version 1.3 supporting partial and slumber power modes.

DisplayPort

The DisplayPort controller supports up to two lanes of source-only DisplayPort compliant with VESA DisplayPort v1.2a specification (source only) at 1.62Gb/s, 2.7Gb/s, and 5.4Gb/s data rates. The controller supports single stream transport (SST); video resolution up to 4Kx2K at a 30Hz frame rate; video formats Y-only, YCbCr444, YCbCr422, YCbCr420, RGB, YUV444, YUV422, xvYCC, and pixel color depth of 6, 8, 10, and 12 bits per color component.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100 Ω internal resistor. All UltraScale devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. UltraScale+ families add support for MIPI with a dedicated D-PHY in the I/O bank.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

High-Speed Serial Transceivers

Serial data transmission between devices on the same PCB, over backplanes, and across even longer distances is becoming increasingly important for scaling to 100Gb/s and 400Gb/s line cards. Specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues are required at these high data rates.

Three types of transceivers are used in the UltraScale architecture: GTH and GTY in FPGAs and MPSoC PL, and PS-GTR in the MPSoC PS. All transceivers are arranged in groups of four, known as a transceiver Quad. Each serial transceiver is a combined transmitter and receiver. [Table 17](#) compares the available transceivers.

Table 17: Transceiver Information

	Kintex UltraScale		Kintex UltraScale+		Virtex UltraScale		Virtex UltraScale+	Zynq UltraScale+		
Type	GTH	GTY	GTH	GTY	GTH	GTY	GTY	PS-GTR	GTH	GTY
Qty	16–64	0–32	20–60	0–60	20–60	0–60	40–128	4	0–44	0–28
Max. Data Rate	16.3Gb/s	16.3Gb/s	16.3Gb/s	32.75Gb/s	16.3Gb/s	30.5Gb/s	32.75Gb/s	6.0Gb/s	16.3Gb/s	32.75Gb/s
Min. Data Rate	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	1.25Gb/s	0.5Gb/s	0.5Gb/s
Key Apps	<ul style="list-style-type: none"> Backplane PCIe Gen4 HMC 	<ul style="list-style-type: none"> Backplane PCIe Gen4 HMC 	<ul style="list-style-type: none"> Backplane PCIe Gen4 HMC 	<ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC 	<ul style="list-style-type: none"> Backplane PCIe Gen4 HMC 	<ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC 	<ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC 	<ul style="list-style-type: none"> PCIe Gen2 USB Ethernet 	<ul style="list-style-type: none"> Backplane PCIe Gen4 HMC 	<ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC

The following information in this section pertains to the GTH and GTY only.

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Cache Coherent Interconnect for Accelerators (CCIX)

CCIX is a chip-to-chip interconnect operating at data rates up to 25Gb/s that allows two or more devices to share memory in a cache coherent manner. Using PCIe for the transport layer, CCIX can operate at several standard data rates (2.5, 5, 8, and 16Gb/s) with an additional high-speed 25Gb/s option. The specification employs a subset of full coherency protocols and ensures that FPGAs used as accelerators can coherently share data with processors using different instruction set architectures.

Virtex UltraScale+ HBM devices support CCIX data rates up to 16Gb/s and contain four CCIX ports and at least four integrated blocks for PCIe. Each CCIX port requires the use of one integrated block for PCIe. If not used with a CCIX port, the integrated blocks for PCIe can still be used for PCIe communication.

Integrated Block for Interlaken

Some UltraScale architecture-based devices include integrated blocks for Interlaken. Interlaken is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gb/s to 150Gb/s. The Interlaken integrated block in the UltraScale architecture is compliant to revision 1.2 of the Interlaken specification with data striping and de-striping across 1 to 12 lanes. Permitted configurations are: 1 to 12 lanes at up to 12.5Gb/s and 1 to 6 lanes at up to 25.78125Gb/s, enabling flexible support for up to 150Gb/s per integrated block. With multiple Interlaken blocks, certain UltraScale devices enable easy, reliable Interlaken switches and bridges.

Integrated Block for 100G Ethernet

Compliant to the IEEE Std 802.3ba, the 100G Ethernet integrated blocks in the UltraScale architecture provide low latency 100Gb/s Ethernet ports with a wide range of user customization and statistics gathering. With support for 10 x 10.3125Gb/s (CAUI) and 4 x 25.78125Gb/s (CAUI-4) configurations, the integrated block includes both the 100G MAC and PCS logic with support for IEEE Std 1588v2 1-step and 2-step hardware timestamping.

In UltraScale+ devices, the 100G Ethernet blocks contain a Reed Solomon Forward Error Correction (RS-FEC) block, compliant to IEEE Std 802.3bj, that can be used with the Ethernet block or stand alone in user applications. These families also support OTN mapping mode in which the PCS can be operated without using the MAC.

Stacked Silicon Interconnect (SSI) Technology

Many challenges associated with creating high-capacity devices are addressed by Xilinx with the second generation of the pioneering 3D SSI technology. SSI technology enables multiple super-logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders, to create a single device with more than 20,000 low-power inter-SLR connections. Dedicated interface tiles within the SLRs provide ultra-high bandwidth, low latency connectivity to other SLRs. Table 19 shows the number of SLRs in devices that use SSI technology and their dimensions.

Table 19: UltraScale and UltraScale+ 3D IC SLR Count and Dimensions

	Kintex UltraScale		Virtex UltraScale				Virtex UltraScale+								
Device	KU085	KU115	VU125	VU160	VU190	VU440	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
# SLRs	2	2	2	3	3	3	2	2	3	3	4	1	1	2	3
SLR Width (in regions)	6	6	6	6	6	9	6	6	6	8	8	8	8	8	8
SLR Height (in regions)	5	5	5	5	5	5	5	5	5	4	4	4	4	4	4

Clock Management

The clock generation and distribution components in UltraScale devices are located adjacent to the columns that contain the memory interface and input and output circuitry. This tight coupling of clocking and I/O provides low-latency clocking to the I/O for memory interfaces and other I/O protocols. Within every clock management tile (CMT) resides one mixed-mode clock manager (MMCM), two PLLs, clock distribution buffers and routing, and dedicated circuitry for implementing external memory interfaces.

Mixed-Mode Clock Manager

The mixed-mode clock manager (MMCM) can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of the MMCM is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers (D, M, and O) that are programmable by configuration and during normal operation via the Dynamic Reconfiguration Port (DRP). The pre-divider D reduces the input frequency and feeds one input of the phase/frequency comparator. The feedback divider M acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each phase can be selected to drive one of the output dividers, and each divider is programmable by configuration to divide by any integer from 1 to 128.

The MMCM has three input-jitter filter options: low bandwidth, high bandwidth, or optimized mode. Low-Bandwidth mode has the best jitter attenuation. High-Bandwidth mode has the best phase offset. Optimized mode allows the tools to find the best setting.

Block RAM

Every UltraScale architecture-based device contains a number of 36 Kb block RAMs, each with two completely independent ports that share only the stored data. Each block RAM can be configured as one 36Kb RAM or two independent 18Kb RAMs. Each memory access, read or write, is controlled by the clock. Connections in every block RAM column enable signals to be cascaded between vertically adjacent block RAMs, providing an easy method to create large, fast memory arrays, and FIFOs with greatly reduced power consumption.

All inputs, data, address, clock enables, and write enables are registered. The input address is always clocked (unless address latching is turned off), retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency. During a write operation, the data output can reflect either the previously stored data or the newly written data, or it can remain unchanged. Block RAM sites that remain unused in the user design are automatically powered down to reduce total power consumption. There is an additional pin on every block RAM to control the dynamic power gating feature.

Programmable Data Width

Each port can be configured as $32K \times 1$; $16K \times 2$; $8K \times 4$; $4K \times 9$ (or 8); $2K \times 18$ (or 16); $1K \times 36$ (or 32); or 512×72 (or 64). Whether configured as block RAM or FIFO, the two ports can have different aspect ratios without any constraints. Each block RAM can be divided into two completely independent 18Kb block RAMs that can each be configured to any aspect ratio from $16K \times 1$ to 512×36 . Everything described previously for the full 36Kb block RAM also applies to each of the smaller 18Kb block RAMs. Only in simple dual-port (SDP) mode can data widths of greater than 18bits (18Kb RAM) or 36 bits (36Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72. Both sides of the dual-port 36Kb RAM can be of variable width.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

Each block RAM can be configured as a 36Kb FIFO or an 18Kb FIFO. The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, programmable full, and programmable empty. The programmable flags allow the user to specify the FIFO counter values that make these flags go active. The FIFO width and depth are programmable with support for different read port and write port widths on a single FIFO. A dedicated cascade path allows for easy creation of deeper FIFOs.

Zynq UltraScale+ MPSoCs contain an additional System Monitor block in the PS. See [Table 20](#).

Table 20: Key System Monitor Features

	Kintex UltraScale Virtex UltraScale	Kintex UltraScale+ Virtex UltraScale+ Zynq UltraScale+ MPSoC PL	Zynq UltraScale+ MPSoC PS
ADC	10-bit 200kSPS	10-bit 200kSPS	10-bit 1MSPS
Interfaces	JTAG, I2C, DRP	JTAG, I2C, DRP, PMBus	APB

In FPGAs and the MPSoC PL, sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, PMBus, or I2C interfaces. The I2C interface and PMBus allow the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

The System Monitor in the MPSoC PS uses a 10-bit, 1 mega-sample-per-second (MSPS) ADC to digitize the sensor outputs. The measurements are stored in registers and are accessed via the Advanced Peripheral Bus (APB) interface by the processors and the platform management unit (PMU) in the PS.

Configuration

The UltraScale architecture-based devices store their customized configuration in SRAM-type internal latches. The configuration storage is volatile and must be reloaded whenever the device is powered up. This storage can also be reloaded at any time. Several methods and data formats for loading configuration are available, determined by the mode pins, with more dedicated configuration datapath pins to simplify the configuration process.

UltraScale architecture-based devices support secure and non-secure boot with optional Advanced Encryption Standard - Galois/Counter Mode (AES-GCM) decryption and authentication logic. If only authentication is required, the UltraScale architecture provides an alternative form of authentication in the form of RSA algorithms. For RSA authentication support in the Kintex UltraScale and Virtex UltraScale families, go to [UG570](#), *UltraScale Architecture Configuration User Guide*.

UltraScale architecture-based devices also have the ability to select between multiple configurations, and support robust field-update methodologies. This is especially useful for updates to a design after the end product has been shipped. Designers can release their product with an early version of the design, thus getting their product to market faster. This feature allows designers to keep their customers current with the most up-to-date design while the product is already deployed in the field.

Booting MPSoCs

Zynq UltraScale+ MPSoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the AES-GCM, SHA-3/384 decryption/authentication, and 4096-bit RSA blocks decrypt and authenticate the image.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NAND, Quad-SPI, SD, eMMC, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. One of the CPUs, Cortex-A53 or Cortex-R5, executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip memory (OCM).

Date	Version	Description of Revisions
02/06/2014	1.1	Updated PCIe information in Table 1 and Table 3 . Added FFVJ1924 package to Table 8 .
12/10/2013	1.0	Initial Xilinx release.