# AMD Xilinx - XCKU15P-3FFVA1156E Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 65340 |
| Number of Logic Elements/Cells | 1143450 |
| Total RAM Bits | 82329600 |
| Number of I/O | 516 |
| Number of Gates | - |
| Voltage - Supply | 0.873V ~ 0.927V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 1156-BBGA, FCBGA |
| Supplier Device Package | 1156-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcku15p-3ffva1156e |

# Summary of Features

## Processing System Overview

UltraScale+ MPSoCs feature dual and quad core variants of the ARM Cortex-A53 (APU) with dual-core ARM Cortex-R5 (RPU) processing system (PS). Some devices also include a dedicated ARM Mali™-400 MP2 graphics processing unit (GPU). See Table 2.

*Table 2:* **Zynq UltraScale+ MPSoC Device Features**

| | CG Devices | EG Devices | EV Devices |
|---|---|---|---|
| APU | Dual-core ARM Cortex-A53 | Quad-core ARM Cortex-A53 | Quad-core ARM Cortex-A53 |
| RPU | Dual-core ARM Cortex-R5 | Dual-core ARM Cortex-R5 | Dual-core ARM Cortex-R5 |
| GPU | – | Mali-400MP2 | Mali-400MP2 |
| VCU | – | – | H.264/H.265 |

To support the processors' functionality, a number of peripherals with dedicated functions are included in the PS. For interfacing to external memories for data or configuration storage, the PS includes a multi-protocol dynamic memory controller, a DMA controller, a NAND controller, an SD/eMMC controller and a Quad SPI controller. In addition to interfacing to external memories, the APU also includes a Level-1 (L1) and Level-2 (L2) cache hierarchy; the RPU includes an L1 cache and Tightly Coupled memory subsystem. Each has access to a 256KB on-chip memory.

For high-speed interfacing, the PS includes 4 channels of transmit (TX) and receive (RX) pairs of transceivers, called PS-GTR transceivers, supporting data rates of up to 6.0Gb/s. These transceivers can interface to the high-speed peripheral blocks to support PCIe Gen2 root complex or end point in x1, x2, or x4 configurations; Serial-ATA (SATA) at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates; and up to two lanes of Display Port at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s data rates. The PS-GTR transceivers can also interface to components over USB 3.0 and Serial Gigabit Media Independent Interface (SGMII).

For general connectivity, the PS includes: a pair of USB 2.0 controllers, which can be configured as host, device, or On-The-Go (OTG); an I2C controller; a UART; and a CAN2.0B controller that conforms to ISO11898-1. There are also four triple speed Ethernet MACs and 128 bits of GPIO, of which 78 bits are available through the MIO and 96 through the EMIO.

High-bandwidth connectivity based on the ARM AMBA® AXI4 protocol connects the processing units with the peripherals and provides interface between the PS and the programmable logic (PL).

For additional information, go to: DS891, *Zynq UltraScale+ MPSoC Overview*.

## I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken

Data is transported on and off chip through a combination of the high-performance parallel SelectIO™ interface and high-speed serial transceiver connectivity. I/O blocks provide support for cutting-edge memory interface and network protocols through flexible I/O standard and voltage support. The serial transceivers in the UltraScale architecture-based devices transfer data up to 32.75Gb/s, enabling 25G+ backplane designs with dramatically lower power per bit than previous generation transceivers. All transceivers, except the PS-GTR, support the required data rates for PCIe Gen3, and Gen4 (rev 0.5), and integrated blocks for PCIe enable UltraScale devices to support up to Gen4 x8 and Gen3 x16 Endpoint and Root Port designs. Integrated blocks for 150Gb/s Interlaken and 100Gb/s Ethernet (100G MAC/PCS) extend the capabilities of UltraScale devices, enabling simple, reliable support for Nx100G switch and bridge applications. Virtex UltraScale+ HBM devices include Cache Coherent Interconnect for Accelerators (CCIX) ports for coherently sharing data with different processors.

## Clocks and Memory Interfaces

UltraScale devices contain powerful clock management circuitry, including clock synthesis, buffering, and routing components that together provide a highly capable framework to meet design requirements. The clock network allows for extremely flexible distribution of clocks to minimize the skew, power consumption, and delay associated with clock signals. The clock management technology is tightly integrated with dedicated memory interface circuitry to enable support for high-performance external memories, including DDR4. In addition to parallel memory interfaces, UltraScale devices support serial memories, such as hybrid memory cube (HMC).

## Routing, SSI, Logic, Storage, and Signal Processing

Configurable Logic Blocks (CLBs) containing 6-input look-up tables (LUTs) and flip-flops, DSP slices with 27x18 multipliers, 36Kb block RAMs with built-in FIFO and ECC support, and 4Kx72 UltraRAM blocks (in UltraScale+ devices) are all connected with an abundance of high-performance, low-latency interconnect. In addition to logical functions, the CLB provides shift register, multiplexer, and carry logic functionality as well as the ability to configure the LUTs as distributed memory to complement the highly capable and configurable block RAMs. The DSP slice, with its 96-bit-wide XOR functionality, 27-bit pre-adder, and 30-bit A input, performs numerous independent functions including multiply accumulate, multiply add, and pattern detect. In addition to the device interconnect, in devices using SSI technology, signals can cross between super-logic regions (SLRs) using dedicated, low-latency interface tiles. These combined routing resources enable easy support for next-generation bus data widths. Virtex UltraScale+ HBM devices include up to 8GB of high bandwidth memory.

## Configuration, Encryption, and System Monitoring

The configuration and encryption block performs numerous device-level functions critical to the successful operation of the FPGA or MPSoC. This high-performance configuration block enables device configuration from external media through various protocols, including PCIe, often with no requirement to use multi-function I/O pins during configuration. The configuration block also provides 256-bit AES-GCM decryption capability at the same performance as unencrypted configuration. Additional features include SEU detection and correction, partial reconfiguration support, and battery-backed RAM or eFUSE technology for AES key storage to provide additional security. The System Monitor enables the monitoring of the physical environment via on-chip temperature and supply sensors and can also monitor up to 17 external analog inputs. With UltraScale+ MPSoCs, the device is booted via the Configuration and Security Unit (CSU), which supports secure boot via the 256-bit AES-GCM and SHA/384 blocks. The cryptographic engines in the CSU can be used in the MPSoC after boot for user encryption.

# Kintex UltraScale FPGA Feature Summary

*Table 3:* **Kintex UltraScale FPGA Feature Summary**

| | KU025[1] | KU035 | KU040 | KU060 | KU085 | KU095 | KU115 |
|---|---|---|---|---|---|---|---|
| System Logic Cells | 318,150 | 444,343 | 530,250 | 725,550 | 1,088,325 | 1,176,000 | 1,451,100 |
| CLB Flip-Flops | 290,880 | 406,256 | 484,800 | 663,360 | 995,040 | 1,075,200 | 1,326,720 |
| CLB LUTs | 145,440 | 203,128 | 242,400 | 331,680 | 497,520 | 537,600 | 663,360 |
| Maximum Distributed RAM (Mb) | 4.1 | 5.9 | 7.0 | 9.1 | 13.4 | 4.7 | 18.3 |
| Block RAM Blocks | 360 | 540 | 600 | 1,080 | 1,620 | 1,680 | 2,160 |
| Block RAM (Mb) | 12.7 | 19.0 | 21.1 | 38.0 | 56.9 | 59.1 | 75.9 |
| CMTs (1 MMCM, 2 PLLs) | 6 | 10 | 10 | 12 | 22 | 16 | 24 |
| I/O DLLs | 24 | 40 | 40 | 48 | 56 | 64 | 64 |
| Maximum HP I/Os(2) | 208 | 416 | 416 | 520 | 572 | 650 | 676 |
| Maximum HR I/Os(3) | 104 | 104 | 104 | 104 | 104 | 52 | 156 |
| DSP Slices | 1,152 | 1,700 | 1,920 | 2,760 | 4,100 | 768 | 5,520 |
| System Monitor | 1 | 1 | 1 | 1 | 2 | 1 | 2 |
| PCIe Gen3 x8 | 1 | 2 | 3 | 3 | 4 | 4 | 6 |
| 150G Interlaken | 0 | 0 | 0 | 0 | 0 | 2 | 0 |
| 100G Ethernet | 0 | 0 | 0 | 0 | 0 | 2 | 0 |
| GTH 16.3Gb/s Transceivers(4) | 12 | 16 | 20 | 32 | 56 | 32 | 64 |
| GTY 16.3Gb/s Transceivers(5) | 0 | 0 | 0 | 0 | 0 | 32 | 0 |
| Transceiver Fractional PLLs | 0 | 0 | 0 | 0 | 0 | 16 | 0 |

**Notes:**

1. Certain advanced configuration features are not supported in the KU025. Refer to the Configuring FPGAs section for details.
2. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
3. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
4. GTH transceivers in SF/FB packages support data rates up to 12.5Gb/s. See Table 4.
5. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s. See Table 4.

# Kintex UltraScale+ FPGA Feature Summary

*Table 5:* **Kintex UltraScale+ FPGA Feature Summary**

| | KU3P | KU5P | KU9P | KU11P | KU13P | KU15P |
|---|---|---|---|---|---|---|
| System Logic Cells | 355,950 | 474,600 | 599,550 | 653,100 | 746,550 | 1,143,450 |
| CLB Flip-Flops | 325,440 | 433,920 | 548,160 | 597,120 | 682,560 | 1,045,440 |
| CLB LUTs | 162,720 | 216,960 | 274,080 | 298,560 | 341,280 | 522,720 |
| Max. Distributed RAM (Mb) | 4.7 | 6.1 | 8.8 | 9.1 | 11.3 | 9.8 |
| Block RAM Blocks | 360 | 480 | 912 | 600 | 744 | 984 |
| Block RAM (Mb) | 12.7 | 16.9 | 32.1 | 21.1 | 26.2 | 34.6 |
| UltraRAM Blocks | 48 | 64 | 0 | 80 | 112 | 128 |
| UltraRAM (Mb) | 13.5 | 18.0 | 0 | 22.5 | 31.5 | 36.0 |
| CMTs (1 MMCM and 2 PLLs) | 4 | 4 | 4 | 8 | 4 | 11 |
| Max. HP I/O(1) | 208 | 208 | 208 | 416 | 208 | 572 |
| Max. HD I/O(2) | 96 | 96 | 96 | 96 | 96 | 96 |
| DSP Slices | 1,368 | 1,824 | 2,520 | 2,928 | 3,528 | 1,968 |
| System Monitor | 1 | 1 | 1 | 1 | 1 | 1 |
| GTH Transceiver 16.3Gb/s | 0 | 0 | 28 | 32 | 28 | 44 |
| GTY Transceivers 32.75Gb/s(3) | 16 | 16 | 0 | 20 | 0 | 32 |
| Transceiver Fractional PLLs | 8 | 8 | 14 | 26 | 14 | 38 |
| PCIe Gen3 x16 and Gen4 x8 | 1 | 1 | 0 | 4 | 0 | 5 |
| 150G Interlaken | 0 | 0 | 0 | 1 | 0 | 4 |
| 100G Ethernet w/RS-FEC | 0 | 1 | 0 | 2 | 0 | 4 |

**Notes:**

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTY transceiver line rates are package limited: SFVB784 to 12.5Gb/s; FFVA676, FFVD900, and FFVA1156 to 16.3Gb/s. See Table 6.

# Virtex UltraScale FPGA Feature Summary

*Table 7:* **Virtex UltraScale FPGA Feature Summary**

| | VU065 | VU080 | VU095 | VU125 | VU160 | VU190 | VU440 |
|---|---|---|---|---|---|---|---|
| System Logic Cells | 783,300 | 975,000 | 1,176,000 | 1,566,600 | 2,026,500 | 2,349,900 | 5,540,850 |
| CLB Flip-Flops | 716,160 | 891,424 | 1,075,200 | 1,432,320 | 1,852,800 | 2,148,480 | 5,065,920 |
| CLB LUTs | 358,080 | 445,712 | 537,600 | 716,160 | 926,400 | 1,074,240 | 2,532,960 |
| Maximum Distributed RAM (Mb) | 4.8 | 3.9 | 4.8 | 9.7 | 12.7 | 14.5 | 28.7 |
| Block RAM Blocks | 1,260 | 1,421 | 1,728 | 2,520 | 3,276 | 3,780 | 2,520 |
| Block RAM (Mb) | 44.3 | 50.0 | 60.8 | 88.6 | 115.2 | 132.9 | 88.6 |
| CMT (1 MMCM, 2 PLLs) | 10 | 16 | 16 | 20 | 28 | 30 | 30 |
| I/O DLLs | 40 | 64 | 64 | 80 | 120 | 120 | 120 |
| Maximum HP I/Os(1) | 468 | 780 | 780 | 780 | 650 | 650 | 1,404 |
| Maximum HR I/Os(2) | 52 | 52 | 52 | 104 | 52 | 52 | 52 |
| DSP Slices | 600 | 672 | 768 | 1,200 | 1,560 | 1,800 | 2,880 |
| System Monitor | 1 | 1 | 1 | 2 | 3 | 3 | 3 |
| PCIe Gen3 x8 | 2 | 4 | 4 | 4 | 4 | 6 | 6 |
| 150G Interlaken | 3 | 6 | 6 | 6 | 8 | 9 | 0 |
| 100G Ethernet | 3 | 4 | 4 | 6 | 9 | 9 | 3 |
| GTH 16.3Gb/s Transceivers | 20 | 32 | 32 | 40 | 52 | 60 | 48 |
| GTY 30.5Gb/s Transceivers | 20 | 32 | 32 | 40 | 52 | 60 | 0 |
| Transceiver Fractional PLLs | 10 | 16 | 16 | 20 | 26 | 30 | 0 |

**Notes:**

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

# Zynq UltraScale+: CG Device Feature Summary

*Table 11:* **Zynq UltraScale+: CG Device Feature Summary**

| | ZU2CG | ZU3CG | ZU4CG | ZU5CG | ZU6CG | ZU7CG | ZU9CG |
|---|---|---|---|---|---|---|---|
| Application Processing Unit | Dual-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache | | | | | | |
| Real-Time Processing Unit | Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM | | | | | | |
| Embedded and External Memory | 256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC | | | | | | |
| General Connectivity | 214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters | | | | | | |
| High-Speed Connectivity | 4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII | | | | | | |
| System Logic Cells | 103,320 | 154,350 | 192,150 | 256,200 | 469,446 | 504,000 | 599,550 |
| CLB Flip-Flops | 94,464 | 141,120 | 175,680 | 234,240 | 429,208 | 460,800 | 548,160 |
| CLB LUTs | 47,232 | 70,560 | 87,840 | 117,120 | 214,604 | 230,400 | 274,080 |
| Distributed RAM (Mb) | 1.2 | 1.8 | 2.6 | 3.5 | 6.9 | 6.2 | 8.8 |
| Block RAM Blocks | 150 | 216 | 128 | 144 | 714 | 312 | 912 |
| Block RAM (Mb) | 5.3 | 7.6 | 4.5 | 5.1 | 25.1 | 11.0 | 32.1 |
| UltraRAM Blocks | 0 | 0 | 48 | 64 | 0 | 96 | 0 |
| UltraRAM (Mb) | 0 | 0 | 14.0 | 18.0 | 0 | 27.0 | 0 |
| DSP Slices | 240 | 360 | 728 | 1,248 | 1,973 | 1,728 | 2,520 |
| CMTs | 3 | 3 | 4 | 4 | 4 | 8 | 4 |
| Max. HP I/O(1) | 156 | 156 | 156 | 156 | 208 | 416 | 208 |
| Max. HD I/O(2) | 96 | 96 | 96 | 96 | 120 | 48 | 120 |
| System Monitor | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| GTH Transceiver 16.3Gb/s(3) | 0 | 0 | 16 | 16 | 24 | 24 | 24 |
| GTY Transceivers 32.75Gb/s | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Transceiver Fractional PLLs | 0 | 0 | 8 | 8 | 12 | 12 | 12 |
| PCIe Gen3 x16 and Gen4 x8 | 0 | 0 | 2 | 2 | 0 | 2 | 0 |
| 150G Interlaken | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 100G Ethernet w/ RS-FEC | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Notes:**

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See Table 12.

## Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

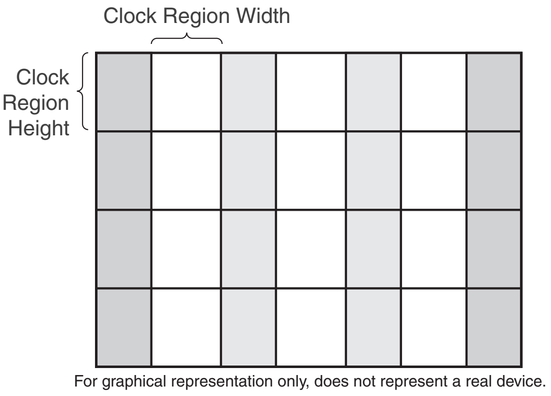
*Table 14:* **Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os**

| Package (1)(2)(3)(4)(5) | Package Dimensions (mm) | ZU2EG | ZU3EG | ZU4EG | ZU5EG | ZU6EG | ZU7EG | ZU9EG | ZU11EG | ZU15EG | ZU17EG | ZU19EG |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY |
| SBVA484(6) | 19x19 | 24, 58<br>0, 0 | 24, 58<br>0, 0 | | | | | | | | | |
| SFVA625 | 21x21 | 24, 156<br>0, 0 | 24, 156<br>0, 0 | | | | | | | | | |
| SFVC784(7) | 23x23 | 96, 156<br>0, 0 | 96, 156<br>0, 0 | 96, 156<br>4, 0 | 96, 156<br>4, 0 | | | | | | | |
| FBVB900 | 31x31 | | | 48, 156<br>16, 0 | 48, 156<br>16, 0 | | 48, 156<br>16, 0 | | | | | |
| FFVC900 | 31x31 | | | | | 48, 156<br>16, 0 | | 48, 156<br>16, 0 | | 48, 156<br>16, 0 | | |
| FFVB1156 | 35x35 | | | | | 120, 208<br>24, 0 | | 120, 208<br>24, 0 | | 120, 208<br>24, 0 | | |
| FFVC1156 | 35x35 | | | | | | 48, 312<br>20, 0 | | 48, 312<br>20, 0 | | | |
| FFVB1517 | 40x40 | | | | | | | | 72, 416<br>16, 0 | | 72, 572<br>16, 0 | 72, 572<br>16, 0 |
| FFVF1517 | 40x40 | | | | | | 48, 416<br>24, 0 | | 48, 416<br>32, 0 | | | |
| FFVC1760 | 42.5x42.5 | | | | | | | | 96, 416<br>32, 16 | | 96, 416<br>32, 16 | 96, 416<br>32, 16 |
| FFVD1760 | 42.5x42.5 | | | | | | | | | | 48, 260<br>44, 28 | 48, 260<br>44, 28 |
| FFVE1924 | 45x45 | | | | | | | | | | 96, 572<br>44, 0 | 96, 572<br>44, 0 |

**Notes:**

1. Go to Ordering Information for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. All device package combinations bond out 214 PS I/O except ZU2EG and ZU3EG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
5. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
6. All 58 HP I/O pins are powered by the same $V_{CCO}$ supply.
7. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. Figure 2 is a representation of an FPGA divided into regions.



For graphical representation only, does not represent a real device.

DS890_02_121014

*Figure 2:* **Column-Based FPGA Divided into Clock Regions**

# Processing System (PS)

Zynq UltraScale+ MPSoCs consist of a PS coupled with programmable logic. The contents of the PS varies between the different Zynq UltraScale+ devices. All devices contain an APU, an RPU, and many peripherals for connecting the multiple processing engines to external components. The EG and EV devices contain a GPU and the EV devices contain a video codec unit (VCU). The components of the PS are connected together and to the PL through a multi-layered ARM AMBA AXI non-blocking interconnect that supports multiple simultaneous master-slave transactions. Traffic through the interconnect can be regulated by the quality of service (QoS) block in the interconnect. Twelve dedicated AXI 32-bit, 64-bit, or 128-bit ports connect the PL to high-speed interconnect and DDR in the PS via a FIFO interface.

There are four independently controllable power domains: the PL plus three within the PS (full power, lower power, and battery power domains). Additionally, many peripherals support clock gating and power gating to further reduce dynamic and static power consumption.

## Application Processing Unit (APU)

The APU has a feature-rich dual-core or quad-core ARM Cortex-A53 processor. Cortex-A53 cores are 32-bit/64-bit application processors based on ARM-v8A architecture, offering the best performance-to-power ratio. The ARMv8 architecture supports hardware virtualization. Each of the Cortex-A53 cores has: 32KB of instruction and data L1 caches, with parity and ECC protection respectively; a NEON SIMD engine; and a single and double precision floating point unit. In addition to these blocks, the APU consists of a snoop control unit and a 1MB L2 cache with ECC protection to enhance system-level performance. The snoop control unit keeps the L1 caches coherent thus eliminating the need of spending software bandwidth for coherency. The APU also has a built-in interrupt controller supporting virtual interrupts. The APU communicates to the rest of the PS through 128-bit AXI coherent extension (ACE) port via Cache Coherent Interconnect (CCI) block, using the System Memory Management Unit (SMMU). The APU is also connected to the Programmable Logic (PL), through the 128-bit accelerator coherency port

(ACP), providing a low latency coherent port for accelerators in the PL. To support real-time debug and trace, each core also has an Embedded Trace Macrocell (ETM) that communicates with the ARM CoreSight™ Debug System.

## Real-Time Processing Unit (RPU)

The RPU in the PS contains a dual-core ARM Cortex-R5 PS. Cortex-R5 cores are 32-bit real-time processor cores based on ARM-v7R architecture. Each of the Cortex-R5 cores has 32KB of level-1 (L1) instruction and data cache with ECC protection. In addition to the L1 caches, each of the Cortex-R5 cores also has a 128KB tightly coupled memory (TCM) interface for real-time single cycle access. The RPU also has a dedicated interrupt controller. The RPU can operate in either split or lock-step mode. In split mode, both processors run independently of each other. In lock-step mode, they run in parallel with each other, with integrated comparator logic, and the TCMs are used as 256KB unified memory. The RPU communicates with the rest of the PS via the 128-bit AXI-4 ports connected to the low power domain switch. It also communicates directly with the PL through 128-bit low latency AXI-4 ports. To support real-time debug and trace each core also has an embedded trace macrocell (ETM) that communicates with the ARM CoreSight Debug System.

## External Memory

The PS can interface to many types of external memories through dedicated memory controllers. The dynamic memory controller supports DDR3, DDR3L, DDR4, LPDDR3, and LPDDR4 memories. The multi-protocol DDR memory controller can be configured to access a 2GB address space in 32-bit addressing mode and up to 32GB in 64-bit addressing mode using a single or dual rank configuration of 8-bit, 16-bit, or 32-bit DRAM memories. Both 32-bit and 64-bit bus access modes are protected by ECC using extra bits.

The SD/eMMC controller supports 1 and 4 bit data interfaces at low, default, high-speed, and ultra-high-speed (UHS) clock rates. This controller also supports 1-, 4-, or 8-bit-wide eMMC interfaces that are compliant to the eMMC 4.51 specification. eMMC is one of the primary boot and configuration modes for Zynq UltraScale+ MPSoCs and supports boot from managed NAND devices. The controller has a built-in DMA for enhanced performance.

The Quad-SPI controller is one of the primary boot and configuration devices. It supports 4-byte and 3-byte addressing modes. In both addressing modes, single, dual-stacked, and dual-parallel configurations are supported. Single mode supports a quad serial NOR flash memory, while in double stacked and double parallel modes, it supports two quad serial NOR flash memories.

The NAND controller is based on ONFI3.1 specification. It has an 8-pin interface and provides 200Mb/s of bandwidth in synchronous mode. It supports 24 bits of ECC thus enabling support for SLC NAND memories. It has two chip-selects to support deeper memory and a built-in DMA for enhanced performance.

## I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards $V_{CCO}$ or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100Ω internal resistor. All UltraScale devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. UltraScale+ families add support for MIPI with a dedicated D-PHY in the I/O bank.

### *3-State Digitally Controlled Impedance and Low Power I/O Features*

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to $V_{CCO}$ or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

## I/O Logic

### *Input and Output Delay*

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

### *ISERDES and OSERDES*

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

# Integrated Interface Blocks for PCI Express Designs

The UltraScale architecture includes integrated blocks for PCIe technology that can be configured as an Endpoint or Root Port. UltraScale devices are compliant to the PCI Express Base Specification Revision 3.0. UltraScale+ devices are compliant to the PCI Express Base Specification Revision 3.1 for Gen3 and lower data rates, and compatible with the PCI Express Base Specification Revision 4.0 (rev 0.5) for Gen4 data rates.

The Root Port can be used to build the basis for a compatible Root Complex, to allow custom chip-to-chip communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the FPGA or MPSoC.

This block is highly configurable to system design requirements and can operate up to the maximum lane widths and data rates listed in Table 18.

*Table 18:* **PCIe Maximum Configurations**

| | Kintex UltraScale | Kintex UltraScale+ | Virtex UltraScale | Virtex UltraScale+ | Zynq UltraScale+ |
|---|---|---|---|---|---|
| Gen1 (2.5Gb/s) | x8 | x16 | x8 | x16 | x16 |
| Gen2 (5Gb/s) | x8 | x16 | x8 | x16 | x16 |
| Gen3 (8Gb/s) | x8 | x16 | x8 | x16 | x16 |
| Gen4 (16Gb/s)(1) | | x8 | | x8 | x8 |

**Notes:**

1. Transceivers in Kintex UltraScale and Virtex UltraScale devices are capable of operating at Gen4 data rates.

For high-performance applications, advanced buffering techniques of the block offer a flexible maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block for PCIe, the transceivers, block RAM, and clocking resources) into an Endpoint or Root Port solution. The system designer has control over many configurable parameters: link width and speed, maximum payload size, FPGA or MPSoC logic interface speeds, reference clock frequency, and base address register decoding and filtering.

# Stacked Silicon Interconnect (SSI) Technology

Many challenges associated with creating high-capacity devices are addressed by Xilinx with the second generation of the pioneering 3D SSI technology. SSI technology enables multiple super-logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders, to create a single device with more than 20,000 low-power inter-SLR connections. Dedicated interface tiles within the SLRs provide ultra-high bandwidth, low latency connectivity to other SLRs. Table 19 shows the number of SLRs in devices that use SSI technology and their dimensions.

*Table 19:* **UltraScale and UltraScale+ 3D IC SLR Count and Dimensions**

| | Kintex UltraScale | | Virtex UltraScale | | | | Virtex UltraScale+ | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Device | KU085 | KU115 | VU125 | VU160 | VU190 | VU440 | VU5P | VU7P | VU9P | VU11P | VU13P | VU31P | VU33P | VU35P | VU37P |
| # SLRs | 2 | 2 | 2 | 3 | 3 | 3 | 2 | 2 | 3 | 3 | 4 | 1 | 1 | 2 | 3 |
| SLR Width (in regions) | 6 | 6 | 6 | 6 | 6 | 9 | 6 | 6 | 6 | 8 | 8 | 8 | 8 | 8 | 8 |
| SLR Height (in regions) | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 4 | 4 | 4 | 4 | 4 | 4 |

# Clock Management

The clock generation and distribution components in UltraScale devices are located adjacent to the columns that contain the memory interface and input and output circuitry. This tight coupling of clocking and I/O provides low-latency clocking to the I/O for memory interfaces and other I/O protocols. Within every clock management tile (CMT) resides one mixed-mode clock manager (MMCM), two PLLs, clock distribution buffers and routing, and dedicated circuitry for implementing external memory interfaces.

## Mixed-Mode Clock Manager

The mixed-mode clock manager (MMCM) can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of the MMCM is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers (D, M, and O) that are programmable by configuration and during normal operation via the Dynamic Reconfiguration Port (DRP). The pre-divider D reduces the input frequency and feeds one input of the phase/frequency comparator. The feedback divider M acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each phase can be selected to drive one of the output dividers, and each divider is programmable by configuration to divide by any integer from 1 to 128.

The MMCM has three input-jitter filter options: low bandwidth, high bandwidth, or optimized mode. Low-Bandwidth mode has the best jitter attenuation. High-Bandwidth mode has the best phase offset. Optimized mode allows the tools to find the best setting.

The MMCM can have a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of 1/8 and can thus increase frequency synthesis capabilities by a factor of 8. The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency. At 1,600MHz, the phase-shift timing increment is 11.2ps.

### PLL

With fewer features than the MMCM, the two PLLs in a clock management tile are primarily present to provide the necessary clocks to the dedicated memory interface circuitry. The circuit at the center of the PLLs is similar to the MMCM, with PFD feeding a VCO and programmable M, D, and O counters. There are two divided outputs to the device fabric per PLL as well as one clock plus one enable signal to the memory interface circuitry.

UltraScale+ MPSoCs are equipped with five additional PLLs in the PS for independently configuring the four primary clock domains with the PS: the APU, the RPU, the DDR controller, and the I/O peripherals.

## Clock Distribution

Clocks are distributed throughout UltraScale devices via buffers that drive a number of vertical and horizontal tracks. There are 24 horizontal clock routes per clock region and 24 vertical clock routes per clock region with 24 additional vertical clock routes adjacent to the MMCM and PLL. Within a clock region, clock signals are routed to the device logic (CLBs, etc.) via 16 gateable leaf clocks.

Several types of clock buffers are available. The BUFGCE and BUFCE_LEAF buffers provide clock gating at the global and leaf levels, respectively. BUFGCTRL provides glitchless clock muxing and gating capability. BUFGCE_DIV has clock gating capability and can divide a clock by 1 to 8. BUFG_GT performs clock division from 1 to 8 for the transceiver clocks. In MPSoCs, clocks can be transferred from the PS to the PL using dedicated buffers.

## Memory Interfaces

Memory interface data rates continue to increase, driving the need for dedicated circuitry that enables high performance, reliable interfacing to current and next-generation memory technologies. Every UltraScale device includes dedicated physical interfaces (PHY) blocks located between the CMT and I/O columns that support implementation of high-performance PHY blocks to external memories such as DDR4, DDR3, QDRII+, and RLDRAM3. The PHY blocks in each I/O bank generate the address/control and data bus signaling protocols as well as the precision clock/data alignment required to reliably communicate with a variety of high-performance memory standards. Multiple I/O banks can be used to create wider memory interfaces.

As well as external parallel memory interfaces, UltraScale FPGAs and MPSoCs can communicate to external serial memories, such as Hybrid Memory Cube (HMC), via the high-speed serial transceivers. All transceivers in the UltraScale architecture support the HMC protocol, up to 15Gb/s line rates. UltraScale devices support the highest bandwidth HMC configuration of 64 lanes with a single FPGA.

After copying the FSBL to OCM, the processor executes the FSBL. Xilinx supplies example FSBLs or users can create their own. The FSBL initiates the boot of the PS and can load and configure the PL, or configuration of the PL can be deferred to a later stage. The FSBL typically loads either a user application or an optional second stage boot loader (SSBL) such as U-Boot. Users obtain example SSBL from Xilinx or a third party, or they can create their own SSBL. The SSBL continues the boot process by loading code from any of the primary boot devices or from other sources such as USB, Ethernet, etc. If the FSBL did not configure the PL, the SSBL can do so, or again, the configuration can be deferred to a later stage.

The static memory interface controller (NAND, eMMC, or Quad-SPI) is configured using default settings. To improve device configuration speed, these settings can be modified by information provided in the boot image header. The ROM boot image is not user readable or executable after boot.

## Configuring FPGAs

The SPI (serial NOR) interface (x1, x2, x4, and dual x4 modes) and the BPI (parallel NOR) interface (x8 and x16 modes) are two common methods used for configuring the FPGA. Users can directly connect an SPI or BPI flash to the FPGA, and the FPGA's internal configuration logic reads the bitstream out of the flash and configures itself, eliminating the need for an external controller. The FPGA automatically detects the bus width on the fly, eliminating the need for any external controls or switches. Bus widths supported are x1, x2, x4, and dual x4 for SPI, and x8 and x16 for BPI. The larger bus widths increase configuration speed and reduce the amount of time it takes for the FPGA to start up after power-on.

In master mode, the FPGA can drive the configuration clock from an internally generated clock, or for higher speed configuration, the FPGA can use an external configuration clock source. This allows high-speed configuration with the ease of use characteristic of master mode. Slave modes up to 32 bits wide that are especially useful for processor-driven configuration are also supported by the FPGA. In addition, the new media configuration access port (MCAP) provides a direct connection between the integrated block for PCIe and the configuration logic to simplify configuration over PCIe.

SEU detection and mitigation (SEM) IP, RSA authentication, post-configuration CRC, and Security Monitor (SecMon) IP are not supported in the KU025 FPGA.

# Packaging

The UltraScale devices are available in a variety of organic flip-chip and lidless flip-chip packages supporting different quantities of I/Os and transceivers. Maximum supported performance can depend on the style of package and its material. Always refer to the specific device data sheet for performance specifications by package type.

In flip-chip packages, the silicon device is attached to the package substrate using a high-performance flip-chip process. Decoupling capacitors are mounted on the package substrate to optimize signal integrity under simultaneous switching of outputs (SSO) conditions.

# Ordering Information

Table 21 shows the speed and temperature grades available in the different device families. $V_{CCINT}$ supply voltage is listed in parentheses.

*Table 21:* **Speed Grade and Temperature Grade**

| Device Family | Devices | Speed Grade and Temperature Grade | | | |
|---|---|---|---|---|---|
| | | Commercial (C) | Extended (E) | | Industrial (I) |
| | | 0°C to +85°C | 0°C to +100°C | 0°C to +110°C | –40°C to +100°C |
| Kintex UltraScale | All | | -3E(1) (1.0V) | | |
| | | | -2E (0.95V) | | -2I (0.95V) |
| | | -1C (0.95V) | | | -1I (0.95V) |
| | | | | | -1LI(1) (0.95V or 0.90V) |
| Kintex UltraScale+ | All | | -3E (0.90V) | | |
| | | | -2E (0.85V) | | -2I (0.85V) |
| | | | | -2LE(2) (0.85V or 0.72V) | |
| | | | -1E (0.85V) | | -1I (0.85V) |
| | | | | | -1LI (0.85V or 0.72V) |
| Virtex UltraScale | VU065<br>VU080<br>VU095<br>VU125<br>VU160<br>VU190 | | -3E (1.0V) | | |
| | | | -2E (0.95V) | | -2I (0.95V) |
| | | | -1HE (0.95V or 1.0V) | | -1I (0.95V) |
| | VU440 | | -3E (1.0V) | | |
| | | | -2E (0.95V) | | -2I (0.95V) |
| | | -1C (0.95V) | | | -1I (0.95V) |
| Virtex UltraScale+ | VU3P<br>VU5P<br>VU7P<br>VU9P<br>VU11P<br>VU13P | | -3E (0.90V) | | |
| | | | -2E (0.85V) | | -2I (0.85V) |
| | | | | -2LE(2) (0.85V or 0.72V) | |
| | | | -1E (0.85V) | | -1I (0.85V) |
| | VU31P<br>VU33P<br>VU35P<br>VU37P | | -3E (0.90V) | | |
| | | | -2E (0.85V) | | |
| | | | | -2LE(2) (0.85V or 0.72V) | |
| | | | -1E (0.85V) | | |

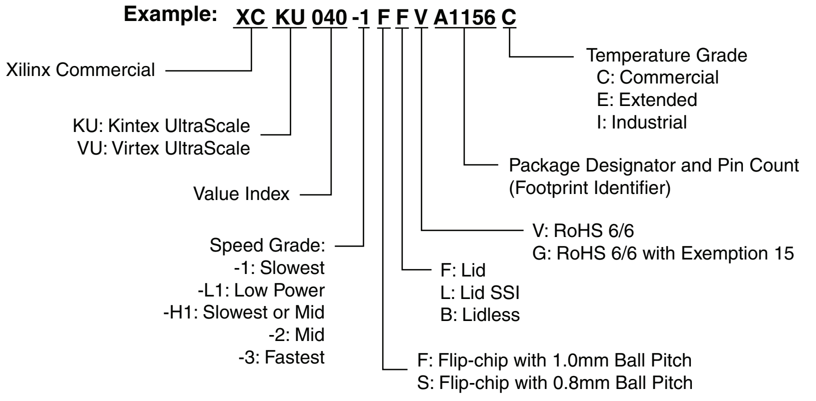
*Table 21:* **Speed Grade and Temperature Grade *(Cont'd)***

| Device Family | Devices | Speed Grade and Temperature Grade | | | |
|---|---|---|---|---|---|
| | | Commercial (C) | Extended (E) | | Industrial (I) |
| | | 0°C to +85°C | 0°C to +100°C | 0°C to +110°C | –40°C to +100°C |
| Zynq UltraScale+ | CG Devices | | -2E (0.85V) | | -2I (0.85V) |
| | | | | -2LE(2)(3) (0.85V or 0.72V) | |
| | | | -1E (0.85V) | | -1I (0.85V) |
| | | | | | -1LI(3) (0.85V or 0.72V) |
| | ZU2EG<br>ZU3EG | | -2E (0.85V) | | -2I (0.85V) |
| | | | | -2LE(2)(3) (0.85V or 0.72V) | |
| | | | -1E (0.85V) | | -1I (0.85V) |
| | | | | | -1LI(3) (0.85V or 0.72V) |
| | ZU4EG<br>ZU5EG<br>ZU6EG<br>ZU7EG<br>ZU9EG<br>ZU11EG<br>ZU15EG<br>ZU17EG<br>ZU19EG | | -3E (0.90V) | | |
| | | | -2E (0.85V) | | -2I (0.85V) |
| | | | | -2LE(2)(3) (0.85V or 0.72V) | |
| | | | -1E (0.85V) | | -1I (0.85V) |
| | | | | | -1LI(3) (0.85V or 0.72V) |
| | EV Devices | | -3E (0.90V) | | |
| | | | -2E (0.85V) | | -2I (0.85V) |
| | | | | -2LE(2)(3) (0.85V or 0.72V) | |
| | | | -1E (0.85V) | | -1I (0.85V) |
| | | | | | -1LI(3) (0.85V or 0.72V) |

**Notes:**

1. KU025 and KU095 are not available in -3E or -1LI speed/temperature grades.
2. In -2LE speed/temperature grade, devices can operate for a limited time with junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal at 0.85V or low voltage at 0.72V). Operation at 110°C Tj is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of device lifetime.
3. In Zynq UltraScale+ MPSoCs, when operating the PL at low voltage (0.72V), the PS operates at nominal voltage (0.85V).

The ordering information shown in Figure 3 applies to all packages in the Kintex UltraScale and Virtex UltraScale FPGAs. Refer to the Package Marking section of UG575, *UltraScale and UltraScale+ FPGAs Packaging and Pinouts User Guide* for a more detailed explanation of the device markings.



1) -L1 and -H1 are the ordering codes for the -1L and -1H speed grades, respectively.
2) See UG575: *UltraScale and UltraScale+ FPGAs Packaging and Pinouts User Guide* for more information.

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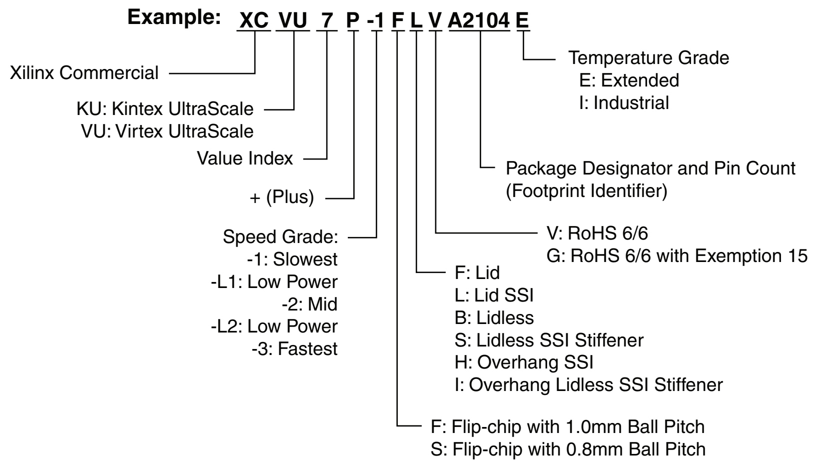
*Figure 3:* **Kintex UltraScale and Virtex UltraScale FPGA Ordering Information**

The ordering information shown in Figure 4 applies to all packages in the Kintex UltraScale+ and Virtex UltraScale+ FPGAs, and Figure 5 applies to Zynq UltraScale+s.

The -1L and -2L speed grades in the UltraScale+ families can run at one of two different $V_{CCINT}$ operating voltages. At 0.72V, they operate at similar performance to the Kintex UltraScale and Virtex UltraScale devices with up to 30% reduction in power consumption. At 0.85V, they consume similar power to the Kintex UltraScale and Virtex UltraScale devices, but operate over 30% faster.

For UltraScale+ devices, the information in this document is pre-release, provided ahead of silicon ordering availability. Please contact your Xilinx sales representative for more information on Early Access Programs.



1) -L1 and -L2 are the ordering codes for the low power -1L and -2L speed grades, respectively.

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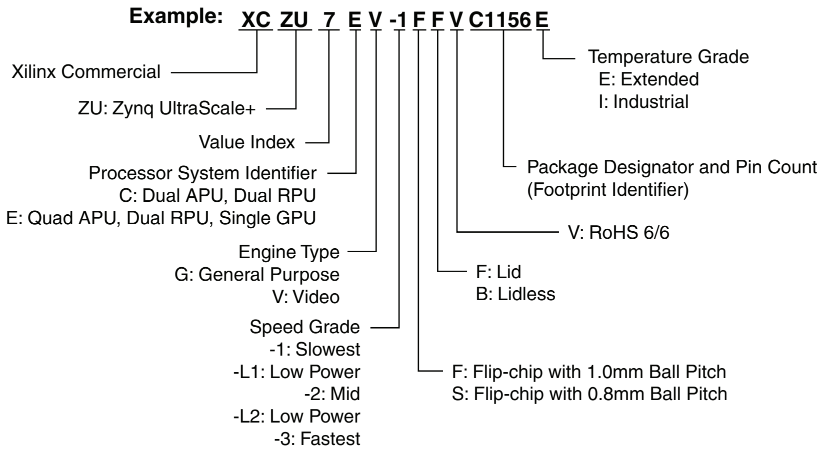
*Figure 4:* **UltraScale+ FPGA Ordering Information**



1) -L1 and -L2 are the ordering codes for the low power -1L and -2L speed grades, respectively.

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*Figure 5:* **Zynq UltraScale+ Ordering Information**

# Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|---|---|---|
| 02/15/2017 | 2.11 | Updated Table 1, Table 9: Converted HBM from Gb to GB. Updated Table 11, Table 13, and Table 15: Updated DSP count for Zynq UltraScale+ MPSoCs. Updated Cache Coherent Interconnect for Accelerators (CCIX). Updated High Bandwidth Memory (HBM). Updated Table 21: Added-2E speed grade to all UltraScale+ devices. Removed -3E from XCZU2 and XCZU3. |
| 11/09/2016 | 2.10 | Updated Table 1. Added HBM devices to Table 9, Table 10, Table 19 and new High Bandwidth Memory (HBM) section. Added Cache Coherent Interconnect for Accelerators (CCIX) section. |
| 09/27/2016 | 2.9 | Updated Table 5, Table 12, Table 13, and Table 14. |
| 06/03/2016 | 2.8 | Added Zynq UltraScale+ MPSoC CG devices: Added Table 2. Updated Table 11, Table 12, Table 21, and Figure 5. Created separate tables for EG and EV devices: Table 13, Table 14, Table 15, and Table 16.<br>Updated Table 1, Table 3, Table 5 and notes, Table 6 and notes, Table 7, Table 9, Table 10, Processing System Overview, and Processing System (PS) details. |
| 02/17/2016 | 2.7 | Added Migrating Devices. Updated Table 4, Table 5, Table 6, Table 10, Table 11, Table 12, and Figure 4. |
| 12/15/2015 | 2.6 | Updated Table 1, Table 5, Table 6, Table 9, Table 12, and Configuration. |
| 11/24/2015 | 2.5 | Updated Configuration, Encryption, and System Monitoring, Table 5, Table 9, Table 11, and Table 21. |
| 10/15/2015 | 2.4 | Updated Table 1, Table 3, Table 5, Table 7, Table 9, and Table 11 with System Logic Cells. Updated Figure 3. Updated Table 19. |
| 09/29/2015 | 2.3 | Added A1156 to KU095 in Table 4. Updated Table 5. Updated Max. Distributed RAM in Table 9. Updated Distributed RAM in Table 11. Added Table 19. Updated Table 21. Updated Figure 3. |
| 08/14/2015 | 2.2 | Updated Table 1. Added XCKU025 to Table 3, Table 4, and Table 21. Updated Table 7, Table 9, Table 11, Table 12, Table 18. Updated System Monitor. Added voltage information to Table 21. |
| 04/27/2015 | 2.1 | Updated Table 1, Table 3, Table 4, Table 5, Table 6, Table 7, Table 10, Table 11, Table 12, Table 17, I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken, Integrated Interface Blocks for PCI Express Designs, USB 3.0/2.0, Clock Management, System Monitor, and Figure 3. |
| 02/23/2015 | 2.0 | UltraScale+ device information (Kintex UltraScale+ FPGA, Virtex UltraScale+ FPGA, and Zynq UltraScale+ MPSoC) added throughout document. |
| 12/16/2014 | 1.6 | Updated Table 1; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 3, Table 7; Table 8; and Table 17. |
| 11/17/2014 | 1.5 | Updated I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 1; Table 4; Table 7; Table 8; Table 17; Input/Output; and Figure 3. |
| 09/16/2014 | 1.4 | Updated Logic Cell information in Table 1. Updated Table 3; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 7; Table 8; Integrated Block for 100G Ethernet; and Figure 3. |
| 05/20/2014 | 1.3 | Updated Table 8. |
| 05/13/2014 | 1.2 | Added Ordering Information. Updated Table 1, Clocks and Memory Interfaces, Table 3, Table 7 (removed XCVU145; added XCVU190), Table 8 (removed XCVU145; removed FLVD1924 from XCVU160; added XCVU190; updated Table Notes), Table 17, Integrated Interface Blocks for PCI Express Designs, and Integrated Block for Interlaken, and Memory Interfaces. |

| Date | Version | Description of Revisions |
|---|---|---|
| 02/06/2014 | 1.1 | Updated PCIe information in Table 1 and Table 3. Added FFVJ1924 package to Table 8. |
| 12/10/2013 | 1.0 | Initial Xilinx release. |