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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	20340
Number of Logic Elements/Cells	355950
Total RAM Bits	31641600
Number of I/O	280
Number of Gates	-
Voltage - Supply	0.825V ~ 0.876V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BBGA, FCBGA
Supplier Device Package	676-FCBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcku3p-1ffvb676i">https://www.e-xfl.com/product-detail/xilinx/xcku3p-1ffvb676i</a>

# Kintex UltraScale+ FPGA Feature Summary

Table 5: Kintex UltraScale+ FPGA Feature Summary

	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P
System Logic Cells	355,950	474,600	599,550	653,100	746,550	1,143,450
CLB Flip-Flops	325,440	433,920	548,160	597,120	682,560	1,045,440
CLB LUTs	162,720	216,960	274,080	298,560	341,280	522,720
Max. Distributed RAM (Mb)	4.7	6.1	8.8	9.1	11.3	9.8
Block RAM Blocks	360	480	912	600	744	984
Block RAM (Mb)	12.7	16.9	32.1	21.1	26.2	34.6
UltraRAM Blocks	48	64	0	80	112	128
UltraRAM (Mb)	13.5	18.0	0	22.5	31.5	36.0
CMTs (1 MMCM and 2 PLLs)	4	4	4	8	4	11
Max. HP I/O <sup>(1)</sup>	208	208	208	416	208	572
Max. HD I/O <sup>(2)</sup>	96	96	96	96	96	96
DSP Slices	1,368	1,824	2,520	2,928	3,528	1,968
System Monitor	1	1	1	1	1	1
GTH Transceiver 16.3Gb/s	0	0	28	32	28	44
GTY Transceivers 32.75Gb/s <sup>(3)</sup>	16	16	0	20	0	32
Transceiver Fractional PLLs	8	8	14	26	14	38
PCIe Gen3 x16 and Gen4 x8	1	1	0	4	0	5
150G Interlaken	0	0	0	1	0	4
100G Ethernet w/RS-FEC	0	1	0	2	0	4

## Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTY transceiver line rates are package limited: SFVB784 to 12.5Gb/s; FFVA676, FFVD900, and FFVA1156 to 16.3Gb/s. See [Table 6](#).

# Kintex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 6: Kintex UltraScale+ Device-Package Combinations and Maximum I/Os

Package (1)(2)(4)	Package Dimensions (mm)	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SFVB784(3)	23x23	96, 208 0, 16	96, 208 0, 16				
FFVA676(3)	27x27	48, 208 0, 16	48, 208 0, 16				
FFVB676	27x27	72, 208 0, 16	72, 208 0, 16				
FFVD900(3)	31x31	96, 208 0, 16	96, 208 0, 16		96, 312 16, 0		
FFVE900	31x31			96, 208 28, 0		96, 208 28, 0	
FFVA1156(3)	35x35				48, 416 20, 8		48, 468 20, 8
FFVE1517	40x40				96, 416 32, 20		96, 416 32, 24
FFVA1760	42.5x42.5						96, 416 44, 32
FFVE1760	42.5x42.5						96, 572 32, 24

## Notes:

1. Go to [Ordering Information](#) for package designation details.
2. FF packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. GTY transceiver line rates are package limited: SFVB784 to 12.5Gb/s; FFVA676, FFVD900, and FFVA1156 to 16.3Gb/s.
4. Packages with the same last letter and number sequence, e.g., A676, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.

# Virtex UltraScale FPGA Feature Summary

Table 7: Virtex UltraScale FPGA Feature Summary

	VU065	VU080	VU095	VU125	VU160	VU190	VU440
System Logic Cells	783,300	975,000	1,176,000	1,566,600	2,026,500	2,349,900	5,540,850
CLB Flip-Flops	716,160	891,424	1,075,200	1,432,320	1,852,800	2,148,480	5,065,920
CLB LUTs	358,080	445,712	537,600	716,160	926,400	1,074,240	2,532,960
Maximum Distributed RAM (Mb)	4.8	3.9	4.8	9.7	12.7	14.5	28.7
Block RAM Blocks	1,260	1,421	1,728	2,520	3,276	3,780	2,520
Block RAM (Mb)	44.3	50.0	60.8	88.6	115.2	132.9	88.6
CMT (1 MMCM, 2 PLLs)	10	16	16	20	28	30	30
I/O DLLs	40	64	64	80	120	120	120
Maximum HP I/Os <sup>(1)</sup>	468	780	780	780	650	650	1,404
Maximum HR I/Os <sup>(2)</sup>	52	52	52	104	52	52	52
DSP Slices	600	672	768	1,200	1,560	1,800	2,880
System Monitor	1	1	1	2	3	3	3
PCIe Gen3 x8	2	4	4	4	4	6	6
150G Interlaken	3	6	6	6	8	9	0
100G Ethernet	3	4	4	6	9	9	3
GTH 16.3Gb/s Transceivers	20	32	32	40	52	60	48
GTY 30.5Gb/s Transceivers	20	32	32	40	52	60	0
Transceiver Fractional PLLs	10	16	16	20	26	30	0

## Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

# Virtex UltraScale+ FPGA Feature Summary

Table 9: Virtex UltraScale+ FPGA Feature Summary

	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
System Logic Cells	862,050	1,313,763	1,724,100	2,586,150	2,835,000	3,780,000	961,800	961,800	1,906,800	2,851,800
CLB Flip-Flops	788,160	1,201,154	1,576,320	2,364,480	2,592,000	3,456,000	879,360	879,360	1,743,360	2,607,360
CLB LUTs	394,080	600,577	788,160	1,182,240	1,296,000	1,728,000	439,680	439,680	871,680	1,303,680
Max. Distributed RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	12.5	12.5	24.6	36.7
Block RAM Blocks	720	1,024	1,440	2,160	2,016	2,688	672	672	1,344	2,016
Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	23.6	23.6	47.3	70.9
UltraRAM Blocks	320	470	640	960	960	1,280	320	320	640	960
UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	90.0	90.0	180.0	270.0
HBM DRAM (GB)	–	–	–	–	–	–	4	8	8	8
CMTs (1 MMCM and 2 PLLs)	10	20	20	30	12	16	4	4	8	12
Max. HP I/O <sup>(1)</sup>	520	832	832	832	624	832	208	208	416	624
DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	2,880	2,880	5,952	9,024
System Monitor	1	2	2	3	3	4	1	1	2	3
GTY Transceivers 32.75Gb/s <sup>(2)</sup>	40	80	80	120	96	128	32	32	64	96
Transceiver Fractional PLLs	20	40	40	60	48	64	16	16	32	48
PCIe Gen3 x16 and Gen4 x8	2	4	4	6	3	4	4	4	5	6
CCIX Ports <sup>(3)</sup>	–	–	–	–	–	–	4	4	4	4
150G Interlaken	3	4	6	9	6	8	0	0	2	4
100G Ethernet w/RS-FEC	3	4	6	9	9	12	2	2	5	8

## Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s. See [Table 10](#).
3. A CCIX port requires the use of a PCIe Gen3 x16 / Gen4 x8 block.

# Zynq UltraScale+: CG Device Feature Summary

Table 11: Zynq UltraScale+: CG Device Feature Summary

	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
Application Processing Unit	Dual-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache						
Real-Time Processing Unit	Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM						
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC						
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters						
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII						
System Logic Cells	103,320	154,350	192,150	256,200	469,446	504,000	599,550
CLB Flip-Flops	94,464	141,120	175,680	234,240	429,208	460,800	548,160
CLB LUTs	47,232	70,560	87,840	117,120	214,604	230,400	274,080
Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8
Block RAM Blocks	150	216	128	144	714	312	912
Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1
UltraRAM Blocks	0	0	48	64	0	96	0
UltraRAM (Mb)	0	0	14.0	18.0	0	27.0	0
DSP Slices	240	360	728	1,248	1,973	1,728	2,520
CMTs	3	3	4	4	4	8	4
Max. HP I/O <sup>(1)</sup>	156	156	156	156	208	416	208
Max. HD I/O <sup>(2)</sup>	96	96	96	96	120	48	120
System Monitor	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s <sup>(3)</sup>	0	0	16	16	24	24	24
GTY Transceivers 32.75Gb/s	0	0	0	0	0	0	0
Transceiver Fractional PLLs	0	0	8	8	12	12	12
PCIe Gen3 x16 and Gen4 x8	0	0	2	2	0	2	0
150G Interlaken	0	0	0	0	0	0	0
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0

## Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 12](#).

# Zynq UltraScale+: CG Device-Package Combinations and Maximum I/Os

Table 12: Zynq UltraScale+: CG Device-Package Combinations and Maximum I/Os

Package (1)(2)(3)(4)(5)	Package Dimensions (mm)	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SBVA484(6)	19x19	24, 58 0, 0	24, 58 0, 0					
SFVA625	21x21	24, 156 0, 0	24, 156 0, 0					
SFVC784(7)	23x23	96, 156 0, 0	96, 156 0, 0	96, 156 4, 0	96, 156 4, 0			
FBVB900	31x31			48, 156 16, 0	48, 156 16, 0		48, 156 16, 0	
FFVC900	31x31					48, 156 16, 0		48, 156 16, 0
FFVB1156	35x35					120, 208 24, 0		120, 208 24, 0
FFVC1156	35x35						48, 312 20, 0	
FFVF1517	40x40						48, 416 24, 0	

## Notes:

1. Go to [Ordering Information](#) for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. All device package combinations bond out 214 PS I/O except ZU2CG and ZU3CG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
5. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
6. All 58 HP I/O pins are powered by the same  $V_{CCO}$  supply.
7. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

# Zynq UltraScale+: EG Device Feature Summary

Table 15: Zynq UltraScale+: EV Device Feature Summary

	ZU4EV	ZU5EV	ZU7EV
Application Processing Unit	Quad-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache		
Real-Time Processing Unit	Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM		
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC		
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters		
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII		
Graphic Processing Unit	ARM Mali-400 MP2; 64KB L2 Cache		
Video Codec	1	1	1
System Logic Cells	192,150	256,200	504,000
CLB Flip-Flops	175,680	234,240	460,800
CLB LUTs	87,840	117,120	230,400
Distributed RAM (Mb)	2.6	3.5	6.2
Block RAM Blocks	128	144	312
Block RAM (Mb)	4.5	5.1	11.0
UltraRAM Blocks	48	64	96
UltraRAM (Mb)	14.0	18.0	27.0
DSP Slices	728	1,248	1,728
CMTs	4	4	8
Max. HP I/O <sup>(1)</sup>	156	156	416
Max. HD I/O <sup>(2)</sup>	96	96	48
System Monitor	2	2	2
GTH Transceiver 16.3Gb/s <sup>(3)</sup>	16	16	24
GTY Transceivers 32.75Gb/s	0	0	0
Transceiver Fractional PLLs	8	8	12
PCIe Gen3 x16 and Gen4 x8	2	2	2
150G Interlaken	0	0	0
100G Ethernet w/ RS-FEC	0	0	0

## Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 16](#).



contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. Figure 2 is a representation of an FPGA divided into regions.

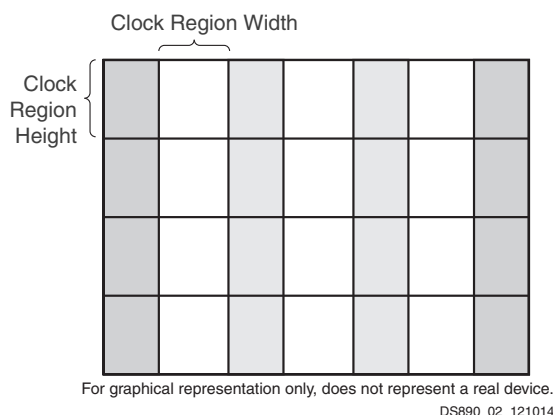


Figure 2: Column-Based FPGA Divided into Clock Regions

## Processing System (PS)

Zynq UltraScale+ MPSoCs consist of a PS coupled with programmable logic. The contents of the PS varies between the different Zynq UltraScale+ devices. All devices contain an APU, an RPU, and many peripherals for connecting the multiple processing engines to external components. The EG and EV devices contain a GPU and the EV devices contain a video codec unit (VCU). The components of the PS are connected together and to the PL through a multi-layered ARM AMBA AXI non-blocking interconnect that supports multiple simultaneous master-slave transactions. Traffic through the interconnect can be regulated by the quality of service (QoS) block in the interconnect. Twelve dedicated AXI 32-bit, 64-bit, or 128-bit ports connect the PL to high-speed interconnect and DDR in the PS via a FIFO interface.

There are four independently controllable power domains: the PL plus three within the PS (full power, lower power, and battery power domains). Additionally, many peripherals support clock gating and power gating to further reduce dynamic and static power consumption.

## Application Processing Unit (APU)

The APU has a feature-rich dual-core or quad-core ARM Cortex-A53 processor. Cortex-A53 cores are 32-bit/64-bit application processors based on ARM-v8A architecture, offering the best performance-to-power ratio. The ARMv8 architecture supports hardware virtualization. Each of the Cortex-A53 cores has: 32KB of instruction and data L1 caches, with parity and ECC protection respectively; a NEON SIMD engine; and a single and double precision floating point unit. In addition to these blocks, the APU consists of a snoop control unit and a 1MB L2 cache with ECC protection to enhance system-level performance. The snoop control unit keeps the L1 caches coherent thus eliminating the need of spending software bandwidth for coherency. The APU also has a built-in interrupt controller supporting virtual interrupts. The APU communicates to the rest of the PS through 128-bit AXI coherent extension (ACE) port via Cache Coherent Interconnect (CCI) block, using the System Memory Management Unit (SMMU). The APU is also connected to the Programmable Logic (PL), through the 128-bit accelerator coherency port

(ACP), providing a low latency coherent port for accelerators in the PL. To support real-time debug and trace, each core also has an Embedded Trace Macrocell (ETM) that communicates with the ARM CoreSight™ Debug System.

## Real-Time Processing Unit (RPU)

The RPU in the PS contains a dual-core ARM Cortex-R5 PS. Cortex-R5 cores are 32-bit real-time processor cores based on ARM-v7R architecture. Each of the Cortex-R5 cores has 32KB of level-1 (L1) instruction and data cache with ECC protection. In addition to the L1 caches, each of the Cortex-R5 cores also has a 128KB tightly coupled memory (TCM) interface for real-time single cycle access. The RPU also has a dedicated interrupt controller. The RPU can operate in either split or lock-step mode. In split mode, both processors run independently of each other. In lock-step mode, they run in parallel with each other, with integrated comparator logic, and the TCMs are used as 256KB unified memory. The RPU communicates with the rest of the PS via the 128-bit AXI-4 ports connected to the low power domain switch. It also communicates directly with the PL through 128-bit low latency AXI-4 ports. To support real-time debug and trace each core also has an embedded trace macrocell (ETM) that communicates with the ARM CoreSight Debug System.

## External Memory

The PS can interface to many types of external memories through dedicated memory controllers. The dynamic memory controller supports DDR3, DDR3L, DDR4, LPDDR3, and LPDDR4 memories. The multi-protocol DDR memory controller can be configured to access a 2GB address space in 32-bit addressing mode and up to 32GB in 64-bit addressing mode using a single or dual rank configuration of 8-bit, 16-bit, or 32-bit DRAM memories. Both 32-bit and 64-bit bus access modes are protected by ECC using extra bits.

The SD/eMMC controller supports 1 and 4 bit data interfaces at low, default, high-speed, and ultra-high-speed (UHS) clock rates. This controller also supports 1-, 4-, or 8-bit-wide eMMC interfaces that are compliant to the eMMC 4.51 specification. eMMC is one of the primary boot and configuration modes for Zynq UltraScale+ MPSoCs and supports boot from managed NAND devices. The controller has a built-in DMA for enhanced performance.

The Quad-SPI controller is one of the primary boot and configuration devices. It supports 4-byte and 3-byte addressing modes. In both addressing modes, single, dual-stacked, and dual-parallel configurations are supported. Single mode supports a quad serial NOR flash memory, while in double stacked and double parallel modes, it supports two quad serial NOR flash memories.

The NAND controller is based on ONFI3.1 specification. It has an 8-pin interface and provides 200Mb/s of bandwidth in synchronous mode. It supports 24 bits of ECC thus enabling support for SLC NAND memories. It has two chip-selects to support deeper memory and a built-in DMA for enhanced performance.

## General Connectivity

There are many peripherals in the PS for connecting to external devices over industry standard protocols, including CAN2.0B, USB, Ethernet, I2C, and UART. Many of the peripherals support clock gating and power gating modes to reduce dynamic and static power consumption.

### **USB 3.0/2.0**

The pair of USB controllers can be configured as host, device, or On-The-Go (OTG). The core is compliant to USB 3.0 specification and supports super, high, full, and low speed modes in all configurations. In host mode, the USB controller is compliant with the Intel XHCI specification. In device mode, it supports up to 12 end points. While operating in USB 3.0 mode, the controller uses the serial transceiver and operates up to 5.0Gb/s. In USB 2.0 mode, the Universal Low Peripheral Interface (ULPI) is used to connect the controller to an external PHY operating up to 480Mb/s. The ULPI is also connected in USB 3.0 mode to support high-speed operations.

### **Ethernet MAC**

The four tri-speed ethernet MACs support 10Mb/s, 100Mb/s, and 1Gb/s operations. The MACs support jumbo frames and time stamping through the interfaces based on IEEE Std 1588v2. The ethernet MACs can be connected through the serial transceivers (SGMII), the MIO (RGMII), or through EMIO (GMII). The GMII interface can be converted to a different interface within the PL.

## High-Speed Connectivity

The PS includes four PS-GTR transceivers (transmit and receive), supporting data rates up to 6.0Gb/s and can interface to the peripherals for communication over PCIe, SATA, USB 3.0, SGMII, and DisplayPort.

### **PCIe**

The integrated block for PCIe is compliant with PCI Express base specification 2.1 and supports x1, x2, and x4 configurations as root complex or end point, compliant to transaction ordering rules in both configurations. It has built-in DMA, supports one virtual channel and provides fully configurable base address registers.

### **SATA**

Users can connect up to two external devices using the two SATA host port interfaces compliant to the SATA 3.1 specification. The SATA interfaces can operate at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates and are compliant with advanced host controller interface (AHCI) version 1.3 supporting partial and slumber power modes.

### **DisplayPort**

The DisplayPort controller supports up to two lanes of source-only DisplayPort compliant with VESA DisplayPort v1.2a specification (source only) at 1.62Gb/s, 2.7Gb/s, and 5.4Gb/s data rates. The controller supports single stream transport (SST); video resolution up to 4Kx2K at a 30Hz frame rate; video formats Y-only, YCbCr444, YCbCr422, YCbCr420, RGB, YUV444, YUV422, xvYCC, and pixel color depth of 6, 8, 10, and 12 bits per color component.

## I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards  $V_{CCO}$  or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a  $100\Omega$  internal resistor. All UltraScale devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. UltraScale+ families add support for MIPI with a dedicated D-PHY in the I/O bank.

### ***3-State Digitally Controlled Impedance and Low Power I/O Features***

The 3-state Digitally Controlled Impedance (T\_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to  $V_{CCO}$  or split (Thevenin) termination to  $V_{CCO}/2$ . This allows users to eliminate off-chip termination for signals using T\_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

## I/O Logic

### ***Input and Output Delay***

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

### ***ISERDES and OSERDES***

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

# High-Speed Serial Transceivers

Serial data transmission between devices on the same PCB, over backplanes, and across even longer distances is becoming increasingly important for scaling to 100Gb/s and 400Gb/s line cards. Specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues are required at these high data rates.

Three types of transceivers are used in the UltraScale architecture: GTH and GTY in FPGAs and MPSoC PL, and PS-GTR in the MPSoC PS. All transceivers are arranged in groups of four, known as a transceiver Quad. Each serial transceiver is a combined transmitter and receiver. [Table 17](#) compares the available transceivers.

**Table 17: Transceiver Information**

	Kintex UltraScale		Kintex UltraScale+		Virtex UltraScale		Virtex UltraScale+	Zynq UltraScale+		
Type	GTH	GTY	GTH	GTY	GTH	GTY	GTY	PS-GTR	GTH	GTY
Qty	16–64	0–32	20–60	0–60	20–60	0–60	40–128	4	0–44	0–28
Max. Data Rate	16.3Gb/s	16.3Gb/s	16.3Gb/s	32.75Gb/s	16.3Gb/s	30.5Gb/s	32.75Gb/s	6.0Gb/s	16.3Gb/s	32.75Gb/s
Min. Data Rate	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	0.5Gb/s	1.25Gb/s	0.5Gb/s	0.5Gb/s
Key Apps	<ul style="list-style-type: none"> <li>Backplane</li> <li>PCIe Gen4</li> <li>HMC</li> </ul>	<ul style="list-style-type: none"> <li>Backplane</li> <li>PCIe Gen4</li> <li>HMC</li> </ul>	<ul style="list-style-type: none"> <li>Backplane</li> <li>PCIe Gen4</li> <li>HMC</li> </ul>	<ul style="list-style-type: none"> <li>100G+ Optics</li> <li>Chip-to-Chip</li> <li>25G+ Backplane</li> <li>HMC</li> </ul>	<ul style="list-style-type: none"> <li>Backplane</li> <li>PCIe Gen4</li> <li>HMC</li> </ul>	<ul style="list-style-type: none"> <li>100G+ Optics</li> <li>Chip-to-Chip</li> <li>25G+ Backplane</li> <li>HMC</li> </ul>	<ul style="list-style-type: none"> <li>100G+ Optics</li> <li>Chip-to-Chip</li> <li>25G+ Backplane</li> <li>HMC</li> </ul>	<ul style="list-style-type: none"> <li>PCIe Gen2</li> <li>USB</li> <li>Ethernet</li> </ul>	<ul style="list-style-type: none"> <li>Backplane</li> <li>PCIe Gen4</li> <li>HMC</li> </ul>	<ul style="list-style-type: none"> <li>100G+ Optics</li> <li>Chip-to-Chip</li> <li>25G+ Backplane</li> <li>HMC</li> </ul>

The following information in this section pertains to the GTH and GTY only.

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

## Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

## Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally “auto-adapt” to automatically learn and compensate for different interconnect characteristics. This enables even more margin for 10G+ and 25G+ backplanes.

## Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

The MMCM can have a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of 1/8 and can thus increase frequency synthesis capabilities by a factor of 8. The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency. At 1,600MHz, the phase-shift timing increment is 11.2ps.

## PLL

With fewer features than the MMCM, the two PLLs in a clock management tile are primarily present to provide the necessary clocks to the dedicated memory interface circuitry. The circuit at the center of the PLLs is similar to the MMCM, with PFD feeding a VCO and programmable M, D, and O counters. There are two divided outputs to the device fabric per PLL as well as one clock plus one enable signal to the memory interface circuitry.

UltraScale+ MPSoCs are equipped with five additional PLLs in the PS for independently configuring the four primary clock domains with the PS: the APU, the RPU, the DDR controller, and the I/O peripherals.

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## Clock Distribution

Clocks are distributed throughout UltraScale devices via buffers that drive a number of vertical and horizontal tracks. There are 24 horizontal clock routes per clock region and 24 vertical clock routes per clock region with 24 additional vertical clock routes adjacent to the MMCM and PLL. Within a clock region, clock signals are routed to the device logic (CLBs, etc.) via 16 gateable leaf clocks.

Several types of clock buffers are available. The BUFGCE and BUFCE\_LEAF buffers provide clock gating at the global and leaf levels, respectively. BUFGCTRL provides glitchless clock muxing and gating capability. BUFGCE\_DIV has clock gating capability and can divide a clock by 1 to 8. BUFG\_GT performs clock division from 1 to 8 for the transceiver clocks. In MPSoCs, clocks can be transferred from the PS to the PL using dedicated buffers.

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## Memory Interfaces

Memory interface data rates continue to increase, driving the need for dedicated circuitry that enables high performance, reliable interfacing to current and next-generation memory technologies. Every UltraScale device includes dedicated physical interfaces (PHY) blocks located between the CMT and I/O columns that support implementation of high-performance PHY blocks to external memories such as DDR4, DDR3, QDRII+, and RLDRAM3. The PHY blocks in each I/O bank generate the address/control and data bus signaling protocols as well as the precision clock/data alignment required to reliably communicate with a variety of high-performance memory standards. Multiple I/O banks can be used to create wider memory interfaces.

As well as external parallel memory interfaces, UltraScale FPGAs and MPSoCs can communicate to external serial memories, such as Hybrid Memory Cube (HMC), via the high-speed serial transceivers. All transceivers in the UltraScale architecture support the HMC protocol, up to 15Gb/s line rates. UltraScale devices support the highest bandwidth HMC configuration of 64 lanes with a single FPGA.



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## Interconnect

Various length vertical and horizontal routing resources in the UltraScale architecture that span 1, 2, 4, 5, 12, or 16 CLBs ensure that all signals can be transported from source to destination with ease, providing support for the next generation of wide data buses to be routed across even the highest capacity devices while simultaneously improving quality of results and software run time.

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## Digital Signal Processing

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All UltraScale devices have many dedicated, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated  $27 \times 18$  bit twos complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The 96-bit-wide XOR function, programmable to 12, 24, 48, or 96-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP also includes a 48-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

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## System Monitor

The System Monitor blocks in the UltraScale architecture are used to enhance the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors and external channels to the ADC.

All UltraScale architecture-based devices contain at least one System Monitor. The System Monitor in UltraScale+ FPGAs and the PL of Zynq UltraScale+ MPSoCs is similar to the Kintex UltraScale and Virtex UltraScale devices but with additional features including a PMBus interface.



Zynq UltraScale+ MPSoCs contain an additional System Monitor block in the PS. See [Table 20](#).

**Table 20: Key System Monitor Features**

	Kintex UltraScale Virtex UltraScale	Kintex UltraScale+ Virtex UltraScale+ Zynq UltraScale+ MPSoC PL	Zynq UltraScale+ MPSoC PS
ADC	10-bit 200kSPS	10-bit 200kSPS	10-bit 1MSPS
Interfaces	JTAG, I2C, DRP	JTAG, I2C, DRP, PMBus	APB

In FPGAs and the MPSoC PL, sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, PMBus, or I2C interfaces. The I2C interface and PMBus allow the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

The System Monitor in the MPSoC PS uses a 10-bit, 1 mega-sample-per-second (MSPS) ADC to digitize the sensor outputs. The measurements are stored in registers and are accessed via the Advanced Peripheral Bus (APB) interface by the processors and the platform management unit (PMU) in the PS.

## Configuration

The UltraScale architecture-based devices store their customized configuration in SRAM-type internal latches. The configuration storage is volatile and must be reloaded whenever the device is powered up. This storage can also be reloaded at any time. Several methods and data formats for loading configuration are available, determined by the mode pins, with more dedicated configuration datapath pins to simplify the configuration process.

UltraScale architecture-based devices support secure and non-secure boot with optional Advanced Encryption Standard - Galois/Counter Mode (AES-GCM) decryption and authentication logic. If only authentication is required, the UltraScale architecture provides an alternative form of authentication in the form of RSA algorithms. For RSA authentication support in the Kintex UltraScale and Virtex UltraScale families, go to [UG570](#), *UltraScale Architecture Configuration User Guide*.

UltraScale architecture-based devices also have the ability to select between multiple configurations, and support robust field-update methodologies. This is especially useful for updates to a design after the end product has been shipped. Designers can release their product with an early version of the design, thus getting their product to market faster. This feature allows designers to keep their customers current with the most up-to-date design while the product is already deployed in the field.

## Booting MPSoCs

Zynq UltraScale+ MPSoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the AES-GCM, SHA-3/384 decryption/authentication, and 4096-bit RSA blocks decrypt and authenticate the image.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NAND, Quad-SPI, SD, eMMC, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. One of the CPUs, Cortex-A53 or Cortex-R5, executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip memory (OCM).

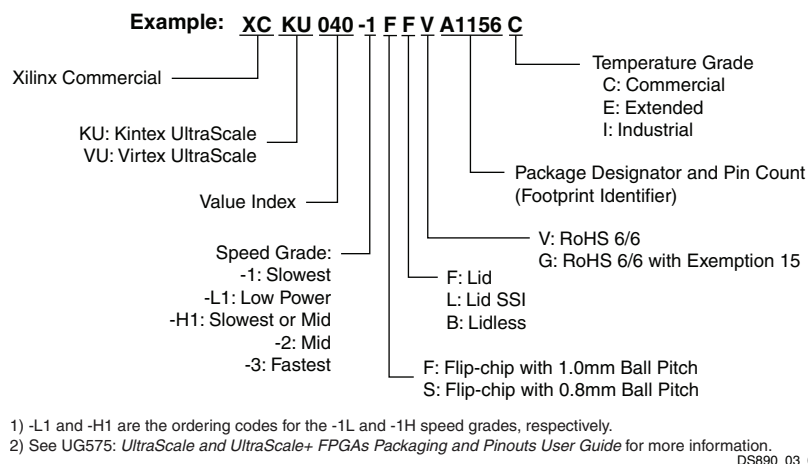
Table 21: Speed Grade and Temperature Grade (Cont'd)

Device Family	Devices	Speed Grade and Temperature Grade			
		Commercial (C)	Extended (E)		Industrial (I)
		0°C to +85°C	0°C to +100°C	0°C to +110°C	–40°C to +100°C
Zynq UltraScale+	CG Devices		-2E (0.85V)		-2I (0.85V)
				-2LE <sup>(2)(3)</sup> (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI <sup>(3)</sup> (0.85V or 0.72V)
	ZU2EG ZU3EG		-2E (0.85V)		-2I (0.85V)
				-2LE <sup>(2)(3)</sup> (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI <sup>(3)</sup> (0.85V or 0.72V)
	ZU4EG ZU5EG ZU6EG ZU7EG ZU9EG ZU11EG ZU15EG ZU17EG ZU19EG		-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE <sup>(2)(3)</sup> (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI <sup>(3)</sup> (0.85V or 0.72V)
			-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE <sup>(2)(3)</sup> (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI <sup>(3)</sup> (0.85V or 0.72V)
	EV Devices		-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE <sup>(2)(3)</sup> (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI <sup>(3)</sup> (0.85V or 0.72V)

**Notes:**

1. KU025 and KU095 are not available in -3E or -1LI speed/temperature grades.
2. In -2LE speed/temperature grade, devices can operate for a limited time with junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal at 0.85V or low voltage at 0.72V). Operation at 110°C Tj is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of device lifetime.
3. In Zynq UltraScale+ MPSoCs, when operating the PL at low voltage (0.72V), the PS operates at nominal voltage (0.85V).

The ordering information shown in [Figure 3](#) applies to all packages in the Kintex UltraScale and Virtex UltraScale FPGAs. Refer to the Package Marking section of [UG575, UltraScale and UltraScale+ FPGAs Packaging and Pinouts User Guide](#) for a more detailed explanation of the device markings.



**Figure 3: Kintex UltraScale and Virtex UltraScale FPGA Ordering Information**

# Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/15/2017	2.11	Updated <a href="#">Table 1</a> , <a href="#">Table 9</a> : Converted HBM from Gb to GB. Updated <a href="#">Table 11</a> , <a href="#">Table 13</a> , and <a href="#">Table 15</a> : Updated DSP count for Zynq UltraScale+ MPSoCs. Updated <a href="#">Cache Coherent Interconnect for Accelerators (CCIX)</a> . Updated <a href="#">High Bandwidth Memory (HBM)</a> . Updated <a href="#">Table 21</a> : Added -2E speed grade to all UltraScale+ devices. Removed -3E from XCZU2 and XCZU3.
11/09/2016	2.10	Updated <a href="#">Table 1</a> . Added HBM devices to <a href="#">Table 9</a> , <a href="#">Table 10</a> , <a href="#">Table 19</a> and new <a href="#">High Bandwidth Memory (HBM)</a> section. Added <a href="#">Cache Coherent Interconnect for Accelerators (CCIX)</a> section.
09/27/2016	2.9	Updated <a href="#">Table 5</a> , <a href="#">Table 12</a> , <a href="#">Table 13</a> , and <a href="#">Table 14</a> .
06/03/2016	2.8	Added Zynq UltraScale+ MPSoC CG devices: Added <a href="#">Table 2</a> . Updated <a href="#">Table 11</a> , <a href="#">Table 12</a> , <a href="#">Table 21</a> , and <a href="#">Figure 5</a> . Created separate tables for EG and EV devices: <a href="#">Table 13</a> , <a href="#">Table 14</a> , <a href="#">Table 15</a> , and <a href="#">Table 16</a> . Updated <a href="#">Table 1</a> , <a href="#">Table 3</a> , <a href="#">Table 5</a> and notes, <a href="#">Table 6</a> and notes, <a href="#">Table 7</a> , <a href="#">Table 9</a> , <a href="#">Table 10</a> , <a href="#">Processing System Overview</a> , and <a href="#">Processing System (PS)</a> details.
02/17/2016	2.7	Added <a href="#">Migrating Devices</a> . Updated <a href="#">Table 4</a> , <a href="#">Table 5</a> , <a href="#">Table 6</a> , <a href="#">Table 10</a> , <a href="#">Table 11</a> , <a href="#">Table 12</a> , and <a href="#">Figure 4</a> .
12/15/2015	2.6	Updated <a href="#">Table 1</a> , <a href="#">Table 5</a> , <a href="#">Table 6</a> , <a href="#">Table 9</a> , <a href="#">Table 12</a> , and <a href="#">Configuration</a> .
11/24/2015	2.5	Updated <a href="#">Configuration, Encryption, and System Monitoring</a> , <a href="#">Table 5</a> , <a href="#">Table 9</a> , <a href="#">Table 11</a> , and <a href="#">Table 21</a> .
10/15/2015	2.4	Updated <a href="#">Table 1</a> , <a href="#">Table 3</a> , <a href="#">Table 5</a> , <a href="#">Table 7</a> , <a href="#">Table 9</a> , and <a href="#">Table 11</a> with System Logic Cells. Updated <a href="#">Figure 3</a> . Updated <a href="#">Table 19</a> .
09/29/2015	2.3	Added A1156 to KU095 in <a href="#">Table 4</a> . Updated <a href="#">Table 5</a> . Updated Max. Distributed RAM in <a href="#">Table 9</a> . Updated Distributed RAM in <a href="#">Table 11</a> . Added <a href="#">Table 19</a> . Updated <a href="#">Table 21</a> . Updated <a href="#">Figure 3</a> .
08/14/2015	2.2	Updated <a href="#">Table 1</a> . Added XCKU025 to <a href="#">Table 3</a> , <a href="#">Table 4</a> , and <a href="#">Table 21</a> . Updated <a href="#">Table 7</a> , <a href="#">Table 9</a> , <a href="#">Table 11</a> , <a href="#">Table 12</a> , <a href="#">Table 18</a> . Updated <a href="#">System Monitor</a> . Added voltage information to <a href="#">Table 21</a> .
04/27/2015	2.1	Updated <a href="#">Table 1</a> , <a href="#">Table 3</a> , <a href="#">Table 4</a> , <a href="#">Table 5</a> , <a href="#">Table 6</a> , <a href="#">Table 7</a> , <a href="#">Table 10</a> , <a href="#">Table 11</a> , <a href="#">Table 12</a> , <a href="#">Table 17</a> , I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken, <a href="#">Integrated Interface Blocks for PCI Express Designs</a> , USB 3.0/2.0, Clock Management, System Monitor, and <a href="#">Figure 3</a> .
02/23/2015	2.0	UltraScale+ device information (Kintex UltraScale+ FPGA, Virtex UltraScale+ FPGA, and Zynq UltraScale+ MPSoC) added throughout document.
12/16/2014	1.6	Updated <a href="#">Table 1</a> ; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; <a href="#">Table 3</a> , <a href="#">Table 7</a> ; <a href="#">Table 8</a> ; and <a href="#">Table 17</a> .
11/17/2014	1.5	Updated I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; <a href="#">Table 1</a> ; <a href="#">Table 4</a> ; <a href="#">Table 7</a> ; <a href="#">Table 8</a> ; <a href="#">Table 17</a> ; <a href="#">Input/Output</a> ; and <a href="#">Figure 3</a> .
09/16/2014	1.4	Updated Logic Cell information in <a href="#">Table 1</a> . Updated <a href="#">Table 3</a> ; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; <a href="#">Table 7</a> ; <a href="#">Table 8</a> ; <a href="#">Integrated Block for 100G Ethernet</a> ; and <a href="#">Figure 3</a> .
05/20/2014	1.3	Updated <a href="#">Table 8</a> .
05/13/2014	1.2	Added <a href="#">Ordering Information</a> . Updated <a href="#">Table 1</a> , <a href="#">Clocks and Memory Interfaces</a> , <a href="#">Table 3</a> , <a href="#">Table 7</a> (removed XCVU145; added XCVU190), <a href="#">Table 8</a> (removed XCVU145; removed FLVD1924 from XCVU160; added XCVU190; updated Table Notes), <a href="#">Table 17</a> , <a href="#">Integrated Interface Blocks for PCI Express Designs</a> , and <a href="#">Integrated Block for Interlaken</a> , and <a href="#">Memory Interfaces</a> .

Date	Version	Description of Revisions
02/06/2014	1.1	Updated PCIe information in <a href="#">Table 1</a> and <a href="#">Table 3</a> . Added FFVJ1924 package to <a href="#">Table 8</a> .
12/10/2013	1.0	Initial Xilinx release.