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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Product Status | Active |
| Number of LABs/CLBs | 20340 |
| Number of Logic Elements/Cells | 355950 |
| Total RAM Bits | 31641600 |
| Number of I/O | 304 |
| Number of Gates | - |
| Voltage - Supply | 0.825V ~ 0.876V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 900-BBGA, FCBGA |
| Supplier Device Package | 900-FCBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcku3p-2ffvd900i |

I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken

Data is transported on and off chip through a combination of the high-performance parallel SelectIO™ interface and high-speed serial transceiver connectivity. I/O blocks provide support for cutting-edge memory interface and network protocols through flexible I/O standard and voltage support. The serial transceivers in the UltraScale architecture-based devices transfer data up to 32.75Gb/s, enabling 25G+ backplane designs with dramatically lower power per bit than previous generation transceivers. All transceivers, except the PS-GTR, support the required data rates for PCIe Gen3, and Gen4 (rev 0.5), and integrated blocks for PCIe enable UltraScale devices to support up to Gen4 x8 and Gen3 x16 Endpoint and Root Port designs. Integrated blocks for 150Gb/s Interlaken and 100Gb/s Ethernet (100G MAC/PCS) extend the capabilities of UltraScale devices, enabling simple, reliable support for Nx100G switch and bridge applications. Virtex UltraScale+ HBM devices include Cache Coherent Interconnect for Accelerators (CCIX) ports for coherently sharing data with different processors.

Clocks and Memory Interfaces

UltraScale devices contain powerful clock management circuitry, including clock synthesis, buffering, and routing components that together provide a highly capable framework to meet design requirements. The clock network allows for extremely flexible distribution of clocks to minimize the skew, power consumption, and delay associated with clock signals. The clock management technology is tightly integrated with dedicated memory interface circuitry to enable support for high-performance external memories, including DDR4. In addition to parallel memory interfaces, UltraScale devices support serial memories, such as hybrid memory cube (HMC).

Routing, SSI, Logic, Storage, and Signal Processing

Configurable Logic Blocks (CLBs) containing 6-input look-up tables (LUTs) and flip-flops, DSP slices with 27x18 multipliers, 36Kb block RAMs with built-in FIFO and ECC support, and 4Kx72 UltraRAM blocks (in UltraScale+ devices) are all connected with an abundance of high-performance, low-latency interconnect. In addition to logical functions, the CLB provides shift register, multiplexer, and carry logic functionality as well as the ability to configure the LUTs as distributed memory to complement the highly capable and configurable block RAMs. The DSP slice, with its 96-bit-wide XOR functionality, 27-bit pre-adder, and 30-bit A input, performs numerous independent functions including multiply accumulate, multiply add, and pattern detect. In addition to the device interconnect, in devices using SSI technology, signals can cross between super-logic regions (SLRs) using dedicated, low-latency interface tiles. These combined routing resources enable easy support for next-generation bus data widths. Virtex UltraScale+ HBM devices include up to 8GB of high bandwidth memory.

Configuration, Encryption, and System Monitoring

The configuration and encryption block performs numerous device-level functions critical to the successful operation of the FPGA or MPSoC. This high-performance configuration block enables device configuration from external media through various protocols, including PCIe, often with no requirement to use multi-function I/O pins during configuration. The configuration block also provides 256-bit AES-GCM decryption capability at the same performance as unencrypted configuration. Additional features include SEU detection and correction, partial reconfiguration support, and battery-backed RAM or eFUSE technology for AES key storage to provide additional security. The System Monitor enables the monitoring of the physical environment via on-chip temperature and supply sensors and can also monitor up to 17 external analog inputs. With UltraScale+ MPSoCs, the device is booted via the Configuration and Security Unit (CSU), which supports secure boot via the 256-bit AES-GCM and SHA/384 blocks. The cryptographic engines in the CSU can be used in the MPSoC after boot for user encryption.

Migrating Devices

UltraScale and UltraScale+ families provide footprint compatibility to enable users to migrate designs from one device or family to another. Any two packages with the same footprint identifier code are footprint compatible. For example, Kintex UltraScale devices in the A1156 packages are footprint compatible with Kintex UltraScale+ devices in the A1156 packages. Likewise, Virtex UltraScale devices in the B2104 packages are compatible with Virtex UltraScale+ devices and Kintex UltraScale devices in the B2104 packages. All valid device/package combinations are provided in the Device-Package Combinations and Maximum I/Os tables in this document. Refer to [UG583](#), *UltraScale Architecture PCB Design User Guide* for more detail on migrating between UltraScale and UltraScale+ devices and packages.

Kintex UltraScale FPGA Feature Summary

Table 3: Kintex UltraScale FPGA Feature Summary

| | KU025 ⁽¹⁾ | KU035 | KU040 | KU060 | KU085 | KU095 | KU115 |
|------------------------------------------|----------------------|---------|---------|---------|-----------|-----------|-----------|
| System Logic Cells | 318,150 | 444,343 | 530,250 | 725,550 | 1,088,325 | 1,176,000 | 1,451,100 |
| CLB Flip-Flops | 290,880 | 406,256 | 484,800 | 663,360 | 995,040 | 1,075,200 | 1,326,720 |
| CLB LUTs | 145,440 | 203,128 | 242,400 | 331,680 | 497,520 | 537,600 | 663,360 |
| Maximum Distributed RAM (Mb) | 4.1 | 5.9 | 7.0 | 9.1 | 13.4 | 4.7 | 18.3 |
| Block RAM Blocks | 360 | 540 | 600 | 1,080 | 1,620 | 1,680 | 2,160 |
| Block RAM (Mb) | 12.7 | 19.0 | 21.1 | 38.0 | 56.9 | 59.1 | 75.9 |
| CMTs (1 MMCM, 2 PLLs) | 6 | 10 | 10 | 12 | 22 | 16 | 24 |
| I/O DLLs | 24 | 40 | 40 | 48 | 56 | 64 | 64 |
| Maximum HP I/Os ⁽²⁾ | 208 | 416 | 416 | 520 | 572 | 650 | 676 |
| Maximum HR I/Os ⁽³⁾ | 104 | 104 | 104 | 104 | 104 | 52 | 156 |
| DSP Slices | 1,152 | 1,700 | 1,920 | 2,760 | 4,100 | 768 | 5,520 |
| System Monitor | 1 | 1 | 1 | 1 | 2 | 1 | 2 |
| PCIe Gen3 x8 | 1 | 2 | 3 | 3 | 4 | 4 | 6 |
| 150G Interlaken | 0 | 0 | 0 | 0 | 0 | 2 | 0 |
| 100G Ethernet | 0 | 0 | 0 | 0 | 0 | 2 | 0 |
| GTH 16.3Gb/s Transceivers ⁽⁴⁾ | 12 | 16 | 20 | 32 | 56 | 32 | 64 |
| GTY 16.3Gb/s Transceivers ⁽⁵⁾ | 0 | 0 | 0 | 0 | 0 | 32 | 0 |
| Transceiver Fractional PLLs | 0 | 0 | 0 | 0 | 0 | 16 | 0 |

Notes:

1. Certain advanced configuration features are not supported in the KU025. Refer to the [Configuring FPGAs](#) section for details.
2. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
3. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
4. GTH transceivers in SF/FB packages support data rates up to 12.5Gb/s. See [Table 4](#).
5. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s. See [Table 4](#).

Kintex UltraScale+ FPGA Feature Summary

Table 5: Kintex UltraScale+ FPGA Feature Summary

| | KU3P | KU5P | KU9P | KU11P | KU13P | KU15P |
|-------------------------------------------|---------|---------|---------|---------|---------|-----------|
| System Logic Cells | 355,950 | 474,600 | 599,550 | 653,100 | 746,550 | 1,143,450 |
| CLB Flip-Flops | 325,440 | 433,920 | 548,160 | 597,120 | 682,560 | 1,045,440 |
| CLB LUTs | 162,720 | 216,960 | 274,080 | 298,560 | 341,280 | 522,720 |
| Max. Distributed RAM (Mb) | 4.7 | 6.1 | 8.8 | 9.1 | 11.3 | 9.8 |
| Block RAM Blocks | 360 | 480 | 912 | 600 | 744 | 984 |
| Block RAM (Mb) | 12.7 | 16.9 | 32.1 | 21.1 | 26.2 | 34.6 |
| UltraRAM Blocks | 48 | 64 | 0 | 80 | 112 | 128 |
| UltraRAM (Mb) | 13.5 | 18.0 | 0 | 22.5 | 31.5 | 36.0 |
| CMTs (1 MMCM and 2 PLLs) | 4 | 4 | 4 | 8 | 4 | 11 |
| Max. HP I/O ⁽¹⁾ | 208 | 208 | 208 | 416 | 208 | 572 |
| Max. HD I/O ⁽²⁾ | 96 | 96 | 96 | 96 | 96 | 96 |
| DSP Slices | 1,368 | 1,824 | 2,520 | 2,928 | 3,528 | 1,968 |
| System Monitor | 1 | 1 | 1 | 1 | 1 | 1 |
| GTH Transceiver 16.3Gb/s | 0 | 0 | 28 | 32 | 28 | 44 |
| GTY Transceivers 32.75Gb/s ⁽³⁾ | 16 | 16 | 0 | 20 | 0 | 32 |
| Transceiver Fractional PLLs | 8 | 8 | 14 | 26 | 14 | 38 |
| PCIe Gen3 x16 and Gen4 x8 | 1 | 1 | 0 | 4 | 0 | 5 |
| 150G Interlaken | 0 | 0 | 0 | 1 | 0 | 4 |
| 100G Ethernet w/RS-FEC | 0 | 1 | 0 | 2 | 0 | 4 |

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTY transceiver line rates are package limited: SFVB784 to 12.5Gb/s; FFVA676, FFVD900, and FFVA1156 to 16.3Gb/s. See [Table 6](#).

Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 10: Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

| Package (1)(2)(3) | Package Dimensions (mm) | VU3P | VU5P | VU7P | VU9P | VU11P | VU13P | VU31P | VU33P | VU35P | VU37P |
|----------------------|-------------------------------|---------|---------|---------|----------|---------|----------|---------|---------|---------|---------|
| | | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY |
| FFVC1517 | 40x40 | 520, 40 | | | | | | | | | |
| FLGF1924(4) | 45x45 | | | | | 624, 64 | | | | | |
| FLVA2104 | 47.5x47.5 | | 832, 52 | 832, 52 | | | | | | | |
| FLGA2104 | 47.5x47.5 | | | | 832, 52 | | | | | | |
| FHGA2104 | 52.5x52.5(5) | | | | | | 832, 52 | | | | |
| FLVB2104 | 47.5x47.5 | | 702, 76 | 702, 76 | | | | | | | |
| FLGB2104 | 47.5x47.5 | | | | 702, 76 | 572, 76 | | | | | |
| FHGB2104 | 52.5x52.5(5) | | | | | | 702, 76 | | | | |
| FLVC2104 | 47.5x47.5 | | 416, 80 | 416, 80 | | | | | | | |
| FLGC2104 | 47.5x47.5 | | | | 416, 104 | 416, 96 | | | | | |
| FHGC2104 | 52.5x52.5(5) | | | | | | 416, 104 | | | | |
| FSGD2104 | 47.5x47.5 | | | | 676, 76 | 572, 76 | | | | | |
| FIGD2104 | 52.5x52.5(5) | | | | | | 676, 76 | | | | |
| FLGA2577 | 52.5x52.5 | | | | 448, 120 | 448, 96 | 448, 128 | | | | |
| FSVH1924 | 45x45 | | | | | | | 208, 32 | | | |
| FSVH2104 | 47.5x47.5 | | | | | | | | 208, 32 | 416, 64 | |
| FSVH2892 | 55x55 | | | | | | | | | 416, 64 | 624, 96 |

Notes:

- Go to [Ordering Information](#) for package designation details.
- All packages have 1.0mm ball pitch.
- Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.
- GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s.
- These 52.5x52.5mm overhang packages have the same PCB ball footprint as the corresponding 47.5x47.5mm packages (i.e., the same last letter and number sequence) and are footprint compatible.

Zynq UltraScale+: EG Device Feature Summary

Table 13: Zynq UltraScale+: EG Device Feature Summary

| | ZU2EG | ZU3EG | ZU4EG | ZU5EG | ZU6EG | ZU7EG | ZU9EG | ZU11EG | ZU15EG | ZU17EG | ZU19EG |
|-----------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|-----------|
| Application Processing Unit | Quad-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache | | | | | | | | | | |
| Real-Time Processing Unit | Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM | | | | | | | | | | |
| Embedded and External Memory | 256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC | | | | | | | | | | |
| General Connectivity | 214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters | | | | | | | | | | |
| High-Speed Connectivity | 4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII | | | | | | | | | | |
| Graphic Processing Unit | ARM Mali-400 MP2; 64KB L2 Cache | | | | | | | | | | |
| System Logic Cells | 103,320 | 154,350 | 192,150 | 256,200 | 469,446 | 504,000 | 599,550 | 653,100 | 746,550 | 926,194 | 1,143,450 |
| CLB Flip-Flops | 94,464 | 141,120 | 175,680 | 234,240 | 429,208 | 460,800 | 548,160 | 597,120 | 682,560 | 846,806 | 1,045,440 |
| CLB LUTs | 47,232 | 70,560 | 87,840 | 117,120 | 214,604 | 230,400 | 274,080 | 298,560 | 341,280 | 423,403 | 522,720 |
| Distributed RAM (Mb) | 1.2 | 1.8 | 2.6 | 3.5 | 6.9 | 6.2 | 8.8 | 9.1 | 11.3 | 8.0 | 9.8 |
| Block RAM Blocks | 150 | 216 | 128 | 144 | 714 | 312 | 912 | 600 | 744 | 796 | 984 |
| Block RAM (Mb) | 5.3 | 7.6 | 4.5 | 5.1 | 25.1 | 11.0 | 32.1 | 21.1 | 26.2 | 28.0 | 34.6 |
| UltraRAM Blocks | 0 | 0 | 48 | 64 | 0 | 96 | 0 | 80 | 112 | 102 | 128 |
| UltraRAM (Mb) | 0 | 0 | 14.0 | 18.0 | 0 | 27.0 | 0 | 22.5 | 31.5 | 28.7 | 36.0 |
| DSP Slices | 240 | 360 | 728 | 1,248 | 1,973 | 1,728 | 2,520 | 2,928 | 3,528 | 1,590 | 1,968 |
| CMTs | 3 | 3 | 4 | 4 | 4 | 8 | 4 | 8 | 4 | 11 | 11 |
| Max. HP I/O ⁽¹⁾ | 156 | 156 | 156 | 156 | 208 | 416 | 208 | 416 | 208 | 572 | 572 |
| Max. HD I/O ⁽²⁾ | 96 | 96 | 96 | 96 | 120 | 48 | 120 | 96 | 120 | 96 | 96 |
| System Monitor | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| GTH Transceiver 16.3Gb/s ⁽³⁾ | 0 | 0 | 16 | 16 | 24 | 24 | 24 | 32 | 24 | 44 | 44 |
| GTY Transceivers 32.75Gb/s | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 16 | 0 | 28 | 28 |
| Transceiver Fractional PLLs | 0 | 0 | 8 | 8 | 12 | 12 | 12 | 24 | 12 | 36 | 36 |
| PCIe Gen3 x16 and Gen4 x8 | 0 | 0 | 2 | 2 | 0 | 2 | 0 | 4 | 0 | 4 | 5 |
| 150G Interlaken | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 | 4 |
| 100G Ethernet w/ RS-FEC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 0 | 2 | 4 |

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 14](#).

Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

Table 14: Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

| Package (1)(2)(3)(4)(5) | Package Dimensions (mm) | ZU2EG | ZU3EG | ZU4EG | ZU5EG | ZU6EG | ZU7EG | ZU9EG | ZU11EG | ZU15EG | ZU17EG | ZU19EG |
|----------------------------|-------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| | | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY |
| SBVA484(6) | 19x19 | 24, 58 0, 0 | 24, 58 0, 0 | | | | | | | | | |
| SFVA625 | 21x21 | 24, 156 0, 0 | 24, 156 0, 0 | | | | | | | | | |
| SFVC784(7) | 23x23 | 96, 156 0, 0 | 96, 156 0, 0 | 96, 156 4, 0 | 96, 156 4, 0 | | | | | | | |
| FBVB900 | 31x31 | | | 48, 156 16, 0 | 48, 156 16, 0 | | 48, 156 16, 0 | | | | | |
| FFVC900 | 31x31 | | | | | 48, 156 16, 0 | | 48, 156 16, 0 | | 48, 156 16, 0 | | |
| FFVB1156 | 35x35 | | | | | 120, 208 24, 0 | | 120, 208 24, 0 | | 120, 208 24, 0 | | |
| FFVC1156 | 35x35 | | | | | | 48, 312 20, 0 | | 48, 312 20, 0 | | | |
| FFVB1517 | 40x40 | | | | | | | | 72, 416 16, 0 | | 72, 572 16, 0 | 72, 572 16, 0 |
| FFVF1517 | 40x40 | | | | | | 48, 416 24, 0 | | 48, 416 32, 0 | | | |
| FFVC1760 | 42.5x42.5 | | | | | | | | 96, 416 32, 16 | | 96, 416 32, 16 | 96, 416 32, 16 |
| FFVD1760 | 42.5x42.5 | | | | | | | | | | 48, 260 44, 28 | 48, 260 44, 28 |
| FFVE1924 | 45x45 | | | | | | | | | | 96, 572 44, 0 | 96, 572 44, 0 |

Notes:

- Go to [Ordering Information](#) for package designation details.
- FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
- All device package combinations bond out 4 PS-GTR transceivers.
- All device package combinations bond out 214 PS I/O except ZU2EG and ZU3EG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
- Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
- All 58 HP I/O pins are powered by the same V_{CCO} supply.
- GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. Figure 2 is a representation of an FPGA divided into regions.



Figure 2: Column-Based FPGA Divided into Clock Regions

Processing System (PS)

Zynq UltraScale+ MPSoCs consist of a PS coupled with programmable logic. The contents of the PS varies between the different Zynq UltraScale+ devices. All devices contain an APU, an RPU, and many peripherals for connecting the multiple processing engines to external components. The EG and EV devices contain a GPU and the EV devices contain a video codec unit (VCU). The components of the PS are connected together and to the PL through a multi-layered ARM AMBA AXI non-blocking interconnect that supports multiple simultaneous master-slave transactions. Traffic through the interconnect can be regulated by the quality of service (QoS) block in the interconnect. Twelve dedicated AXI 32-bit, 64-bit, or 128-bit ports connect the PL to high-speed interconnect and DDR in the PS via a FIFO interface.

There are four independently controllable power domains: the PL plus three within the PS (full power, lower power, and battery power domains). Additionally, many peripherals support clock gating and power gating to further reduce dynamic and static power consumption.

Application Processing Unit (APU)

The APU has a feature-rich dual-core or quad-core ARM Cortex-A53 processor. Cortex-A53 cores are 32-bit/64-bit application processors based on ARM-v8A architecture, offering the best performance-to-power ratio. The ARMv8 architecture supports hardware virtualization. Each of the Cortex-A53 cores has: 32KB of instruction and data L1 caches, with parity and ECC protection respectively; a NEON SIMD engine; and a single and double precision floating point unit. In addition to these blocks, the APU consists of a snoop control unit and a 1MB L2 cache with ECC protection to enhance system-level performance. The snoop control unit keeps the L1 caches coherent thus eliminating the need of spending software bandwidth for coherency. The APU also has a built-in interrupt controller supporting virtual interrupts. The APU communicates to the rest of the PS through 128-bit AXI coherent extension (ACE) port via Cache Coherent Interconnect (CCI) block, using the System Memory Management Unit (SMMU). The APU is also connected to the Programmable Logic (PL), through the 128-bit accelerator coherency port

(ACP), providing a low latency coherent port for accelerators in the PL. To support real-time debug and trace, each core also has an Embedded Trace Macrocell (ETM) that communicates with the ARM CoreSight™ Debug System.

Real-Time Processing Unit (RPU)

The RPU in the PS contains a dual-core ARM Cortex-R5 PS. Cortex-R5 cores are 32-bit real-time processor cores based on ARM-v7R architecture. Each of the Cortex-R5 cores has 32KB of level-1 (L1) instruction and data cache with ECC protection. In addition to the L1 caches, each of the Cortex-R5 cores also has a 128KB tightly coupled memory (TCM) interface for real-time single cycle access. The RPU also has a dedicated interrupt controller. The RPU can operate in either split or lock-step mode. In split mode, both processors run independently of each other. In lock-step mode, they run in parallel with each other, with integrated comparator logic, and the TCMs are used as 256KB unified memory. The RPU communicates with the rest of the PS via the 128-bit AXI-4 ports connected to the low power domain switch. It also communicates directly with the PL through 128-bit low latency AXI-4 ports. To support real-time debug and trace each core also has an embedded trace macrocell (ETM) that communicates with the ARM CoreSight Debug System.

External Memory

The PS can interface to many types of external memories through dedicated memory controllers. The dynamic memory controller supports DDR3, DDR3L, DDR4, LPDDR3, and LPDDR4 memories. The multi-protocol DDR memory controller can be configured to access a 2GB address space in 32-bit addressing mode and up to 32GB in 64-bit addressing mode using a single or dual rank configuration of 8-bit, 16-bit, or 32-bit DRAM memories. Both 32-bit and 64-bit bus access modes are protected by ECC using extra bits.

The SD/eMMC controller supports 1 and 4 bit data interfaces at low, default, high-speed, and ultra-high-speed (UHS) clock rates. This controller also supports 1-, 4-, or 8-bit-wide eMMC interfaces that are compliant to the eMMC 4.51 specification. eMMC is one of the primary boot and configuration modes for Zynq UltraScale+ MPSoCs and supports boot from managed NAND devices. The controller has a built-in DMA for enhanced performance.

The Quad-SPI controller is one of the primary boot and configuration devices. It supports 4-byte and 3-byte addressing modes. In both addressing modes, single, dual-stacked, and dual-parallel configurations are supported. Single mode supports a quad serial NOR flash memory, while in double stacked and double parallel modes, it supports two quad serial NOR flash memories.

The NAND controller is based on ONFI3.1 specification. It has an 8-pin interface and provides 200Mb/s of bandwidth in synchronous mode. It supports 24 bits of ECC thus enabling support for SLC NAND memories. It has two chip-selects to support deeper memory and a built-in DMA for enhanced performance.

General Connectivity

There are many peripherals in the PS for connecting to external devices over industry standard protocols, including CAN2.0B, USB, Ethernet, I2C, and UART. Many of the peripherals support clock gating and power gating modes to reduce dynamic and static power consumption.

USB 3.0/2.0

The pair of USB controllers can be configured as host, device, or On-The-Go (OTG). The core is compliant to USB 3.0 specification and supports super, high, full, and low speed modes in all configurations. In host mode, the USB controller is compliant with the Intel XHCI specification. In device mode, it supports up to 12 end points. While operating in USB 3.0 mode, the controller uses the serial transceiver and operates up to 5.0Gb/s. In USB 2.0 mode, the Universal Low Peripheral Interface (ULPI) is used to connect the controller to an external PHY operating up to 480Mb/s. The ULPI is also connected in USB 3.0 mode to support high-speed operations.

Ethernet MAC

The four tri-speed ethernet MACs support 10Mb/s, 100Mb/s, and 1Gb/s operations. The MACs support jumbo frames and time stamping through the interfaces based on IEEE Std 1588v2. The ethernet MACs can be connected through the serial transceivers (SGMII), the MIO (RGMII), or through EMIO (GMII). The GMII interface can be converted to a different interface within the PL.

High-Speed Connectivity

The PS includes four PS-GTR transceivers (transmit and receive), supporting data rates up to 6.0Gb/s and can interface to the peripherals for communication over PCIe, SATA, USB 3.0, SGMII, and DisplayPort.

PCIe

The integrated block for PCIe is compliant with PCI Express base specification 2.1 and supports x1, x2, and x4 configurations as root complex or end point, compliant to transaction ordering rules in both configurations. It has built-in DMA, supports one virtual channel and provides fully configurable base address registers.

SATA

Users can connect up to two external devices using the two SATA host port interfaces compliant to the SATA 3.1 specification. The SATA interfaces can operate at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates and are compliant with advanced host controller interface (AHCI) version 1.3 supporting partial and slumber power modes.

DisplayPort

The DisplayPort controller supports up to two lanes of source-only DisplayPort compliant with VESA DisplayPort v1.2a specification (source only) at 1.62Gb/s, 2.7Gb/s, and 5.4Gb/s data rates. The controller supports single stream transport (SST); video resolution up to 4Kx2K at a 30Hz frame rate; video formats Y-only, YCbCr444, YCbCr422, YCbCr420, RGB, YUV444, YUV422, xvYCC, and pixel color depth of 6, 8, 10, and 12 bits per color component.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100Ω internal resistor. All UltraScale devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. UltraScale+ families add support for MIPI with a dedicated D-PHY in the I/O bank.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

High-Speed Serial Transceivers

Serial data transmission between devices on the same PCB, over backplanes, and across even longer distances is becoming increasingly important for scaling to 100Gb/s and 400Gb/s line cards. Specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues are required at these high data rates.

Three types of transceivers are used in the UltraScale architecture: GTH and GTY in FPGAs and MPSoC PL, and PS-GTR in the MPSoC PS. All transceivers are arranged in groups of four, known as a transceiver Quad. Each serial transceiver is a combined transmitter and receiver. [Table 17](#) compares the available transceivers.

Table 17: Transceiver Information

| | Kintex UltraScale | | Kintex UltraScale+ | | Virtex UltraScale | | Virtex UltraScale+ | Zynq UltraScale+ | | |
|----------------|---------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|
| Type | GTH | GTY | GTH | GTY | GTH | GTY | GTY | PS-GTR | GTH | GTY |
| Qty | 16–64 | 0–32 | 20–60 | 0–60 | 20–60 | 0–60 | 40–128 | 4 | 0–44 | 0–28 |
| Max. Data Rate | 16.3Gb/s | 16.3Gb/s | 16.3Gb/s | 32.75Gb/s | 16.3Gb/s | 30.5Gb/s | 32.75Gb/s | 6.0Gb/s | 16.3Gb/s | 32.75Gb/s |
| Min. Data Rate | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 1.25Gb/s | 0.5Gb/s | 0.5Gb/s |
| Key Apps | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC | <ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC | <ul style="list-style-type: none"> PCIe Gen2 USB Ethernet | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC |

The following information in this section pertains to the GTH and GTY only.

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Cache Coherent Interconnect for Accelerators (CCIX)

CCIX is a chip-to-chip interconnect operating at data rates up to 25Gb/s that allows two or more devices to share memory in a cache coherent manner. Using PCIe for the transport layer, CCIX can operate at several standard data rates (2.5, 5, 8, and 16Gb/s) with an additional high-speed 25Gb/s option. The specification employs a subset of full coherency protocols and ensures that FPGAs used as accelerators can coherently share data with processors using different instruction set architectures.

Virtex UltraScale+ HBM devices support CCIX data rates up to 16Gb/s and contain four CCIX ports and at least four integrated blocks for PCIe. Each CCIX port requires the use of one integrated block for PCIe. If not used with a CCIX port, the integrated blocks for PCIe can still be used for PCIe communication.

Integrated Block for Interlaken

Some UltraScale architecture-based devices include integrated blocks for Interlaken. Interlaken is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gb/s to 150Gb/s. The Interlaken integrated block in the UltraScale architecture is compliant to revision 1.2 of the Interlaken specification with data striping and de-striping across 1 to 12 lanes. Permitted configurations are: 1 to 12 lanes at up to 12.5Gb/s and 1 to 6 lanes at up to 25.78125Gb/s, enabling flexible support for up to 150Gb/s per integrated block. With multiple Interlaken blocks, certain UltraScale devices enable easy, reliable Interlaken switches and bridges.

Integrated Block for 100G Ethernet

Compliant to the IEEE Std 802.3ba, the 100G Ethernet integrated blocks in the UltraScale architecture provide low latency 100Gb/s Ethernet ports with a wide range of user customization and statistics gathering. With support for 10 x 10.3125Gb/s (CAUI) and 4 x 25.78125Gb/s (CAUI-4) configurations, the integrated block includes both the 100G MAC and PCS logic with support for IEEE Std 1588v2 1-step and 2-step hardware timestamping.

In UltraScale+ devices, the 100G Ethernet blocks contain a Reed Solomon Forward Error Correction (RS-FEC) block, compliant to IEEE Std 802.3bj, that can be used with the Ethernet block or stand alone in user applications. These families also support OTN mapping mode in which the PCS can be operated without using the MAC.

Stacked Silicon Interconnect (SSI) Technology

Many challenges associated with creating high-capacity devices are addressed by Xilinx with the second generation of the pioneering 3D SSI technology. SSI technology enables multiple super-logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders, to create a single device with more than 20,000 low-power inter-SLR connections. Dedicated interface tiles within the SLRs provide ultra-high bandwidth, low latency connectivity to other SLRs. Table 19 shows the number of SLRs in devices that use SSI technology and their dimensions.

Table 19: UltraScale and UltraScale+ 3D IC SLR Count and Dimensions

| | Kintex UltraScale | | Virtex UltraScale | | | | Virtex UltraScale+ | | | | | | | | |
|-------------------------|-------------------|-------|-------------------|-------|-------|-------|--------------------|------|------|-------|-------|-------|-------|-------|-------|
| Device | KU085 | KU115 | VU125 | VU160 | VU190 | VU440 | VU5P | VU7P | VU9P | VU11P | VU13P | VU31P | VU33P | VU35P | VU37P |
| # SLRs | 2 | 2 | 2 | 3 | 3 | 3 | 2 | 2 | 3 | 3 | 4 | 1 | 1 | 2 | 3 |
| SLR Width (in regions) | 6 | 6 | 6 | 6 | 6 | 9 | 6 | 6 | 6 | 8 | 8 | 8 | 8 | 8 | 8 |
| SLR Height (in regions) | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 4 | 4 | 4 | 4 | 4 | 4 |

Clock Management

The clock generation and distribution components in UltraScale devices are located adjacent to the columns that contain the memory interface and input and output circuitry. This tight coupling of clocking and I/O provides low-latency clocking to the I/O for memory interfaces and other I/O protocols. Within every clock management tile (CMT) resides one mixed-mode clock manager (MMCM), two PLLs, clock distribution buffers and routing, and dedicated circuitry for implementing external memory interfaces.

Mixed-Mode Clock Manager

The mixed-mode clock manager (MMCM) can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of the MMCM is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers (D, M, and O) that are programmable by configuration and during normal operation via the Dynamic Reconfiguration Port (DRP). The pre-divider D reduces the input frequency and feeds one input of the phase/frequency comparator. The feedback divider M acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each phase can be selected to drive one of the output dividers, and each divider is programmable by configuration to divide by any integer from 1 to 128.

The MMCM has three input-jitter filter options: low bandwidth, high bandwidth, or optimized mode. Low-Bandwidth mode has the best jitter attenuation. High-Bandwidth mode has the best phase offset. Optimized mode allows the tools to find the best setting.

Interconnect

Various length vertical and horizontal routing resources in the UltraScale architecture that span 1, 2, 4, 5, 12, or 16 CLBs ensure that all signals can be transported from source to destination with ease, providing support for the next generation of wide data buses to be routed across even the highest capacity devices while simultaneously improving quality of results and software run time.

Digital Signal Processing

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All UltraScale devices have many dedicated, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 27×18 bit twos complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The 96-bit-wide XOR function, programmable to 12, 24, 48, or 96-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP also includes a 48-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

System Monitor

The System Monitor blocks in the UltraScale architecture are used to enhance the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors and external channels to the ADC.

All UltraScale architecture-based devices contain at least one System Monitor. The System Monitor in UltraScale+ FPGAs and the PL of Zynq UltraScale+ MPSoCs is similar to the Kintex UltraScale and Virtex UltraScale devices but with additional features including a PMBus interface.

Zynq UltraScale+ MPSoCs contain an additional System Monitor block in the PS. See [Table 20](#).

Table 20: Key System Monitor Features

| | Kintex UltraScale Virtex UltraScale | Kintex UltraScale+ Virtex UltraScale+ Zynq UltraScale+ MPSoC PL | Zynq UltraScale+ MPSoC PS |
|------------|------------------------------------------------|--------------------------------------------------------------------------------|----------------------------------|
| ADC | 10-bit 200kSPS | 10-bit 200kSPS | 10-bit 1MSPS |
| Interfaces | JTAG, I2C, DRP | JTAG, I2C, DRP, PMBus | APB |

In FPGAs and the MPSoC PL, sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, PMBus, or I2C interfaces. The I2C interface and PMBus allow the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

The System Monitor in the MPSoC PS uses a 10-bit, 1 mega-sample-per-second (MSPS) ADC to digitize the sensor outputs. The measurements are stored in registers and are accessed via the Advanced Peripheral Bus (APB) interface by the processors and the platform management unit (PMU) in the PS.

Configuration

The UltraScale architecture-based devices store their customized configuration in SRAM-type internal latches. The configuration storage is volatile and must be reloaded whenever the device is powered up. This storage can also be reloaded at any time. Several methods and data formats for loading configuration are available, determined by the mode pins, with more dedicated configuration datapath pins to simplify the configuration process.

UltraScale architecture-based devices support secure and non-secure boot with optional Advanced Encryption Standard - Galois/Counter Mode (AES-GCM) decryption and authentication logic. If only authentication is required, the UltraScale architecture provides an alternative form of authentication in the form of RSA algorithms. For RSA authentication support in the Kintex UltraScale and Virtex UltraScale families, go to [UG570](#), *UltraScale Architecture Configuration User Guide*.

UltraScale architecture-based devices also have the ability to select between multiple configurations, and support robust field-update methodologies. This is especially useful for updates to a design after the end product has been shipped. Designers can release their product with an early version of the design, thus getting their product to market faster. This feature allows designers to keep their customers current with the most up-to-date design while the product is already deployed in the field.

Booting MPSoCs

Zynq UltraScale+ MPSoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the AES-GCM, SHA-3/384 decryption/authentication, and 4096-bit RSA blocks decrypt and authenticate the image.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NAND, Quad-SPI, SD, eMMC, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. One of the CPUs, Cortex-A53 or Cortex-R5, executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip memory (OCM).

The ordering information shown in Figure 4 applies to all packages in the Kintex UltraScale+ and Virtex UltraScale+ FPGAs, and Figure 5 applies to Zynq UltraScale+.

The -1L and -2L speed grades in the UltraScale+ families can run at one of two different V_{CCINT} operating voltages. At 0.72V, they operate at similar performance to the Kintex UltraScale and Virtex UltraScale devices with up to 30% reduction in power consumption. At 0.85V, they consume similar power to the Kintex UltraScale and Virtex UltraScale devices, but operate over 30% faster.

For UltraScale+ devices, the information in this document is pre-release, provided ahead of silicon ordering availability. Please contact your Xilinx sales representative for more information on Early Access Programs.

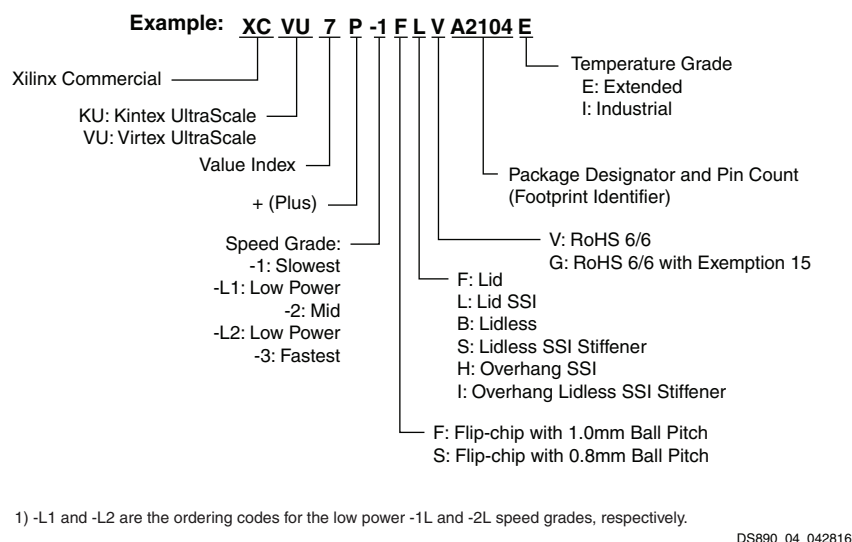


Figure 4: UltraScale+ FPGA Ordering Information

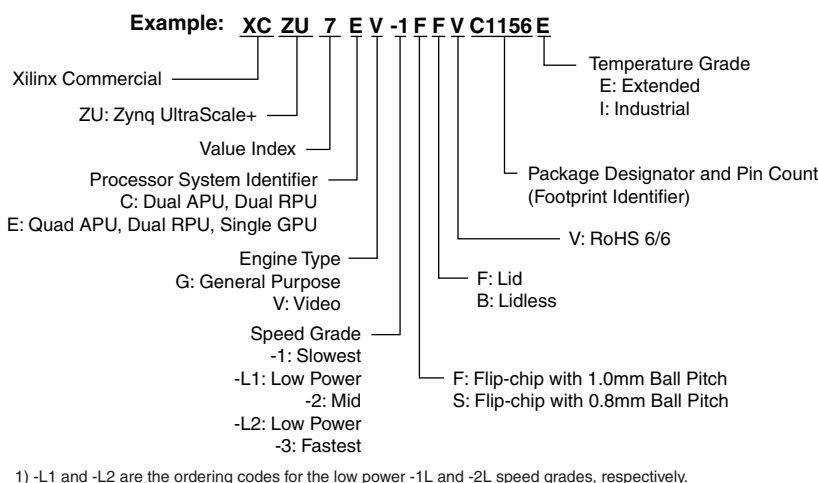


Figure 5: Zynq UltraScale+ Ordering Information

Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 02/15/2017 | 2.11 | Updated Table 1 , Table 9 : Converted HBM from Gb to GB. Updated Table 11 , Table 13 , and Table 15 : Updated DSP count for Zynq UltraScale+ MPSoCs. Updated Cache Coherent Interconnect for Accelerators (CCIX) . Updated High Bandwidth Memory (HBM) . Updated Table 21 : Added -2E speed grade to all UltraScale+ devices. Removed -3E from XCZU2 and XCZU3. |
| 11/09/2016 | 2.10 | Updated Table 1 . Added HBM devices to Table 9 , Table 10 , Table 19 and new High Bandwidth Memory (HBM) section. Added Cache Coherent Interconnect for Accelerators (CCIX) section. |
| 09/27/2016 | 2.9 | Updated Table 5 , Table 12 , Table 13 , and Table 14 . |
| 06/03/2016 | 2.8 | Added Zynq UltraScale+ MPSoC CG devices: Added Table 2 . Updated Table 11 , Table 12 , Table 21 , and Figure 5 . Created separate tables for EG and EV devices: Table 13 , Table 14 , Table 15 , and Table 16 . Updated Table 1 , Table 3 , Table 5 and notes, Table 6 and notes, Table 7 , Table 9 , Table 10 , Processing System Overview , and Processing System (PS) details. |
| 02/17/2016 | 2.7 | Added Migrating Devices . Updated Table 4 , Table 5 , Table 6 , Table 10 , Table 11 , Table 12 , and Figure 4 . |
| 12/15/2015 | 2.6 | Updated Table 1 , Table 5 , Table 6 , Table 9 , Table 12 , and Configuration . |
| 11/24/2015 | 2.5 | Updated Configuration, Encryption, and System Monitoring , Table 5 , Table 9 , Table 11 , and Table 21 . |
| 10/15/2015 | 2.4 | Updated Table 1 , Table 3 , Table 5 , Table 7 , Table 9 , and Table 11 with System Logic Cells. Updated Figure 3 . Updated Table 19 . |
| 09/29/2015 | 2.3 | Added A1156 to KU095 in Table 4 . Updated Table 5 . Updated Max. Distributed RAM in Table 9 . Updated Distributed RAM in Table 11 . Added Table 19 . Updated Table 21 . Updated Figure 3 . |
| 08/14/2015 | 2.2 | Updated Table 1 . Added XCKU025 to Table 3 , Table 4 , and Table 21 . Updated Table 7 , Table 9 , Table 11 , Table 12 , Table 18 . Updated System Monitor . Added voltage information to Table 21 . |
| 04/27/2015 | 2.1 | Updated Table 1 , Table 3 , Table 4 , Table 5 , Table 6 , Table 7 , Table 10 , Table 11 , Table 12 , Table 17 , I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken, Integrated Interface Blocks for PCI Express Designs , USB 3.0/2.0, Clock Management, System Monitor, and Figure 3 . |
| 02/23/2015 | 2.0 | UltraScale+ device information (Kintex UltraScale+ FPGA, Virtex UltraScale+ FPGA, and Zynq UltraScale+ MPSoC) added throughout document. |
| 12/16/2014 | 1.6 | Updated Table 1 ; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 3 , Table 7 ; Table 8 ; and Table 17 . |
| 11/17/2014 | 1.5 | Updated I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 1 ; Table 4 ; Table 7 ; Table 8 ; Table 17 ; Input/Output ; and Figure 3 . |
| 09/16/2014 | 1.4 | Updated Logic Cell information in Table 1 . Updated Table 3 ; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 7 ; Table 8 ; Integrated Block for 100G Ethernet ; and Figure 3 . |
| 05/20/2014 | 1.3 | Updated Table 8 . |
| 05/13/2014 | 1.2 | Added Ordering Information . Updated Table 1 , Clocks and Memory Interfaces , Table 3 , Table 7 (removed XCVU145; added XCVU190), Table 8 (removed XCVU145; removed FLVD1924 from XCVU160; added XCVU190; updated Table Notes), Table 17 , Integrated Interface Blocks for PCI Express Designs , and Integrated Block for Interlaken , and Memory Interfaces . |

| Date | Version | Description of Revisions |
|------------|---------|---------------------------------------------------------------------------------------------------------------------------------------|
| 02/06/2014 | 1.1 | Updated PCIe information in Table 1 and Table 3 . Added FFVJ1924 package to Table 8 . |
| 12/10/2013 | 1.0 | Initial Xilinx release. |

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