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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	89520
Number of Logic Elements/Cells	1566600
Total RAM Bits	90726400
Number of I/O	416
Number of Gates	-
Voltage - Supply	0.922V ~ 0.979V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	2104-BBGA, FCBGA
Supplier Device Package	2104-FCBGA (47.5x47.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcvu125-2flvc2104e

Migrating Devices

UltraScale and UltraScale+ families provide footprint compatibility to enable users to migrate designs from one device or family to another. Any two packages with the same footprint identifier code are footprint compatible. For example, Kintex UltraScale devices in the A1156 packages are footprint compatible with Kintex UltraScale+ devices in the A1156 packages. Likewise, Virtex UltraScale devices in the B2104 packages are compatible with Virtex UltraScale+ devices and Kintex UltraScale devices in the B2104 packages. All valid device/package combinations are provided in the Device-Package Combinations and Maximum I/Os tables in this document. Refer to [UG583](#), *UltraScale Architecture PCB Design User Guide* for more detail on migrating between UltraScale and UltraScale+ devices and packages.

Kintex UltraScale FPGA Feature Summary

Table 3: Kintex UltraScale FPGA Feature Summary

	KU025 ⁽¹⁾	KU035	KU040	KU060	KU085	KU095	KU115
System Logic Cells	318,150	444,343	530,250	725,550	1,088,325	1,176,000	1,451,100
CLB Flip-Flops	290,880	406,256	484,800	663,360	995,040	1,075,200	1,326,720
CLB LUTs	145,440	203,128	242,400	331,680	497,520	537,600	663,360
Maximum Distributed RAM (Mb)	4.1	5.9	7.0	9.1	13.4	4.7	18.3
Block RAM Blocks	360	540	600	1,080	1,620	1,680	2,160
Block RAM (Mb)	12.7	19.0	21.1	38.0	56.9	59.1	75.9
CMTs (1 MMCM, 2 PLLs)	6	10	10	12	22	16	24
I/O DLLs	24	40	40	48	56	64	64
Maximum HP I/Os ⁽²⁾	208	416	416	520	572	650	676
Maximum HR I/Os ⁽³⁾	104	104	104	104	104	52	156
DSP Slices	1,152	1,700	1,920	2,760	4,100	768	5,520
System Monitor	1	1	1	1	2	1	2
PCIe Gen3 x8	1	2	3	3	4	4	6
150G Interlaken	0	0	0	0	0	2	0
100G Ethernet	0	0	0	0	0	2	0
GTH 16.3Gb/s Transceivers ⁽⁴⁾	12	16	20	32	56	32	64
GTY 16.3Gb/s Transceivers ⁽⁵⁾	0	0	0	0	0	32	0
Transceiver Fractional PLLs	0	0	0	0	0	16	0

Notes:

1. Certain advanced configuration features are not supported in the KU025. Refer to the [Configuring FPGAs](#) section for details.
2. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
3. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
4. GTH transceivers in SF/FB packages support data rates up to 12.5Gb/s. See [Table 4](#).
5. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s. See [Table 4](#).

Kintex UltraScale Device-Package Combinations and Maximum I/Os

Table 4: Kintex UltraScale Device-Package Combinations and Maximum I/Os

Package (1)(2)(3)	Package Dimensions (mm)	KU025	KU035	KU040	KU060	KU085	KU095	KU115
		HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH, GTY ⁽⁴⁾	HR, HP GTH
SFVA784 ⁽⁵⁾	23x23		104, 364 8	104, 364 8				
FBVA676 ⁽⁵⁾	27x27		104, 208 16	104, 208 16				
FBVA900 ⁽⁵⁾	31x31		104, 364 16	104, 364 16				
FFVA1156	35x35	104, 208 12	104, 416 16	104, 416 20	104, 416 28		52, 468 20, 8	
FFVA1517	40x40				104, 520 32			
FLVA1517	40x40					104, 520 48		104, 520 48
FFVC1517	40x40						52, 468 20, 20	
FLVD1517	40x40							104, 234 64
FFVB1760	42.5x42.5						52, 650 32, 16	
FLVB1760	42.5x42.5					104, 572 44		104, 598 52
FLVD1924	45x45							156, 676 52
FLVF1924	45x45					104, 520 56		104, 624 64
FLVA2104	47.5x47.5							156, 676 52
FFVB2104	47.5x47.5						52, 650 32, 32	
FLVB2104	47.5x47.5							104, 598 64

Notes:

- Go to [Ordering Information](#) for package designation details.
- FB/FF/FL packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
- Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.
- GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s.
- GTH transceivers in SF/FB packages support data rates up to 12.5Gb/s.

Kintex UltraScale+ FPGA Feature Summary

Table 5: Kintex UltraScale+ FPGA Feature Summary

	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P
System Logic Cells	355,950	474,600	599,550	653,100	746,550	1,143,450
CLB Flip-Flops	325,440	433,920	548,160	597,120	682,560	1,045,440
CLB LUTs	162,720	216,960	274,080	298,560	341,280	522,720
Max. Distributed RAM (Mb)	4.7	6.1	8.8	9.1	11.3	9.8
Block RAM Blocks	360	480	912	600	744	984
Block RAM (Mb)	12.7	16.9	32.1	21.1	26.2	34.6
UltraRAM Blocks	48	64	0	80	112	128
UltraRAM (Mb)	13.5	18.0	0	22.5	31.5	36.0
CMTs (1 MMCM and 2 PLLs)	4	4	4	8	4	11
Max. HP I/O ⁽¹⁾	208	208	208	416	208	572
Max. HD I/O ⁽²⁾	96	96	96	96	96	96
DSP Slices	1,368	1,824	2,520	2,928	3,528	1,968
System Monitor	1	1	1	1	1	1
GTH Transceiver 16.3Gb/s	0	0	28	32	28	44
GTY Transceivers 32.75Gb/s ⁽³⁾	16	16	0	20	0	32
Transceiver Fractional PLLs	8	8	14	26	14	38
PCIe Gen3 x16 and Gen4 x8	1	1	0	4	0	5
150G Interlaken	0	0	0	1	0	4
100G Ethernet w/RS-FEC	0	1	0	2	0	4

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTY transceiver line rates are package limited: SFVB784 to 12.5Gb/s; FFVA676, FFVD900, and FFVA1156 to 16.3Gb/s. See [Table 6](#).

Virtex UltraScale FPGA Feature Summary

Table 7: Virtex UltraScale FPGA Feature Summary

	VU065	VU080	VU095	VU125	VU160	VU190	VU440
System Logic Cells	783,300	975,000	1,176,000	1,566,600	2,026,500	2,349,900	5,540,850
CLB Flip-Flops	716,160	891,424	1,075,200	1,432,320	1,852,800	2,148,480	5,065,920
CLB LUTs	358,080	445,712	537,600	716,160	926,400	1,074,240	2,532,960
Maximum Distributed RAM (Mb)	4.8	3.9	4.8	9.7	12.7	14.5	28.7
Block RAM Blocks	1,260	1,421	1,728	2,520	3,276	3,780	2,520
Block RAM (Mb)	44.3	50.0	60.8	88.6	115.2	132.9	88.6
CMT (1 MMCM, 2 PLLs)	10	16	16	20	28	30	30
I/O DLLs	40	64	64	80	120	120	120
Maximum HP I/Os ⁽¹⁾	468	780	780	780	650	650	1,404
Maximum HR I/Os ⁽²⁾	52	52	52	104	52	52	52
DSP Slices	600	672	768	1,200	1,560	1,800	2,880
System Monitor	1	1	1	2	3	3	3
PCIe Gen3 x8	2	4	4	4	4	6	6
150G Interlaken	3	6	6	6	8	9	0
100G Ethernet	3	4	4	6	9	9	3
GTH 16.3Gb/s Transceivers	20	32	32	40	52	60	48
GTY 30.5Gb/s Transceivers	20	32	32	40	52	60	0
Transceiver Fractional PLLs	10	16	16	20	26	30	0

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

Virtex UltraScale+ FPGA Feature Summary

Table 9: Virtex UltraScale+ FPGA Feature Summary

	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
System Logic Cells	862,050	1,313,763	1,724,100	2,586,150	2,835,000	3,780,000	961,800	961,800	1,906,800	2,851,800
CLB Flip-Flops	788,160	1,201,154	1,576,320	2,364,480	2,592,000	3,456,000	879,360	879,360	1,743,360	2,607,360
CLB LUTs	394,080	600,577	788,160	1,182,240	1,296,000	1,728,000	439,680	439,680	871,680	1,303,680
Max. Distributed RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	12.5	12.5	24.6	36.7
Block RAM Blocks	720	1,024	1,440	2,160	2,016	2,688	672	672	1,344	2,016
Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	23.6	23.6	47.3	70.9
UltraRAM Blocks	320	470	640	960	960	1,280	320	320	640	960
UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	90.0	90.0	180.0	270.0
HBM DRAM (GB)	–	–	–	–	–	–	4	8	8	8
CMTs (1 MMCM and 2 PLLs)	10	20	20	30	12	16	4	4	8	12
Max. HP I/O ⁽¹⁾	520	832	832	832	624	832	208	208	416	624
DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	2,880	2,880	5,952	9,024
System Monitor	1	2	2	3	3	4	1	1	2	3
GTY Transceivers 32.75Gb/s ⁽²⁾	40	80	80	120	96	128	32	32	64	96
Transceiver Fractional PLLs	20	40	40	60	48	64	16	16	32	48
PCIe Gen3 x16 and Gen4 x8	2	4	4	6	3	4	4	4	5	6
CCIX Ports ⁽³⁾	–	–	–	–	–	–	4	4	4	4
150G Interlaken	3	4	6	9	6	8	0	0	2	4
100G Ethernet w/RS-FEC	3	4	6	9	9	12	2	2	5	8

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s. See [Table 10](#).
3. A CCIX port requires the use of a PCIe Gen3 x16 / Gen4 x8 block.

Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 10: Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

Package (1)(2)(3)	Package Dimensions (mm)	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
		HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY
FFVC1517	40x40	520, 40									
FLGF1924(4)	45x45					624, 64					
FLVA2104	47.5x47.5		832, 52	832, 52							
FLGA2104	47.5x47.5				832, 52						
FHGA2104	52.5x52.5(5)						832, 52				
FLVB2104	47.5x47.5		702, 76	702, 76							
FLGB2104	47.5x47.5				702, 76	572, 76					
FHGB2104	52.5x52.5(5)						702, 76				
FLVC2104	47.5x47.5		416, 80	416, 80							
FLGC2104	47.5x47.5				416, 104	416, 96					
FHGC2104	52.5x52.5(5)						416, 104				
FSGD2104	47.5x47.5				676, 76	572, 76					
FIGD2104	52.5x52.5(5)						676, 76				
FLGA2577	52.5x52.5				448, 120	448, 96	448, 128				
FSVH1924	45x45							208, 32			
FSVH2104	47.5x47.5								208, 32	416, 64	
FSVH2892	55x55									416, 64	624, 96

Notes:

- Go to [Ordering Information](#) for package designation details.
- All packages have 1.0mm ball pitch.
- Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.
- GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s.
- These 52.5x52.5mm overhang packages have the same PCB ball footprint as the corresponding 47.5x47.5mm packages (i.e., the same last letter and number sequence) and are footprint compatible.

General Connectivity

There are many peripherals in the PS for connecting to external devices over industry standard protocols, including CAN2.0B, USB, Ethernet, I2C, and UART. Many of the peripherals support clock gating and power gating modes to reduce dynamic and static power consumption.

USB 3.0/2.0

The pair of USB controllers can be configured as host, device, or On-The-Go (OTG). The core is compliant to USB 3.0 specification and supports super, high, full, and low speed modes in all configurations. In host mode, the USB controller is compliant with the Intel XHCI specification. In device mode, it supports up to 12 end points. While operating in USB 3.0 mode, the controller uses the serial transceiver and operates up to 5.0Gb/s. In USB 2.0 mode, the Universal Low Peripheral Interface (ULPI) is used to connect the controller to an external PHY operating up to 480Mb/s. The ULPI is also connected in USB 3.0 mode to support high-speed operations.

Ethernet MAC

The four tri-speed ethernet MACs support 10Mb/s, 100Mb/s, and 1Gb/s operations. The MACs support jumbo frames and time stamping through the interfaces based on IEEE Std 1588v2. The ethernet MACs can be connected through the serial transceivers (SGMII), the MIO (RGMII), or through EMIO (GMII). The GMII interface can be converted to a different interface within the PL.

High-Speed Connectivity

The PS includes four PS-GTR transceivers (transmit and receive), supporting data rates up to 6.0Gb/s and can interface to the peripherals for communication over PCIe, SATA, USB 3.0, SGMII, and DisplayPort.

PCIe

The integrated block for PCIe is compliant with PCI Express base specification 2.1 and supports x1, x2, and x4 configurations as root complex or end point, compliant to transaction ordering rules in both configurations. It has built-in DMA, supports one virtual channel and provides fully configurable base address registers.

SATA

Users can connect up to two external devices using the two SATA host port interfaces compliant to the SATA 3.1 specification. The SATA interfaces can operate at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates and are compliant with advanced host controller interface (AHCI) version 1.3 supporting partial and slumber power modes.

DisplayPort

The DisplayPort controller supports up to two lanes of source-only DisplayPort compliant with VESA DisplayPort v1.2a specification (source only) at 1.62Gb/s, 2.7Gb/s, and 5.4Gb/s data rates. The controller supports single stream transport (SST); video resolution up to 4Kx2K at a 30Hz frame rate; video formats Y-only, YCbCr444, YCbCr422, YCbCr420, RGB, YUV444, YUV422, xvYCC, and pixel color depth of 6, 8, 10, and 12 bits per color component.

Graphics Processing Unit (GPU)

The dedicated ARM Mali-400 MP2 GPU in the PS supports 2D and 3D graphics acceleration up to 1080p resolution. The Mali-400 supports OpenGL ES 1.1 and 2.0 for 3D graphics and Open VG 1.1 standards for 2D vector graphics. It has a geometry processor (GP) and 2 pixel processors to perform tile rendering operations in parallel. It has dedicated Memory management units for GP and pixel processors, which supports 4 KB page size. The GPU also has 64KB level-2 (L2) read-only cache. It supports 4X and 16X Full scene Anti-Aliasing (FSAA). It is fully autonomous, enabling maximum parallelization between APU and GPU. It has built-in hardware texture decompression, allowing the texture to remain compressed (in ETC format) in graphics hardware and decompress the required samples on the fly. It also supports efficient alpha blending of multiple layers in hardware without additional bandwidth consumption. It has a pixel fill rate of 2Mpixel/sec/MHz and a triangle rate of 0.1Mvertex/sec/MHz. The GPU supports extensive texture format for RGBA 8888, 565, and 1556 in Mono 8, 16, and YUV formats. For power sensitive applications, the GPU supports clock and power gating for each GP, pixel processors, and L2 cache. During power gating, GPU does not consume any static or dynamic power; during clock gating, it only consumes static power.

Video Codec Unit (VCU)

The video codec unit (VCU) provides multi-standard video encoding and decoding capabilities, including: High Efficiency Video Coding (HEVC), i.e., H.265; and Advanced Video Coding (AVC), i.e., H.264 standards. The VCU is capable of simultaneous encode and decode at rates up to 4Kx2K at 60 frames per second (fps) (approx. 600Mpixel/sec) or 8Kx4K at a reduced frame rate (~15fps).

Input/Output

All UltraScale devices, whether FPGA or MPSoC, have I/O pins for communicating to external components. In addition, in the MPSoC's PS, there are another 78 I/Os that the I/O peripherals use to communicate to external components, referred to as multiplexed I/O (MIO). If more than 78 pins are required by the I/O peripherals, the I/O pins in the PL can be used to extend the MPSoC interfacing capability, referred to as extended MIO (EMIO).

The number of I/O pins in UltraScale FPGAs and in the programmable logic of UltraScale+ MPSoCs varies depending on device and package. Each I/O is configurable and can comply with a large number of I/O standards. The I/Os are classed as high-range (HR), high-performance (HP), or high-density (HD). The HR I/Os offer the widest range of voltage support, from 1.2V to 3.3V. The HP I/Os are optimized for highest performance operation, from 1.0V to 1.8V. The HD I/Os are reduced-feature I/Os organized in banks of 24, providing voltage support from 1.2V to 3.3V.

All I/O pins are organized in banks, with 52 HP or HR pins per bank or 24 HD pins per bank. Each bank has one common V_{CCO} output buffer power supply, which also powers certain input buffers. In addition, HR banks can be split into two half-banks, each with their own V_{CCO} supply. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). V_{REF} pins can be driven directly from the PCB or internally generated using the internal V_{REF} generator circuitry present in each bank.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100Ω internal resistor. All UltraScale devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. UltraScale+ families add support for MIPI with a dedicated D-PHY in the I/O bank.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally “auto-adapt” to automatically learn and compensate for different interconnect characteristics. This enables even more margin for 10G+ and 25G+ backplanes.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

Integrated Interface Blocks for PCI Express Designs

The UltraScale architecture includes integrated blocks for PCIe technology that can be configured as an Endpoint or Root Port. UltraScale devices are compliant to the PCI Express Base Specification Revision 3.0. UltraScale+ devices are compliant to the PCI Express Base Specification Revision 3.1 for Gen3 and lower data rates, and compatible with the PCI Express Base Specification Revision 4.0 (rev 0.5) for Gen4 data rates.

The Root Port can be used to build the basis for a compatible Root Complex, to allow custom chip-to-chip communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the FPGA or MPSoC.

This block is highly configurable to system design requirements and can operate up to the maximum lane widths and data rates listed in [Table 18](#).

Table 18: PCIe Maximum Configurations

	Kintex UltraScale	Kintex UltraScale+	Virtex UltraScale	Virtex UltraScale+	Zynq UltraScale+
Gen1 (2.5Gb/s)	x8	x16	x8	x16	x16
Gen2 (5Gb/s)	x8	x16	x8	x16	x16
Gen3 (8Gb/s)	x8	x16	x8	x16	x16
Gen4 (16Gb/s) ⁽¹⁾		x8		x8	x8

Notes:

1. Transceivers in Kintex UltraScale and Virtex UltraScale devices are capable of operating at Gen4 data rates.

For high-performance applications, advanced buffering techniques of the block offer a flexible maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block for PCIe, the transceivers, block RAM, and clocking resources) into an Endpoint or Root Port solution. The system designer has control over many configurable parameters: link width and speed, maximum payload size, FPGA or MPSoC logic interface speeds, reference clock frequency, and base address register decoding and filtering.

Cache Coherent Interconnect for Accelerators (CCIX)

CCIX is a chip-to-chip interconnect operating at data rates up to 25Gb/s that allows two or more devices to share memory in a cache coherent manner. Using PCIe for the transport layer, CCIX can operate at several standard data rates (2.5, 5, 8, and 16Gb/s) with an additional high-speed 25Gb/s option. The specification employs a subset of full coherency protocols and ensures that FPGAs used as accelerators can coherently share data with processors using different instruction set architectures.

Virtex UltraScale+ HBM devices support CCIX data rates up to 16Gb/s and contain four CCIX ports and at least four integrated blocks for PCIe. Each CCIX port requires the use of one integrated block for PCIe. If not used with a CCIX port, the integrated blocks for PCIe can still be used for PCIe communication.

Integrated Block for Interlaken

Some UltraScale architecture-based devices include integrated blocks for Interlaken. Interlaken is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gb/s to 150Gb/s. The Interlaken integrated block in the UltraScale architecture is compliant to revision 1.2 of the Interlaken specification with data striping and de-striping across 1 to 12 lanes. Permitted configurations are: 1 to 12 lanes at up to 12.5Gb/s and 1 to 6 lanes at up to 25.78125Gb/s, enabling flexible support for up to 150Gb/s per integrated block. With multiple Interlaken blocks, certain UltraScale devices enable easy, reliable Interlaken switches and bridges.

Integrated Block for 100G Ethernet

Compliant to the IEEE Std 802.3ba, the 100G Ethernet integrated blocks in the UltraScale architecture provide low latency 100Gb/s Ethernet ports with a wide range of user customization and statistics gathering. With support for 10 x 10.3125Gb/s (CAUI) and 4 x 25.78125Gb/s (CAUI-4) configurations, the integrated block includes both the 100G MAC and PCS logic with support for IEEE Std 1588v2 1-step and 2-step hardware timestamping.

In UltraScale+ devices, the 100G Ethernet blocks contain a Reed Solomon Forward Error Correction (RS-FEC) block, compliant to IEEE Std 802.3bj, that can be used with the Ethernet block or stand alone in user applications. These families also support OTN mapping mode in which the PCS can be operated without using the MAC.

Block RAM

Every UltraScale architecture-based device contains a number of 36 Kb block RAMs, each with two completely independent ports that share only the stored data. Each block RAM can be configured as one 36Kb RAM or two independent 18Kb RAMs. Each memory access, read or write, is controlled by the clock. Connections in every block RAM column enable signals to be cascaded between vertically adjacent block RAMs, providing an easy method to create large, fast memory arrays, and FIFOs with greatly reduced power consumption.

All inputs, data, address, clock enables, and write enables are registered. The input address is always clocked (unless address latching is turned off), retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency. During a write operation, the data output can reflect either the previously stored data or the newly written data, or it can remain unchanged. Block RAM sites that remain unused in the user design are automatically powered down to reduce total power consumption. There is an additional pin on every block RAM to control the dynamic power gating feature.

Programmable Data Width

Each port can be configured as $32K \times 1$; $16K \times 2$; $8K \times 4$; $4K \times 9$ (or 8); $2K \times 18$ (or 16); $1K \times 36$ (or 32); or 512×72 (or 64). Whether configured as block RAM or FIFO, the two ports can have different aspect ratios without any constraints. Each block RAM can be divided into two completely independent 18Kb block RAMs that can each be configured to any aspect ratio from $16K \times 1$ to 512×36 . Everything described previously for the full 36Kb block RAM also applies to each of the smaller 18Kb block RAMs. Only in simple dual-port (SDP) mode can data widths of greater than 18bits (18Kb RAM) or 36 bits (36Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72. Both sides of the dual-port 36Kb RAM can be of variable width.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

Each block RAM can be configured as a 36Kb FIFO or an 18Kb FIFO. The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, programmable full, and programmable empty. The programmable flags allow the user to specify the FIFO counter values that make these flags go active. The FIFO width and depth are programmable with support for different read port and write port widths on a single FIFO. A dedicated cascade path allows for easy creation of deeper FIFOs.

UltraRAM

UltraRAM is a high-density, dual-port, synchronous memory block available in UltraScale+ devices. Both of the ports share the same clock and can address all of the 4K x 72 bits. Each port can independently read from or write to the memory array. UltraRAM supports two types of write enable schemes. The first mode is consistent with the block RAM byte write enable mode. The second mode allows gating the data and parity byte writes separately. UltraRAM blocks can be connected together to create larger memory arrays. Dedicated routing in the UltraRAM column enables the entire column height to be connected together. If additional density is required, all the UltraRAM columns in an SLR can be connected together with a few fabric resources to create single instances of RAM approximately 100Mb in size. This makes UltraRAM an ideal solution for replacing external memories such as SRAM. Cascadable anywhere from 288Kb to 100Mb, UltraRAM provides the flexibility to fulfill many different memory requirements.

Error Detection and Correction

Each 64-bit-wide UltraRAM can generate, store and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process.

High Bandwidth Memory (HBM)

Virtex UltraScale+ HBM devices incorporate 4GB HBM stacks adjacent to the FPGA die. Using stacked silicon interconnect technology, the FPGA communicates to the HBM stacks through memory controllers that connect to dedicated low-inductance interconnect in the silicon interposer. Each Virtex UltraScale+ HBM FPGA contains one or two HBM stacks, resulting in up to 8GB of HBM per FPGA.

The FPGA has 32 HBM AXI interfaces used to communicate with the HBM. Through a built-in switch mechanism, any of the 32 HBM AXI interfaces can access any memory address on either one or both of the HBM stacks due to the flexible addressing feature. This flexible connection between the FPGA and the HBM stacks results in easy floorplanning and timing closure. The memory controllers perform read and write reordering to improve bus efficiency. Data integrity is ensured through error checking and correction (ECC) circuitry.

Configurable Logic Block

Every Configurable Logic Block (CLB) in the UltraScale architecture contains 8 LUTs and 16 flip-flops. The LUTs can be configured as either one 6-input LUT with one output, or as two 5-input LUTs with separate outputs but common inputs. Each LUT can optionally be registered in a flip-flop. In addition to the LUTs and flip-flops, the CLB contains arithmetic carry logic and multiplexers to create wider logic functions.

Each CLB contains one slice. There are two types of slices: SLICEL and SLICEM. LUTs in the SLICEM can be configured as 64-bit RAM, as 32-bit shift registers (SRL32), or as two SRL16s. CLBs in the UltraScale architecture have increased routing and connectivity compared to CLBs in previous-generation Xilinx devices. They also have additional control signals to enable superior register packing, resulting in overall higher device utilization.

Zynq UltraScale+ MPSoCs contain an additional System Monitor block in the PS. See [Table 20](#).

Table 20: Key System Monitor Features

	Kintex UltraScale Virtex UltraScale	Kintex UltraScale+ Virtex UltraScale+ Zynq UltraScale+ MPSoC PL	Zynq UltraScale+ MPSoC PS
ADC	10-bit 200kSPS	10-bit 200kSPS	10-bit 1MSPS
Interfaces	JTAG, I2C, DRP	JTAG, I2C, DRP, PMBus	APB

In FPGAs and the MPSoC PL, sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, PMBus, or I2C interfaces. The I2C interface and PMBus allow the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

The System Monitor in the MPSoC PS uses a 10-bit, 1 mega-sample-per-second (MSPS) ADC to digitize the sensor outputs. The measurements are stored in registers and are accessed via the Advanced Peripheral Bus (APB) interface by the processors and the platform management unit (PMU) in the PS.

Configuration

The UltraScale architecture-based devices store their customized configuration in SRAM-type internal latches. The configuration storage is volatile and must be reloaded whenever the device is powered up. This storage can also be reloaded at any time. Several methods and data formats for loading configuration are available, determined by the mode pins, with more dedicated configuration datapath pins to simplify the configuration process.

UltraScale architecture-based devices support secure and non-secure boot with optional Advanced Encryption Standard - Galois/Counter Mode (AES-GCM) decryption and authentication logic. If only authentication is required, the UltraScale architecture provides an alternative form of authentication in the form of RSA algorithms. For RSA authentication support in the Kintex UltraScale and Virtex UltraScale families, go to [UG570](#), *UltraScale Architecture Configuration User Guide*.

UltraScale architecture-based devices also have the ability to select between multiple configurations, and support robust field-update methodologies. This is especially useful for updates to a design after the end product has been shipped. Designers can release their product with an early version of the design, thus getting their product to market faster. This feature allows designers to keep their customers current with the most up-to-date design while the product is already deployed in the field.

Booting MPSoCs

Zynq UltraScale+ MPSoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the AES-GCM, SHA-3/384 decryption/authentication, and 4096-bit RSA blocks decrypt and authenticate the image.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NAND, Quad-SPI, SD, eMMC, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. One of the CPUs, Cortex-A53 or Cortex-R5, executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip memory (OCM).

Table 21: Speed Grade and Temperature Grade (Cont'd)

Device Family	Devices	Speed Grade and Temperature Grade			
		Commercial (C)	Extended (E)		Industrial (I)
		0°C to +85°C	0°C to +100°C	0°C to +110°C	–40°C to +100°C
Zynq UltraScale+	CG Devices		-2E (0.85V)		-2I (0.85V)
				-2LE ⁽²⁾⁽³⁾ (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI ⁽³⁾ (0.85V or 0.72V)
	ZU2EG ZU3EG		-2E (0.85V)		-2I (0.85V)
				-2LE ⁽²⁾⁽³⁾ (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI ⁽³⁾ (0.85V or 0.72V)
	ZU4EG ZU5EG ZU6EG ZU7EG ZU9EG ZU11EG ZU15EG ZU17EG ZU19EG		-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE ⁽²⁾⁽³⁾ (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI ⁽³⁾ (0.85V or 0.72V)
	EV Devices		-3E (0.90V)		
			-2E (0.85V)		-2I (0.85V)
				-2LE ⁽²⁾⁽³⁾ (0.85V or 0.72V)	
			-1E (0.85V)		-1I (0.85V)
					-1LI ⁽³⁾ (0.85V or 0.72V)

Notes:

1. KU025 and KU095 are not available in -3E or -1LI speed/temperature grades.
2. In -2LE speed/temperature grade, devices can operate for a limited time with junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal at 0.85V or low voltage at 0.72V). Operation at 110°C Tj is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of device lifetime.
3. In Zynq UltraScale+ MPSoCs, when operating the PL at low voltage (0.72V), the PS operates at nominal voltage (0.85V).

The ordering information shown in Figure 4 applies to all packages in the Kintex UltraScale+ and Virtex UltraScale+ FPGAs, and Figure 5 applies to Zynq UltraScale+.

The -1L and -2L speed grades in the UltraScale+ families can run at one of two different V_{CCINT} operating voltages. At 0.72V, they operate at similar performance to the Kintex UltraScale and Virtex UltraScale devices with up to 30% reduction in power consumption. At 0.85V, they consume similar power to the Kintex UltraScale and Virtex UltraScale devices, but operate over 30% faster.

For UltraScale+ devices, the information in this document is pre-release, provided ahead of silicon ordering availability. Please contact your Xilinx sales representative for more information on Early Access Programs.

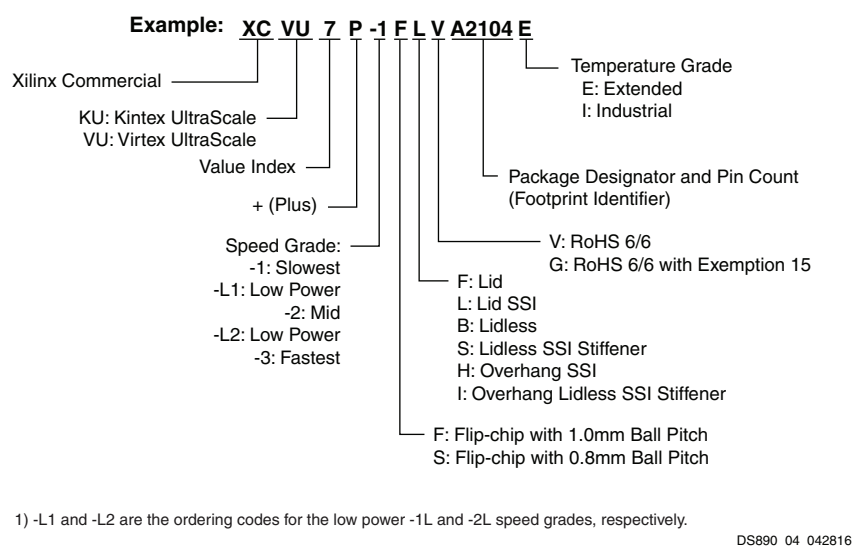


Figure 4: UltraScale+ FPGA Ordering Information



Figure 5: Zynq UltraScale+ Ordering Information

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/15/2017	2.11	Updated Table 1 , Table 9 : Converted HBM from Gb to GB. Updated Table 11 , Table 13 , and Table 15 : Updated DSP count for Zynq UltraScale+ MPSoCs. Updated Cache Coherent Interconnect for Accelerators (CCIX) . Updated High Bandwidth Memory (HBM) . Updated Table 21 : Added -2E speed grade to all UltraScale+ devices. Removed -3E from XCZU2 and XCZU3.
11/09/2016	2.10	Updated Table 1 . Added HBM devices to Table 9 , Table 10 , Table 19 and new High Bandwidth Memory (HBM) section. Added Cache Coherent Interconnect for Accelerators (CCIX) section.
09/27/2016	2.9	Updated Table 5 , Table 12 , Table 13 , and Table 14 .
06/03/2016	2.8	Added Zynq UltraScale+ MPSoC CG devices: Added Table 2 . Updated Table 11 , Table 12 , Table 21 , and Figure 5 . Created separate tables for EG and EV devices: Table 13 , Table 14 , Table 15 , and Table 16 . Updated Table 1 , Table 3 , Table 5 and notes, Table 6 and notes, Table 7 , Table 9 , Table 10 , Processing System Overview , and Processing System (PS) details.
02/17/2016	2.7	Added Migrating Devices . Updated Table 4 , Table 5 , Table 6 , Table 10 , Table 11 , Table 12 , and Figure 4 .
12/15/2015	2.6	Updated Table 1 , Table 5 , Table 6 , Table 9 , Table 12 , and Configuration .
11/24/2015	2.5	Updated Configuration, Encryption, and System Monitoring , Table 5 , Table 9 , Table 11 , and Table 21 .
10/15/2015	2.4	Updated Table 1 , Table 3 , Table 5 , Table 7 , Table 9 , and Table 11 with System Logic Cells. Updated Figure 3 . Updated Table 19 .
09/29/2015	2.3	Added A1156 to KU095 in Table 4 . Updated Table 5 . Updated Max. Distributed RAM in Table 9 . Updated Distributed RAM in Table 11 . Added Table 19 . Updated Table 21 . Updated Figure 3 .
08/14/2015	2.2	Updated Table 1 . Added XCKU025 to Table 3 , Table 4 , and Table 21 . Updated Table 7 , Table 9 , Table 11 , Table 12 , Table 18 . Updated System Monitor . Added voltage information to Table 21 .
04/27/2015	2.1	Updated Table 1 , Table 3 , Table 4 , Table 5 , Table 6 , Table 7 , Table 10 , Table 11 , Table 12 , Table 17 , I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken, Integrated Interface Blocks for PCI Express Designs , USB 3.0/2.0, Clock Management, System Monitor, and Figure 3 .
02/23/2015	2.0	UltraScale+ device information (Kintex UltraScale+ FPGA, Virtex UltraScale+ FPGA, and Zynq UltraScale+ MPSoC) added throughout document.
12/16/2014	1.6	Updated Table 1 ; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 3 , Table 7 ; Table 8 ; and Table 17 .
11/17/2014	1.5	Updated I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 1 ; Table 4 ; Table 7 ; Table 8 ; Table 17 ; Input/Output ; and Figure 3 .
09/16/2014	1.4	Updated Logic Cell information in Table 1 . Updated Table 3 ; I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken; Table 7 ; Table 8 ; Integrated Block for 100G Ethernet ; and Figure 3 .
05/20/2014	1.3	Updated Table 8 .
05/13/2014	1.2	Added Ordering Information . Updated Table 1 , Clocks and Memory Interfaces , Table 3 , Table 7 (removed XCVU145; added XCVU190), Table 8 (removed XCVU145; removed FLVD1924 from XCVU160; added XCVU190; updated Table Notes), Table 17 , Integrated Interface Blocks for PCI Express Designs , and Integrated Block for Interlaken , and Memory Interfaces .

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