



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Active |
| Number of LABs/CLBs | 216000 |
| Number of Logic Elements/Cells | 3780000 |
| Total RAM Bits | 514867200 |
| Number of I/O | 676 |
| Number of Gates | - |
| Voltage - Supply | 0.825V ~ 0.876V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 2104-BBGA, FCBGA |
| Supplier Device Package | 2104-FCBGA (52.5x52.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcvu13p-2figd2104e |

I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken

Data is transported on and off chip through a combination of the high-performance parallel SelectIO™ interface and high-speed serial transceiver connectivity. I/O blocks provide support for cutting-edge memory interface and network protocols through flexible I/O standard and voltage support. The serial transceivers in the UltraScale architecture-based devices transfer data up to 32.75Gb/s, enabling 25G+ backplane designs with dramatically lower power per bit than previous generation transceivers. All transceivers, except the PS-GTR, support the required data rates for PCIe Gen3, and Gen4 (rev 0.5), and integrated blocks for PCIe enable UltraScale devices to support up to Gen4 x8 and Gen3 x16 Endpoint and Root Port designs. Integrated blocks for 150Gb/s Interlaken and 100Gb/s Ethernet (100G MAC/PCS) extend the capabilities of UltraScale devices, enabling simple, reliable support for Nx100G switch and bridge applications. Virtex UltraScale+ HBM devices include Cache Coherent Interconnect for Accelerators (CCIX) ports for coherently sharing data with different processors.

Clocks and Memory Interfaces

UltraScale devices contain powerful clock management circuitry, including clock synthesis, buffering, and routing components that together provide a highly capable framework to meet design requirements. The clock network allows for extremely flexible distribution of clocks to minimize the skew, power consumption, and delay associated with clock signals. The clock management technology is tightly integrated with dedicated memory interface circuitry to enable support for high-performance external memories, including DDR4. In addition to parallel memory interfaces, UltraScale devices support serial memories, such as hybrid memory cube (HMC).

Routing, SSI, Logic, Storage, and Signal Processing

Configurable Logic Blocks (CLBs) containing 6-input look-up tables (LUTs) and flip-flops, DSP slices with 27x18 multipliers, 36Kb block RAMs with built-in FIFO and ECC support, and 4Kx72 UltraRAM blocks (in UltraScale+ devices) are all connected with an abundance of high-performance, low-latency interconnect. In addition to logical functions, the CLB provides shift register, multiplexer, and carry logic functionality as well as the ability to configure the LUTs as distributed memory to complement the highly capable and configurable block RAMs. The DSP slice, with its 96-bit-wide XOR functionality, 27-bit pre-adder, and 30-bit A input, performs numerous independent functions including multiply accumulate, multiply add, and pattern detect. In addition to the device interconnect, in devices using SSI technology, signals can cross between super-logic regions (SLRs) using dedicated, low-latency interface tiles. These combined routing resources enable easy support for next-generation bus data widths. Virtex UltraScale+ HBM devices include up to 8GB of high bandwidth memory.

Configuration, Encryption, and System Monitoring

The configuration and encryption block performs numerous device-level functions critical to the successful operation of the FPGA or MPSoC. This high-performance configuration block enables device configuration from external media through various protocols, including PCIe, often with no requirement to use multi-function I/O pins during configuration. The configuration block also provides 256-bit AES-GCM decryption capability at the same performance as unencrypted configuration. Additional features include SEU detection and correction, partial reconfiguration support, and battery-backed RAM or eFUSE technology for AES key storage to provide additional security. The System Monitor enables the monitoring of the physical environment via on-chip temperature and supply sensors and can also monitor up to 17 external analog inputs. With UltraScale+ MPSoCs, the device is booted via the Configuration and Security Unit (CSU), which supports secure boot via the 256-bit AES-GCM and SHA/384 blocks. The cryptographic engines in the CSU can be used in the MPSoC after boot for user encryption.

Migrating Devices

UltraScale and UltraScale+ families provide footprint compatibility to enable users to migrate designs from one device or family to another. Any two packages with the same footprint identifier code are footprint compatible. For example, Kintex UltraScale devices in the A1156 packages are footprint compatible with Kintex UltraScale+ devices in the A1156 packages. Likewise, Virtex UltraScale devices in the B2104 packages are compatible with Virtex UltraScale+ devices and Kintex UltraScale devices in the B2104 packages. All valid device/package combinations are provided in the Device-Package Combinations and Maximum I/Os tables in this document. Refer to [UG583](#), *UltraScale Architecture PCB Design User Guide* for more detail on migrating between UltraScale and UltraScale+ devices and packages.

Virtex UltraScale FPGA Feature Summary

Table 7: Virtex UltraScale FPGA Feature Summary

| | VU065 | VU080 | VU095 | VU125 | VU160 | VU190 | VU440 |
|--------------------------------|---------|---------|-----------|-----------|-----------|-----------|-----------|
| System Logic Cells | 783,300 | 975,000 | 1,176,000 | 1,566,600 | 2,026,500 | 2,349,900 | 5,540,850 |
| CLB Flip-Flops | 716,160 | 891,424 | 1,075,200 | 1,432,320 | 1,852,800 | 2,148,480 | 5,065,920 |
| CLB LUTs | 358,080 | 445,712 | 537,600 | 716,160 | 926,400 | 1,074,240 | 2,532,960 |
| Maximum Distributed RAM (Mb) | 4.8 | 3.9 | 4.8 | 9.7 | 12.7 | 14.5 | 28.7 |
| Block RAM Blocks | 1,260 | 1,421 | 1,728 | 2,520 | 3,276 | 3,780 | 2,520 |
| Block RAM (Mb) | 44.3 | 50.0 | 60.8 | 88.6 | 115.2 | 132.9 | 88.6 |
| CMT (1 MMCM, 2 PLLs) | 10 | 16 | 16 | 20 | 28 | 30 | 30 |
| I/O DLLs | 40 | 64 | 64 | 80 | 120 | 120 | 120 |
| Maximum HP I/Os ⁽¹⁾ | 468 | 780 | 780 | 780 | 650 | 650 | 1,404 |
| Maximum HR I/Os ⁽²⁾ | 52 | 52 | 52 | 104 | 52 | 52 | 52 |
| DSP Slices | 600 | 672 | 768 | 1,200 | 1,560 | 1,800 | 2,880 |
| System Monitor | 1 | 1 | 1 | 2 | 3 | 3 | 3 |
| PCIe Gen3 x8 | 2 | 4 | 4 | 4 | 4 | 6 | 6 |
| 150G Interlaken | 3 | 6 | 6 | 6 | 8 | 9 | 0 |
| 100G Ethernet | 3 | 4 | 4 | 6 | 9 | 9 | 3 |
| GTH 16.3Gb/s Transceivers | 20 | 32 | 32 | 40 | 52 | 60 | 48 |
| GTY 30.5Gb/s Transceivers | 20 | 32 | 32 | 40 | 52 | 60 | 0 |
| Transceiver Fractional PLLs | 10 | 16 | 16 | 20 | 26 | 30 | 0 |

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

Virtex UltraScale+ FPGA Feature Summary

Table 9: Virtex UltraScale+ FPGA Feature Summary

| | VU3P | VU5P | VU7P | VU9P | VU11P | VU13P | VU31P | VU33P | VU35P | VU37P |
|---|---------|-----------|-----------|-----------|-----------|-----------|---------|---------|-----------|-----------|
| System Logic Cells | 862,050 | 1,313,763 | 1,724,100 | 2,586,150 | 2,835,000 | 3,780,000 | 961,800 | 961,800 | 1,906,800 | 2,851,800 |
| CLB Flip-Flops | 788,160 | 1,201,154 | 1,576,320 | 2,364,480 | 2,592,000 | 3,456,000 | 879,360 | 879,360 | 1,743,360 | 2,607,360 |
| CLB LUTs | 394,080 | 600,577 | 788,160 | 1,182,240 | 1,296,000 | 1,728,000 | 439,680 | 439,680 | 871,680 | 1,303,680 |
| Max. Distributed RAM (Mb) | 12.0 | 18.3 | 24.1 | 36.1 | 36.2 | 48.3 | 12.5 | 12.5 | 24.6 | 36.7 |
| Block RAM Blocks | 720 | 1,024 | 1,440 | 2,160 | 2,016 | 2,688 | 672 | 672 | 1,344 | 2,016 |
| Block RAM (Mb) | 25.3 | 36.0 | 50.6 | 75.9 | 70.9 | 94.5 | 23.6 | 23.6 | 47.3 | 70.9 |
| UltraRAM Blocks | 320 | 470 | 640 | 960 | 960 | 1,280 | 320 | 320 | 640 | 960 |
| UltraRAM (Mb) | 90.0 | 132.2 | 180.0 | 270.0 | 270.0 | 360.0 | 90.0 | 90.0 | 180.0 | 270.0 |
| HBM DRAM (GB) | – | – | – | – | – | – | 4 | 8 | 8 | 8 |
| CMTs (1 MMCM and 2 PLLs) | 10 | 20 | 20 | 30 | 12 | 16 | 4 | 4 | 8 | 12 |
| Max. HP I/O ⁽¹⁾ | 520 | 832 | 832 | 832 | 624 | 832 | 208 | 208 | 416 | 624 |
| DSP Slices | 2,280 | 3,474 | 4,560 | 6,840 | 9,216 | 12,288 | 2,880 | 2,880 | 5,952 | 9,024 |
| System Monitor | 1 | 2 | 2 | 3 | 3 | 4 | 1 | 1 | 2 | 3 |
| GTY Transceivers 32.75Gb/s ⁽²⁾ | 40 | 80 | 80 | 120 | 96 | 128 | 32 | 32 | 64 | 96 |
| Transceiver Fractional PLLs | 20 | 40 | 40 | 60 | 48 | 64 | 16 | 16 | 32 | 48 |
| PCIe Gen3 x16 and Gen4 x8 | 2 | 4 | 4 | 6 | 3 | 4 | 4 | 4 | 5 | 6 |
| CCIX Ports ⁽³⁾ | – | – | – | – | – | – | 4 | 4 | 4 | 4 |
| 150G Interlaken | 3 | 4 | 6 | 9 | 6 | 8 | 0 | 0 | 2 | 4 |
| 100G Ethernet w/RS-FEC | 3 | 4 | 6 | 9 | 9 | 12 | 2 | 2 | 5 | 8 |

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s. See [Table 10](#).
3. A CCIX port requires the use of a PCIe Gen3 x16 / Gen4 x8 block.

Zynq UltraScale+: CG Device-Package Combinations and Maximum I/Os

Table 12: Zynq UltraScale+: CG Device-Package Combinations and Maximum I/Os

| Package (1)(2)(3)(4)(5) | Package Dimensions (mm) | ZU2CG | ZU3CG | ZU4CG | ZU5CG | ZU6CG | ZU7CG | ZU9CG |
|----------------------------|-------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| | | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY |
| SBVA484(6) | 19x19 | 24, 58 0, 0 | 24, 58 0, 0 | | | | | |
| SFVA625 | 21x21 | 24, 156 0, 0 | 24, 156 0, 0 | | | | | |
| SFVC784(7) | 23x23 | 96, 156 0, 0 | 96, 156 0, 0 | 96, 156 4, 0 | 96, 156 4, 0 | | | |
| FBVB900 | 31x31 | | | 48, 156 16, 0 | 48, 156 16, 0 | | 48, 156 16, 0 | |
| FFVC900 | 31x31 | | | | | 48, 156 16, 0 | | 48, 156 16, 0 |
| FFVB1156 | 35x35 | | | | | 120, 208 24, 0 | | 120, 208 24, 0 |
| FFVC1156 | 35x35 | | | | | | 48, 312 20, 0 | |
| FFVF1517 | 40x40 | | | | | | 48, 416 24, 0 | |

Notes:

1. Go to [Ordering Information](#) for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. All device package combinations bond out 214 PS I/O except ZU2CG and ZU3CG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
5. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
6. All 58 HP I/O pins are powered by the same V_{CCO} supply.
7. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

Zynq UltraScale+: EG Device Feature Summary

Table 13: Zynq UltraScale+: EG Device Feature Summary

| | ZU2EG | ZU3EG | ZU4EG | ZU5EG | ZU6EG | ZU7EG | ZU9EG | ZU11EG | ZU15EG | ZU17EG | ZU19EG |
|---|---|---------|---------|---------|---------|---------|---------|---------|---------|---------|-----------|
| Application Processing Unit | Quad-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache | | | | | | | | | | |
| Real-Time Processing Unit | Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM | | | | | | | | | | |
| Embedded and External Memory | 256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC | | | | | | | | | | |
| General Connectivity | 214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters | | | | | | | | | | |
| High-Speed Connectivity | 4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII | | | | | | | | | | |
| Graphic Processing Unit | ARM Mali-400 MP2; 64KB L2 Cache | | | | | | | | | | |
| System Logic Cells | 103,320 | 154,350 | 192,150 | 256,200 | 469,446 | 504,000 | 599,550 | 653,100 | 746,550 | 926,194 | 1,143,450 |
| CLB Flip-Flops | 94,464 | 141,120 | 175,680 | 234,240 | 429,208 | 460,800 | 548,160 | 597,120 | 682,560 | 846,806 | 1,045,440 |
| CLB LUTs | 47,232 | 70,560 | 87,840 | 117,120 | 214,604 | 230,400 | 274,080 | 298,560 | 341,280 | 423,403 | 522,720 |
| Distributed RAM (Mb) | 1.2 | 1.8 | 2.6 | 3.5 | 6.9 | 6.2 | 8.8 | 9.1 | 11.3 | 8.0 | 9.8 |
| Block RAM Blocks | 150 | 216 | 128 | 144 | 714 | 312 | 912 | 600 | 744 | 796 | 984 |
| Block RAM (Mb) | 5.3 | 7.6 | 4.5 | 5.1 | 25.1 | 11.0 | 32.1 | 21.1 | 26.2 | 28.0 | 34.6 |
| UltraRAM Blocks | 0 | 0 | 48 | 64 | 0 | 96 | 0 | 80 | 112 | 102 | 128 |
| UltraRAM (Mb) | 0 | 0 | 14.0 | 18.0 | 0 | 27.0 | 0 | 22.5 | 31.5 | 28.7 | 36.0 |
| DSP Slices | 240 | 360 | 728 | 1,248 | 1,973 | 1,728 | 2,520 | 2,928 | 3,528 | 1,590 | 1,968 |
| CMTs | 3 | 3 | 4 | 4 | 4 | 8 | 4 | 8 | 4 | 11 | 11 |
| Max. HP I/O ⁽¹⁾ | 156 | 156 | 156 | 156 | 208 | 416 | 208 | 416 | 208 | 572 | 572 |
| Max. HD I/O ⁽²⁾ | 96 | 96 | 96 | 96 | 120 | 48 | 120 | 96 | 120 | 96 | 96 |
| System Monitor | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| GTH Transceiver 16.3Gb/s ⁽³⁾ | 0 | 0 | 16 | 16 | 24 | 24 | 24 | 32 | 24 | 44 | 44 |
| GTY Transceivers 32.75Gb/s | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 16 | 0 | 28 | 28 |
| Transceiver Fractional PLLs | 0 | 0 | 8 | 8 | 12 | 12 | 12 | 24 | 12 | 36 | 36 |
| PCIe Gen3 x16 and Gen4 x8 | 0 | 0 | 2 | 2 | 0 | 2 | 0 | 4 | 0 | 4 | 5 |
| 150G Interlaken | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 | 4 |
| 100G Ethernet w/ RS-FEC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 0 | 2 | 4 |

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 14](#).

Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

Table 14: Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

| Package (1)(2)(3)(4)(5) | Package Dimensions (mm) | ZU2EG | ZU3EG | ZU4EG | ZU5EG | ZU6EG | ZU7EG | ZU9EG | ZU11EG | ZU15EG | ZU17EG | ZU19EG |
|----------------------------|-------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| | | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY | HD, HP GTH, GTY |
| SBVA484(6) | 19x19 | 24, 58 0, 0 | 24, 58 0, 0 | | | | | | | | | |
| SFVA625 | 21x21 | 24, 156 0, 0 | 24, 156 0, 0 | | | | | | | | | |
| SFVC784(7) | 23x23 | 96, 156 0, 0 | 96, 156 0, 0 | 96, 156 4, 0 | 96, 156 4, 0 | | | | | | | |
| FBVB900 | 31x31 | | | 48, 156 16, 0 | 48, 156 16, 0 | | 48, 156 16, 0 | | | | | |
| FFVC900 | 31x31 | | | | | 48, 156 16, 0 | | 48, 156 16, 0 | | 48, 156 16, 0 | | |
| FFVB1156 | 35x35 | | | | | 120, 208 24, 0 | | 120, 208 24, 0 | | 120, 208 24, 0 | | |
| FFVC1156 | 35x35 | | | | | | 48, 312 20, 0 | | 48, 312 20, 0 | | | |
| FFVB1517 | 40x40 | | | | | | | | 72, 416 16, 0 | | 72, 572 16, 0 | 72, 572 16, 0 |
| FFVF1517 | 40x40 | | | | | | 48, 416 24, 0 | | 48, 416 32, 0 | | | |
| FFVC1760 | 42.5x42.5 | | | | | | | | 96, 416 32, 16 | | 96, 416 32, 16 | 96, 416 32, 16 |
| FFVD1760 | 42.5x42.5 | | | | | | | | | | 48, 260 44, 28 | 48, 260 44, 28 |
| FFVE1924 | 45x45 | | | | | | | | | | 96, 572 44, 0 | 96, 572 44, 0 |

Notes:

- Go to [Ordering Information](#) for package designation details.
- FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
- All device package combinations bond out 4 PS-GTR transceivers.
- All device package combinations bond out 214 PS I/O except ZU2EG and ZU3EG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
- Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
- All 58 HP I/O pins are powered by the same V_{CCO} supply.
- GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. Figure 2 is a representation of an FPGA divided into regions.



Figure 2: Column-Based FPGA Divided into Clock Regions

Processing System (PS)

Zynq UltraScale+ MPSoCs consist of a PS coupled with programmable logic. The contents of the PS varies between the different Zynq UltraScale+ devices. All devices contain an APU, an RPU, and many peripherals for connecting the multiple processing engines to external components. The EG and EV devices contain a GPU and the EV devices contain a video codec unit (VCU). The components of the PS are connected together and to the PL through a multi-layered ARM AMBA AXI non-blocking interconnect that supports multiple simultaneous master-slave transactions. Traffic through the interconnect can be regulated by the quality of service (QoS) block in the interconnect. Twelve dedicated AXI 32-bit, 64-bit, or 128-bit ports connect the PL to high-speed interconnect and DDR in the PS via a FIFO interface.

There are four independently controllable power domains: the PL plus three within the PS (full power, lower power, and battery power domains). Additionally, many peripherals support clock gating and power gating to further reduce dynamic and static power consumption.

Application Processing Unit (APU)

The APU has a feature-rich dual-core or quad-core ARM Cortex-A53 processor. Cortex-A53 cores are 32-bit/64-bit application processors based on ARM-v8A architecture, offering the best performance-to-power ratio. The ARMv8 architecture supports hardware virtualization. Each of the Cortex-A53 cores has: 32KB of instruction and data L1 caches, with parity and ECC protection respectively; a NEON SIMD engine; and a single and double precision floating point unit. In addition to these blocks, the APU consists of a snoop control unit and a 1MB L2 cache with ECC protection to enhance system-level performance. The snoop control unit keeps the L1 caches coherent thus eliminating the need of spending software bandwidth for coherency. The APU also has a built-in interrupt controller supporting virtual interrupts. The APU communicates to the rest of the PS through 128-bit AXI coherent extension (ACE) port via Cache Coherent Interconnect (CCI) block, using the System Memory Management Unit (SMMU). The APU is also connected to the Programmable Logic (PL), through the 128-bit accelerator coherency port

General Connectivity

There are many peripherals in the PS for connecting to external devices over industry standard protocols, including CAN2.0B, USB, Ethernet, I2C, and UART. Many of the peripherals support clock gating and power gating modes to reduce dynamic and static power consumption.

USB 3.0/2.0

The pair of USB controllers can be configured as host, device, or On-The-Go (OTG). The core is compliant to USB 3.0 specification and supports super, high, full, and low speed modes in all configurations. In host mode, the USB controller is compliant with the Intel XHCI specification. In device mode, it supports up to 12 end points. While operating in USB 3.0 mode, the controller uses the serial transceiver and operates up to 5.0Gb/s. In USB 2.0 mode, the Universal Low Peripheral Interface (ULPI) is used to connect the controller to an external PHY operating up to 480Mb/s. The ULPI is also connected in USB 3.0 mode to support high-speed operations.

Ethernet MAC

The four tri-speed ethernet MACs support 10Mb/s, 100Mb/s, and 1Gb/s operations. The MACs support jumbo frames and time stamping through the interfaces based on IEEE Std 1588v2. The ethernet MACs can be connected through the serial transceivers (SGMII), the MIO (RGMII), or through EMIO (GMII). The GMII interface can be converted to a different interface within the PL.

High-Speed Connectivity

The PS includes four PS-GTR transceivers (transmit and receive), supporting data rates up to 6.0Gb/s and can interface to the peripherals for communication over PCIe, SATA, USB 3.0, SGMII, and DisplayPort.

PCIe

The integrated block for PCIe is compliant with PCI Express base specification 2.1 and supports x1, x2, and x4 configurations as root complex or end point, compliant to transaction ordering rules in both configurations. It has built-in DMA, supports one virtual channel and provides fully configurable base address registers.

SATA

Users can connect up to two external devices using the two SATA host port interfaces compliant to the SATA 3.1 specification. The SATA interfaces can operate at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates and are compliant with advanced host controller interface (AHCI) version 1.3 supporting partial and slumber power modes.

DisplayPort

The DisplayPort controller supports up to two lanes of source-only DisplayPort compliant with VESA DisplayPort v1.2a specification (source only) at 1.62Gb/s, 2.7Gb/s, and 5.4Gb/s data rates. The controller supports single stream transport (SST); video resolution up to 4Kx2K at a 30Hz frame rate; video formats Y-only, YCbCr444, YCbCr422, YCbCr420, RGB, YUV444, YUV422, xvYCC, and pixel color depth of 6, 8, 10, and 12 bits per color component.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100 Ω internal resistor. All UltraScale devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. UltraScale+ families add support for MIPI with a dedicated D-PHY in the I/O bank.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

High-Speed Serial Transceivers

Serial data transmission between devices on the same PCB, over backplanes, and across even longer distances is becoming increasingly important for scaling to 100Gb/s and 400Gb/s line cards. Specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues are required at these high data rates.

Three types of transceivers are used in the UltraScale architecture: GTH and GTY in FPGAs and MPSoC PL, and PS-GTR in the MPSoC PS. All transceivers are arranged in groups of four, known as a transceiver Quad. Each serial transceiver is a combined transmitter and receiver. [Table 17](#) compares the available transceivers.

Table 17: Transceiver Information

| | Kintex UltraScale | | Kintex UltraScale+ | | Virtex UltraScale | | Virtex UltraScale+ | Zynq UltraScale+ | | |
|----------------|---|---|---|---|---|---|---|--|---|---|
| Type | GTH | GTY | GTH | GTY | GTH | GTY | GTY | PS-GTR | GTH | GTY |
| Qty | 16–64 | 0–32 | 20–60 | 0–60 | 20–60 | 0–60 | 40–128 | 4 | 0–44 | 0–28 |
| Max. Data Rate | 16.3Gb/s | 16.3Gb/s | 16.3Gb/s | 32.75Gb/s | 16.3Gb/s | 30.5Gb/s | 32.75Gb/s | 6.0Gb/s | 16.3Gb/s | 32.75Gb/s |
| Min. Data Rate | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 0.5Gb/s | 1.25Gb/s | 0.5Gb/s | 0.5Gb/s |
| Key Apps | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC | <ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC | <ul style="list-style-type: none"> PCIe Gen2 USB Ethernet | <ul style="list-style-type: none"> Backplane PCIe Gen4 HMC | <ul style="list-style-type: none"> 100G+ Optics Chip-to-Chip 25G+ Backplane HMC |

The following information in this section pertains to the GTH and GTY only.

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally “auto-adapt” to automatically learn and compensate for different interconnect characteristics. This enables even more margin for 10G+ and 25G+ backplanes.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

Cache Coherent Interconnect for Accelerators (CCIX)

CCIX is a chip-to-chip interconnect operating at data rates up to 25Gb/s that allows two or more devices to share memory in a cache coherent manner. Using PCIe for the transport layer, CCIX can operate at several standard data rates (2.5, 5, 8, and 16Gb/s) with an additional high-speed 25Gb/s option. The specification employs a subset of full coherency protocols and ensures that FPGAs used as accelerators can coherently share data with processors using different instruction set architectures.

Virtex UltraScale+ HBM devices support CCIX data rates up to 16Gb/s and contain four CCIX ports and at least four integrated blocks for PCIe. Each CCIX port requires the use of one integrated block for PCIe. If not used with a CCIX port, the integrated blocks for PCIe can still be used for PCIe communication.

Integrated Block for Interlaken

Some UltraScale architecture-based devices include integrated blocks for Interlaken. Interlaken is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gb/s to 150Gb/s. The Interlaken integrated block in the UltraScale architecture is compliant to revision 1.2 of the Interlaken specification with data striping and de-striping across 1 to 12 lanes. Permitted configurations are: 1 to 12 lanes at up to 12.5Gb/s and 1 to 6 lanes at up to 25.78125Gb/s, enabling flexible support for up to 150Gb/s per integrated block. With multiple Interlaken blocks, certain UltraScale devices enable easy, reliable Interlaken switches and bridges.

Integrated Block for 100G Ethernet

Compliant to the IEEE Std 802.3ba, the 100G Ethernet integrated blocks in the UltraScale architecture provide low latency 100Gb/s Ethernet ports with a wide range of user customization and statistics gathering. With support for 10 x 10.3125Gb/s (CAUI) and 4 x 25.78125Gb/s (CAUI-4) configurations, the integrated block includes both the 100G MAC and PCS logic with support for IEEE Std 1588v2 1-step and 2-step hardware timestamping.

In UltraScale+ devices, the 100G Ethernet blocks contain a Reed Solomon Forward Error Correction (RS-FEC) block, compliant to IEEE Std 802.3bj, that can be used with the Ethernet block or stand alone in user applications. These families also support OTN mapping mode in which the PCS can be operated without using the MAC.

Block RAM

Every UltraScale architecture-based device contains a number of 36 Kb block RAMs, each with two completely independent ports that share only the stored data. Each block RAM can be configured as one 36Kb RAM or two independent 18Kb RAMs. Each memory access, read or write, is controlled by the clock. Connections in every block RAM column enable signals to be cascaded between vertically adjacent block RAMs, providing an easy method to create large, fast memory arrays, and FIFOs with greatly reduced power consumption.

All inputs, data, address, clock enables, and write enables are registered. The input address is always clocked (unless address latching is turned off), retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency. During a write operation, the data output can reflect either the previously stored data or the newly written data, or it can remain unchanged. Block RAM sites that remain unused in the user design are automatically powered down to reduce total power consumption. There is an additional pin on every block RAM to control the dynamic power gating feature.

Programmable Data Width

Each port can be configured as $32K \times 1$; $16K \times 2$; $8K \times 4$; $4K \times 9$ (or 8); $2K \times 18$ (or 16); $1K \times 36$ (or 32); or 512×72 (or 64). Whether configured as block RAM or FIFO, the two ports can have different aspect ratios without any constraints. Each block RAM can be divided into two completely independent 18Kb block RAMs that can each be configured to any aspect ratio from $16K \times 1$ to 512×36 . Everything described previously for the full 36Kb block RAM also applies to each of the smaller 18Kb block RAMs. Only in simple dual-port (SDP) mode can data widths of greater than 18bits (18Kb RAM) or 36 bits (36Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72. Both sides of the dual-port 36Kb RAM can be of variable width.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

Each block RAM can be configured as a 36Kb FIFO or an 18Kb FIFO. The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, programmable full, and programmable empty. The programmable flags allow the user to specify the FIFO counter values that make these flags go active. The FIFO width and depth are programmable with support for different read port and write port widths on a single FIFO. A dedicated cascade path allows for easy creation of deeper FIFOs.

Interconnect

Various length vertical and horizontal routing resources in the UltraScale architecture that span 1, 2, 4, 5, 12, or 16 CLBs ensure that all signals can be transported from source to destination with ease, providing support for the next generation of wide data buses to be routed across even the highest capacity devices while simultaneously improving quality of results and software run time.

Digital Signal Processing

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All UltraScale devices have many dedicated, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 27×18 bit twos complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The 96-bit-wide XOR function, programmable to 12, 24, 48, or 96-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP also includes a 48-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

System Monitor

The System Monitor blocks in the UltraScale architecture are used to enhance the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors and external channels to the ADC.

All UltraScale architecture-based devices contain at least one System Monitor. The System Monitor in UltraScale+ FPGAs and the PL of Zynq UltraScale+ MPSoCs is similar to the Kintex UltraScale and Virtex UltraScale devices but with additional features including a PMBus interface.

After copying the FSBL to OCM, the processor executes the FSBL. Xilinx supplies example FSBLs or users can create their own. The FSBL initiates the boot of the PS and can load and configure the PL, or configuration of the PL can be deferred to a later stage. The FSBL typically loads either a user application or an optional second stage boot loader (SSBL) such as U-Boot. Users obtain example SSBL from Xilinx or a third party, or they can create their own SSBL. The SSBL continues the boot process by loading code from any of the primary boot devices or from other sources such as USB, Ethernet, etc. If the FSBL did not configure the PL, the SSBL can do so, or again, the configuration can be deferred to a later stage.

The static memory interface controller (NAND, eMMC, or Quad-SPI) is configured using default settings. To improve device configuration speed, these settings can be modified by information provided in the boot image header. The ROM boot image is not user readable or executable after boot.

Configuring FPGAs

The SPI (serial NOR) interface (x1, x2, x4, and dual x4 modes) and the BPI (parallel NOR) interface (x8 and x16 modes) are two common methods used for configuring the FPGA. Users can directly connect an SPI or BPI flash to the FPGA, and the FPGA's internal configuration logic reads the bitstream out of the flash and configures itself, eliminating the need for an external controller. The FPGA automatically detects the bus width on the fly, eliminating the need for any external controls or switches. Bus widths supported are x1, x2, x4, and dual x4 for SPI, and x8 and x16 for BPI. The larger bus widths increase configuration speed and reduce the amount of time it takes for the FPGA to start up after power-on.

In master mode, the FPGA can drive the configuration clock from an internally generated clock, or for higher speed configuration, the FPGA can use an external configuration clock source. This allows high-speed configuration with the ease of use characteristic of master mode. Slave modes up to 32 bits wide that are especially useful for processor-driven configuration are also supported by the FPGA. In addition, the new media configuration access port (MCAP) provides a direct connection between the integrated block for PCIe and the configuration logic to simplify configuration over PCIe.

SEU detection and mitigation (SEM) IP, RSA authentication, post-configuration CRC, and Security Monitor (SecMon) IP are not supported in the KU025 FPGA.

Packaging

The UltraScale devices are available in a variety of organic flip-chip and lidless flip-chip packages supporting different quantities of I/Os and transceivers. Maximum supported performance can depend on the style of package and its material. Always refer to the specific device data sheet for performance specifications by package type.

In flip-chip packages, the silicon device is attached to the package substrate using a high-performance flip-chip process. Decoupling capacitors are mounted on the package substrate to optimize signal integrity under simultaneous switching of outputs (SSO) conditions.

Ordering Information

Table 21 shows the speed and temperature grades available in the different device families. V_{CCINT} supply voltage is listed in parentheses.

Table 21: Speed Grade and Temperature Grade

| Device Family | Devices | Speed Grade and Temperature Grade | | | |
|--------------------|--|-----------------------------------|---------------------------|--------------------------------------|--------------------------------------|
| | | Commercial (C) | Extended (E) | | Industrial (I) |
| | | 0°C to +85°C | 0°C to +100°C | 0°C to +110°C | –40°C to +100°C |
| Kintex UltraScale | All | | -3E ⁽¹⁾ (1.0V) | | |
| | | | -2E (0.95V) | | -2I (0.95V) |
| | | -1C (0.95V) | | | -1I (0.95V) |
| | | | | | -1LI ⁽¹⁾ (0.95V or 0.90V) |
| Kintex UltraScale+ | All | | -3E (0.90V) | | |
| | | | -2E (0.85V) | | -2I (0.85V) |
| | | | | -2LE ⁽²⁾ (0.85V or 0.72V) | |
| | | | -1E (0.85V) | | -1I (0.85V) |
| | | | | | -1LI (0.85V or 0.72V) |
| Virtex UltraScale | VU065 VU080 VU095 VU125 VU160 VU190 | | -3E (1.0V) | | |
| | | | -2E (0.95V) | | -2I (0.95V) |
| | | | -1HE (0.95V or 1.0V) | | -1I (0.95V) |
| | | | | | |
| | VU440 | | -3E (1.0V) | | |
| | | | -2E (0.95V) | | -2I (0.95V) |
| | | -1C (0.95V) | | | -1I (0.95V) |
| Virtex UltraScale+ | VU3P VU5P VU7P VU9P VU11P VU13P | | -3E (0.90V) | | |
| | | | -2E (0.85V) | | -2I (0.85V) |
| | | | | -2LE ⁽²⁾ (0.85V or 0.72V) | |
| | | | -1E (0.85V) | | -1I (0.85V) |
| | | | | | |
| | | | | | |
| | VU31P VU33P VU35P VU37P | | -3E (0.90V) | | |
| | | | -2E (0.85V) | | |
| | | | | -2LE ⁽²⁾ (0.85V or 0.72V) | |
| | | | -1E (0.85V) | | |

The ordering information shown in [Figure 3](#) applies to all packages in the Kintex UltraScale and Virtex UltraScale FPGAs. Refer to the Package Marking section of [UG575, UltraScale and UltraScale+ FPGAs Packaging and Pinouts User Guide](#) for a more detailed explanation of the device markings.



Figure 3: Kintex UltraScale and Virtex UltraScale FPGA Ordering Information

| Date | Version | Description of Revisions |
|------------|---------|---|
| 02/06/2014 | 1.1 | Updated PCIe information in Table 1 and Table 3 . Added FFVJ1924 package to Table 8 . |
| 12/10/2013 | 1.0 | Initial Xilinx release. |

Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at <http://www.xilinx.com/legal.htm#tos>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at <http://www.xilinx.com/legal.htm#tos>.

This document contains preliminary information and is subject to change without notice. Information provided herein relates to products and/or services not yet available for sale, and provided solely for information purposes and are not intended, or to be construed, as an offer for sale or an attempted commercialization of the products and/or services referred to herein.

Automotive Applications Disclaimer

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.