# AMD Xilinx - XCVU9P-1FLGB2104I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 147780 |
| Number of Logic Elements/Cells | 2586150 |
| Total RAM Bits | 391168000 |
| Number of I/O | 702 |
| Number of Gates | - |
| Voltage - Supply | 0.825V ~ 0.876V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 2104-BBGA, FCBGA |
| Supplier Device Package | 2104-FCBGA (47.5x47.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcvu9p-1flgb2104i |

# Kintex UltraScale FPGA Feature Summary

*Table 3:* **Kintex UltraScale FPGA Feature Summary**

| | KU025[(1)] | KU035 | KU040 | KU060 | KU085 | KU095 | KU115 |
|---|---|---|---|---|---|---|---|
| System Logic Cells | 318,150 | 444,343 | 530,250 | 725,550 | 1,088,325 | 1,176,000 | 1,451,100 |
| CLB Flip-Flops | 290,880 | 406,256 | 484,800 | 663,360 | 995,040 | 1,075,200 | 1,326,720 |
| CLB LUTs | 145,440 | 203,128 | 242,400 | 331,680 | 497,520 | 537,600 | 663,360 |
| Maximum Distributed RAM (Mb) | 4.1 | 5.9 | 7.0 | 9.1 | 13.4 | 4.7 | 18.3 |
| Block RAM Blocks | 360 | 540 | 600 | 1,080 | 1,620 | 1,680 | 2,160 |
| Block RAM (Mb) | 12.7 | 19.0 | 21.1 | 38.0 | 56.9 | 59.1 | 75.9 |
| CMTs (1 MMCM, 2 PLLs) | 6 | 10 | 10 | 12 | 22 | 16 | 24 |
| I/O DLLs | 24 | 40 | 40 | 48 | 56 | 64 | 64 |
| Maximum HP I/Os[(2)] | 208 | 416 | 416 | 520 | 572 | 650 | 676 |
| Maximum HR I/Os[(3)] | 104 | 104 | 104 | 104 | 104 | 52 | 156 |
| DSP Slices | 1,152 | 1,700 | 1,920 | 2,760 | 4,100 | 768 | 5,520 |
| System Monitor | 1 | 1 | 1 | 1 | 2 | 1 | 2 |
| PCIe Gen3 x8 | 1 | 2 | 3 | 3 | 4 | 4 | 6 |
| 150G Interlaken | 0 | 0 | 0 | 0 | 0 | 2 | 0 |
| 100G Ethernet | 0 | 0 | 0 | 0 | 0 | 2 | 0 |
| GTH 16.3Gb/s Transceivers[(4)] | 12 | 16 | 20 | 32 | 56 | 32 | 64 |
| GTY 16.3Gb/s Transceivers[(5)] | 0 | 0 | 0 | 0 | 0 | 32 | 0 |
| Transceiver Fractional PLLs | 0 | 0 | 0 | 0 | 0 | 16 | 0 |

**Notes:**

1. Certain advanced configuration features are not supported in the KU025. Refer to the Configuring FPGAs section for details.
2. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
3. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
4. GTH transceivers in SF/FB packages support data rates up to 12.5Gb/s. See Table 4.
5. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s. See Table 4.

# Kintex UltraScale Device-Package Combinations and Maximum I/Os

*Table 4:* **Kintex UltraScale Device-Package Combinations and Maximum I/Os**

| Package (1)(2)(3) | Package Dimensions (mm) | KU025 | KU035 | KU040 | KU060 | KU085 | KU095 | KU115 |
|---|---|---|---|---|---|---|---|---|
| | | HR, HP<br>GTH | HR, HP<br>GTH | HR, HP<br>GTH | HR, HP<br>GTH | HR, HP<br>GTH | HR, HP<br>GTH, GTY(4) | HR, HP<br>GTH |
| SFVA784(5) | 23x23 | | 104, 364<br>8 | 104, 364<br>8 | | | | |
| FBVA676(5) | 27x27 | | 104, 208<br>16 | 104, 208<br>16 | | | | |
| FBVA900(5) | 31x31 | | 104, 364<br>16 | 104, 364<br>16 | | | | |
| FFVA1156 | 35x35 | 104, 208<br>12 | 104, 416<br>16 | 104, 416<br>20 | 104, 416<br>28 | | 52, 468<br>20, 8 | |
| FFVA1517 | 40x40 | | | | 104, 520<br>32 | | | |
| FLVA1517 | 40x40 | | | | | 104, 520<br>48 | | 104, 520<br>48 |
| FFVC1517 | 40x40 | | | | | | 52, 468<br>20, 20 | |
| FLVD1517 | 40x40 | | | | | | | 104, 234<br>64 |
| FFVB1760 | 42.5x42.5 | | | | | | 52, 650<br>32, 16 | |
| FLVB1760 | 42.5x42.5 | | | | | 104, 572<br>44 | | 104, 598<br>52 |
| FLVD1924 | 45x45 | | | | | | | 156, 676<br>52 |
| FLVF1924 | 45x45 | | | | | 104, 520<br>56 | | 104, 624<br>64 |
| FLVA2104 | 47.5x47.5 | | | | | | | 156, 676<br>52 |
| FFVB2104 | 47.5x47.5 | | | | | | 52, 650<br>32, 32 | |
| FLVB2104 | 47.5x47.5 | | | | | | | 104, 598<br>64 |

**Notes:**

1. Go to Ordering Information for package designation details.
2. FB/FF/FL packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the UltraScale Architecture Product Selection Guide for details on inter-family migration.
4. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s.
5. GTH transceivers in SF/FB packages support data rates up to 12.5Gb/s.

# Kintex UltraScale+ FPGA Feature Summary

*Table 5:* **Kintex UltraScale+ FPGA Feature Summary**

| | KU3P | KU5P | KU9P | KU11P | KU13P | KU15P |
|---|---|---|---|---|---|---|
| System Logic Cells | 355,950 | 474,600 | 599,550 | 653,100 | 746,550 | 1,143,450 |
| CLB Flip-Flops | 325,440 | 433,920 | 548,160 | 597,120 | 682,560 | 1,045,440 |
| CLB LUTs | 162,720 | 216,960 | 274,080 | 298,560 | 341,280 | 522,720 |
| Max. Distributed RAM (Mb) | 4.7 | 6.1 | 8.8 | 9.1 | 11.3 | 9.8 |
| Block RAM Blocks | 360 | 480 | 912 | 600 | 744 | 984 |
| Block RAM (Mb) | 12.7 | 16.9 | 32.1 | 21.1 | 26.2 | 34.6 |
| UltraRAM Blocks | 48 | 64 | 0 | 80 | 112 | 128 |
| UltraRAM (Mb) | 13.5 | 18.0 | 0 | 22.5 | 31.5 | 36.0 |
| CMTs (1 MMCM and 2 PLLs) | 4 | 4 | 4 | 8 | 4 | 11 |
| Max. HP I/O[(1)] | 208 | 208 | 208 | 416 | 208 | 572 |
| Max. HD I/O[(2)] | 96 | 96 | 96 | 96 | 96 | 96 |
| DSP Slices | 1,368 | 1,824 | 2,520 | 2,928 | 3,528 | 1,968 |
| System Monitor | 1 | 1 | 1 | 1 | 1 | 1 |
| GTH Transceiver 16.3Gb/s | 0 | 0 | 28 | 32 | 28 | 44 |
| GTY Transceivers 32.75Gb/s[(3)] | 16 | 16 | 0 | 20 | 0 | 32 |
| Transceiver Fractional PLLs | 8 | 8 | 14 | 26 | 14 | 38 |
| PCIe Gen3 x16 and Gen4 x8 | 1 | 1 | 0 | 4 | 0 | 5 |
| 150G Interlaken | 0 | 0 | 0 | 1 | 0 | 4 |
| 100G Ethernet w/RS-FEC | 0 | 1 | 0 | 2 | 0 | 4 |

**Notes:**

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTY transceiver line rates are package limited: SFVB784 to 12.5Gb/s; FFVA676, FFVD900, and FFVA1156 to 16.3Gb/s. See Table 6.

# Virtex UltraScale FPGA Feature Summary

*Table 7:* **Virtex UltraScale FPGA Feature Summary**

| | VU065 | VU080 | VU095 | VU125 | VU160 | VU190 | VU440 |
|---|---|---|---|---|---|---|---|
| System Logic Cells | 783,300 | 975,000 | 1,176,000 | 1,566,600 | 2,026,500 | 2,349,900 | 5,540,850 |
| CLB Flip-Flops | 716,160 | 891,424 | 1,075,200 | 1,432,320 | 1,852,800 | 2,148,480 | 5,065,920 |
| CLB LUTs | 358,080 | 445,712 | 537,600 | 716,160 | 926,400 | 1,074,240 | 2,532,960 |
| Maximum Distributed RAM (Mb) | 4.8 | 3.9 | 4.8 | 9.7 | 12.7 | 14.5 | 28.7 |
| Block RAM Blocks | 1,260 | 1,421 | 1,728 | 2,520 | 3,276 | 3,780 | 2,520 |
| Block RAM (Mb) | 44.3 | 50.0 | 60.8 | 88.6 | 115.2 | 132.9 | 88.6 |
| CMT (1 MMCM, 2 PLLs) | 10 | 16 | 16 | 20 | 28 | 30 | 30 |
| I/O DLLs | 40 | 64 | 64 | 80 | 120 | 120 | 120 |
| Maximum HP I/Os[(1)] | 468 | 780 | 780 | 780 | 650 | 650 | 1,404 |
| Maximum HR I/Os[(2)] | 52 | 52 | 52 | 104 | 52 | 52 | 52 |
| DSP Slices | 600 | 672 | 768 | 1,200 | 1,560 | 1,800 | 2,880 |
| System Monitor | 1 | 1 | 1 | 2 | 3 | 3 | 3 |
| PCIe Gen3 x8 | 2 | 4 | 4 | 4 | 4 | 6 | 6 |
| 150G Interlaken | 3 | 6 | 6 | 6 | 8 | 9 | 0 |
| 100G Ethernet | 3 | 4 | 4 | 6 | 9 | 9 | 3 |
| GTH 16.3Gb/s Transceivers | 20 | 32 | 32 | 40 | 52 | 60 | 48 |
| GTY 30.5Gb/s Transceivers | 20 | 32 | 32 | 40 | 52 | 60 | 0 |
| Transceiver Fractional PLLs | 10 | 16 | 16 | 20 | 26 | 30 | 0 |

**Notes:**
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

# Virtex UltraScale Device-Package Combinations and Maximum I/Os

*Table 8:* **Virtex UltraScale Device-Package Combinations and Maximum I/Os**

| Package[(1)(2)(3)] | Package Dimensions (mm) | VU065 | VU080 | VU095 | VU125 | VU160 | VU190 | VU440 |
|---|---|---|---|---|---|---|---|---|
| | | HR, HP<br>GTH, GTY | HR, HP<br>GTH, GTY | HR, HP<br>GTH, GTY | HR, HP<br>GTH, GTY | HR, HP<br>GTH, GTY | HR, HP<br>GTH, GTY | HR, HP<br>GTH, GTY |
| FFVC1517 | 40x40 | 52, 468<br>20, 20 | 52, 468<br>20, 20 | 52, 468<br>20, 20 | | | | |
| FFVD1517 | 40x40 | | 52, 286<br>32, 32 | 52, 286<br>32, 32 | | | | |
| FLVD1517 | 40x40 | | | | 52, 286<br>40, 32 | | | |
| FFVB1760 | 42.5x42.5 | | 52, 650<br>32, 16 | 52, 650<br>32, 16 | | | | |
| FLVB1760 | 42.5x42.5 | | | | 52, 650<br>36, 16 | | | |
| FFVA2104 | 47.5x47.5 | | 52, 780<br>28, 24 | 52, 780<br>28, 24 | | | | |
| FLVA2104 | 47.5x47.5 | | | | 52, 780<br>28, 24 | | | |
| FFVB2104 | 47.5x47.5 | | 52, 650<br>32, 32 | 52, 650<br>32, 32 | | | | |
| FLVB2104 | 47.5x47.5 | | | | 52, 650<br>40, 36 | | | |
| FLGB2104 | 47.5x47.5 | | | | | 52, 650<br>40, 36 | 52, 650<br>40, 36 | |
| FFVC2104 | 47.5x47.5 | | | 52, 364<br>32, 32 | | | | |
| FLVC2104 | 47.5x47.5 | | | | 52, 364<br>40, 40 | | | |
| FLGC2104 | 47.5x47.5 | | | | | 52, 364<br>52, 52 | 52, 364<br>52, 52 | |
| FLGB2377 | 50x50 | | | | | | | 52, 1248<br>36, 0 |
| FLGA2577 | 52.5x52.5 | | | | | | 0, 448<br>60, 60 | |
| FLGA2892 | 55x55 | | | | | | | 52, 1404<br>48, 0 |

**Notes:**

1. Go to Ordering Information for package designation details.
2. All packages have 1.0mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the UltraScale Architecture Product Selection Guide for details on inter-family migration.

# Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

*Table 10:* **Virtex UltraScale+ Device-Package Combinations and Maximum I/Os**

| Package (1)(2)(3) | Package Dimensions (mm) | VU3P | VU5P | VU7P | VU9P | VU11P | VU13P | VU31P | VU33P | VU35P | VU37P |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY | HP, GTY |
| FFVC1517 | 40x40 | 520, 40 | | | | | | | | | |
| FLGF1924(4) | 45x45 | | | | | 624, 64 | | | | | |
| FLVA2104 | 47.5x47.5 | | 832, 52 | 832, 52 | | | | | | | |
| FLGA2104 | 47.5x47.5 | | | | 832, 52 | | | | | | |
| FHGA2104 | 52.5x52.5(5) | | | | | | 832, 52 | | | | |
| FLVB2104 | 47.5x47.5 | | 702, 76 | 702, 76 | | | | | | | |
| FLGB2104 | 47.5x47.5 | | | | 702, 76 | 572, 76 | | | | | |
| FHGB2104 | 52.5x52.5(5) | | | | | | 702, 76 | | | | |
| FLVC2104 | 47.5x47.5 | | 416, 80 | 416, 80 | | | | | | | |
| FLGC2104 | 47.5x47.5 | | | | 416, 104 | 416, 96 | | | | | |
| FHGC2104 | 52.5x52.5(5) | | | | | | 416, 104 | | | | |
| FSGD2104 | 47.5x47.5 | | | | 676, 76 | 572, 76 | | | | | |
| FIGD2104 | 52.5x52.5(5) | | | | | | 676, 76 | | | | |
| FLGA2577 | 52.5x52.5 | | | | 448, 120 | 448, 96 | 448, 128 | | | | |
| FSVH1924 | 45x45 | | | | | | | 208, 32 | | | |
| FSVH2104 | 47.5x47.5 | | | | | | | | 208, 32 | 416, 64 | |
| FSVH2892 | 55x55 | | | | | | | | | 416, 64 | 624, 96 |

**Notes:**
1. Go to Ordering Information for package designation details.
2. All packages have 1.0mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the UltraScale Architecture Product Selection Guide for details on inter-family migration.
4. GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s.
5. These 52.5x52.5mm overhang packages have the same PCB ball footprint as the corresponding 47.5x47.5mm packages (i.e., the same last letter and number sequence) and are footprint compatible.

# Zynq UltraScale+: EG Device Feature Summary

*Table 13:* **Zynq UltraScale+: EG Device Feature Summary**

| | ZU2EG | ZU3EG | ZU4EG | ZU5EG | ZU6EG | ZU7EG | ZU9EG | ZU11EG | ZU15EG | ZU17EG | ZU19EG |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Application Processing Unit | Quad-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache | | | | | | | | | | |
| Real-Time Processing Unit | Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM | | | | | | | | | | |
| Embedded and External Memory | 256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC | | | | | | | | | | |
| General Connectivity | 214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters | | | | | | | | | | |
| High-Speed Connectivity | 4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII | | | | | | | | | | |
| Graphic Processing Unit | ARM Mali-400 MP2; 64KB L2 Cache | | | | | | | | | | |
| System Logic Cells | 103,320 | 154,350 | 192,150 | 256,200 | 469,446 | 504,000 | 599,550 | 653,100 | 746,550 | 926,194 | 1,143,450 |
| CLB Flip-Flops | 94,464 | 141,120 | 175,680 | 234,240 | 429,208 | 460,800 | 548,160 | 597,120 | 682,560 | 846,806 | 1,045,440 |
| CLB LUTs | 47,232 | 70,560 | 87,840 | 117,120 | 214,604 | 230,400 | 274,080 | 298,560 | 341,280 | 423,403 | 522,720 |
| Distributed RAM (Mb) | 1.2 | 1.8 | 2.6 | 3.5 | 6.9 | 6.2 | 8.8 | 9.1 | 11.3 | 8.0 | 9.8 |
| Block RAM Blocks | 150 | 216 | 128 | 144 | 714 | 312 | 912 | 600 | 744 | 796 | 984 |
| Block RAM (Mb) | 5.3 | 7.6 | 4.5 | 5.1 | 25.1 | 11.0 | 32.1 | 21.1 | 26.2 | 28.0 | 34.6 |
| UltraRAM Blocks | 0 | 0 | 48 | 64 | 0 | 96 | 0 | 80 | 112 | 102 | 128 |
| UltraRAM (Mb) | 0 | 0 | 14.0 | 18.0 | 0 | 27.0 | 0 | 22.5 | 31.5 | 28.7 | 36.0 |
| DSP Slices | 240 | 360 | 728 | 1,248 | 1,973 | 1,728 | 2,520 | 2,928 | 3,528 | 1,590 | 1,968 |
| CMTs | 3 | 3 | 4 | 4 | 4 | 8 | 4 | 8 | 4 | 11 | 11 |
| Max. HP I/O[1] | 156 | 156 | 156 | 156 | 208 | 416 | 208 | 416 | 208 | 572 | 572 |
| Max. HD I/O[2] | 96 | 96 | 96 | 96 | 120 | 48 | 120 | 96 | 120 | 96 | 96 |
| System Monitor | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| GTH Transceiver 16.3Gb/s[3] | 0 | 0 | 16 | 16 | 24 | 24 | 24 | 32 | 24 | 44 | 44 |
| GTY Transceivers 32.75Gb/s | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 16 | 0 | 28 | 28 |
| Transceiver Fractional PLLs | 0 | 0 | 8 | 8 | 12 | 12 | 12 | 24 | 12 | 36 | 36 |
| PCIe Gen3 x16 and Gen4 x8 | 0 | 0 | 2 | 2 | 0 | 2 | 0 | 4 | 0 | 4 | 5 |
| 150G Interlaken | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 | 4 |
| 100G Ethernet w/ RS-FEC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 0 | 2 | 4 |

**Notes:**

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See Table 14.

# Zynq UltraScale+: EG Device Feature Summary

*Table 15:* **Zynq UltraScale+: EV Device Feature Summary**

| | ZU4EV | ZU5EV | ZU7EV |
|---|---|---|---|
| Application Processing Unit | Quad-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache | | |
| Real-Time Processing Unit | Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM | | |
| Embedded and External Memory | 256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC | | |
| General Connectivity | 214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters | | |
| High-Speed Connectivity | 4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII | | |
| Graphic Processing Unit | ARM Mali-400 MP2; 64KB L2 Cache | | |
| Video Codec | 1 | 1 | 1 |
| System Logic Cells | 192,150 | 256,200 | 504,000 |
| CLB Flip-Flops | 175,680 | 234,240 | 460,800 |
| CLB LUTs | 87,840 | 117,120 | 230,400 |
| Distributed RAM (Mb) | 2.6 | 3.5 | 6.2 |
| Block RAM Blocks | 128 | 144 | 312 |
| Block RAM (Mb) | 4.5 | 5.1 | 11.0 |
| UltraRAM Blocks | 48 | 64 | 96 |
| UltraRAM (Mb) | 14.0 | 18.0 | 27.0 |
| DSP Slices | 728 | 1,248 | 1,728 |
| CMTs | 4 | 4 | 8 |
| Max. HP I/O(1) | 156 | 156 | 416 |
| Max. HD I/O(2) | 96 | 96 | 48 |
| System Monitor | 2 | 2 | 2 |
| GTH Transceiver 16.3Gb/s(3) | 16 | 16 | 24 |
| GTY Transceivers 32.75Gb/s | 0 | 0 | 0 |
| Transceiver Fractional PLLs | 8 | 8 | 12 |
| PCIe Gen3 x16 and Gen4 x8 | 2 | 2 | 2 |
| 150G Interlaken | 0 | 0 | 0 |
| 100G Ethernet w/ RS-FEC | 0 | 0 | 0 |

**Notes:**
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See Table 16.

## Zynq UltraScale+: EG Device-Package Combinations and Maximum I/Os

*Table 16:* **Zynq UltraScale+: EV Device-Package Combinations and Maximum I/Os**

| Package (1)(2)(3)(4) | Package Dimensions (mm) | ZU4EV | ZU5EV | ZU7EV |
|---|---|---|---|---|
| | | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY |
| SFVC784(5) | 23x23 | 96, 156<br>4, 0 | 96, 156<br>4, 0 | |
| FBVB900 | 31x31 | 48, 156<br>16, 0 | 48, 156<br>16, 0 | 48, 156<br>16, 0 |
| FFVC1156 | 35x35 | | | 48, 312<br>20, 0 |
| FFVF1517 | 40x40 | | | 48, 416<br>24, 0 |

**Notes:**

1. Go to Ordering Information for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.
5. Packages with the same last letter and number sequence, e.g., B900, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.

# Device Layout

UltraScale devices are arranged in a column-and-grid layout. Columns of resources are combined in different ratios to provide the optimum capability for the device density, target market or application, and device cost. At the core of UltraScale+ MPSoCs is the processing system that displaces some of the full or partial columns of programmable logic resources. Figure 1 shows a device-level view with resources grouped together. For simplicity, certain resources such as the processing system, integrated blocks for PCIe, configuration logic, and System Monitor are not shown.

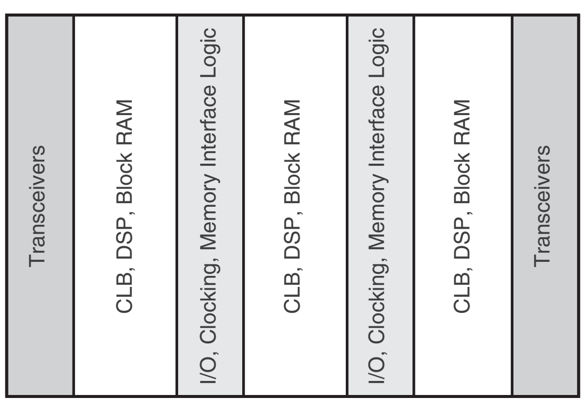


*Figure 1:* **FPGA with Columnar Resources**

Resources within the device are divided into segmented clock regions. The height of a clock region is 60 CLBs. A bank of 52 I/Os, 24 DSP slices, 12 block RAMs, or 4 transceiver channels also matches the height of a clock region. The width of a clock region is essentially the same in all cases, regardless of device size or the mix of resources in the region, enabling repeatable timing results. Each segmented clock region contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. Figure 2 is a representation of an FPGA divided into regions.

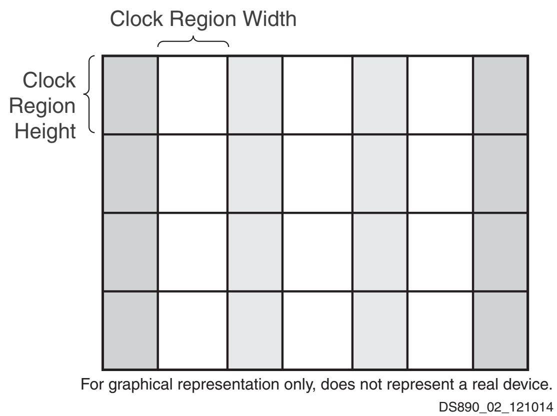


*Figure 2:* **Column-Based FPGA Divided into Clock Regions**

# Processing System (PS)

Zynq UltraScale+ MPSoCs consist of a PS coupled with programmable logic. The contents of the PS varies between the different Zynq UltraScale+ devices. All devices contain an APU, an RPU, and many peripherals for connecting the multiple processing engines to external components. The EG and EV devices contain a GPU and the EV devices contain a video codec unit (VCU). The components of the PS are connected together and to the PL through a multi-layered ARM AMBA AXI non-blocking interconnect that supports multiple simultaneous master-slave transactions. Traffic through the interconnect can be regulated by the quality of service (QoS) block in the interconnect. Twelve dedicated AXI 32-bit, 64-bit, or 128-bit ports connect the PL to high-speed interconnect and DDR in the PS via a FIFO interface.

There are four independently controllable power domains: the PL plus three within the PS (full power, lower power, and battery power domains). Additionally, many peripherals support clock gating and power gating to further reduce dynamic and static power consumption.

## Application Processing Unit (APU)

The APU has a feature-rich dual-core or quad-core ARM Cortex-A53 processor. Cortex-A53 cores are 32-bit/64-bit application processors based on ARM-v8A architecture, offering the best performance-to-power ratio. The ARMv8 architecture supports hardware virtualization. Each of the Cortex-A53 cores has: 32KB of instruction and data L1 caches, with parity and ECC protection respectively; a NEON SIMD engine; and a single and double precision floating point unit. In addition to these blocks, the APU consists of a snoop control unit and a 1MB L2 cache with ECC protection to enhance system-level performance. The snoop control unit keeps the L1 caches coherent thus eliminating the need of spending software bandwidth for coherency. The APU also has a built-in interrupt controller supporting virtual interrupts. The APU communicates to the rest of the PS through 128-bit AXI coherent extension (ACE) port via Cache Coherent Interconnect (CCI) block, using the System Memory Management Unit (SMMU). The APU is also connected to the Programmable Logic (PL), through the 128-bit accelerator coherency port

## Graphics Processing Unit (GPU)

The dedicated ARM Mali-400 MP2 GPU in the PS supports 2D and 3D graphics acceleration up to 1080p resolution. The Mali-400 supports OpenGL ES 1.1 and 2.0 for 3D graphics and Open VG 1.1 standards for 2D vector graphics. It has a geometry processor (GP) and 2 pixel processors to perform tile rendering operations in parallel. It has dedicated Memory management units for GP and pixel processors, which supports 4 KB page size. The GPU also has 64KB level-2 (L2) read-only cache. It supports 4X and 16X Full scene Anti-Aliasing (FSAA). It is fully autonomous, enabling maximum parallelization between APU and GPU. It has built-in hardware texture decompression, allowing the texture to remain compressed (in ETC format) in graphics hardware and decompress the required samples on the fly. It also supports efficient alpha blending of multiple layers in hardware without additional bandwidth consumption. It has a pixel fill rate of 2Mpixel/sec/MHz and a triangle rate of 0.1Mvertex/sec/MHz. The GPU supports extensive texture format for RGBA 8888, 565, and 1556 in Mono 8, 16, and YUV formats. For power sensitive applications, the GPU supports clock and power gating for each GP, pixel processors, and L2 cache. During power gating, GPU does not consume any static or dynamic power; during clock gating, it only consumes static power.

## Video Codec Unit (VCU)

The video codec unit (VCU) provides multi-standard video encoding and decoding capabilities, including: High Efficiency Video Coding (HEVC), i.e., H.265; and Advanced Video Coding (AVC), i.e., H.264 standards. The VCU is capable of simultaneous encode and decode at rates up to 4Kx2K at 60 frames per second (fps) (approx. 600Mpixel/sec) or 8Kx4K at a reduced frame rate (~15fps).

# Input/Output

All UltraScale devices, whether FPGA or MPSoC, have I/O pins for communicating to external components. In addition, in the MPSoC's PS, there are another 78 I/Os that the I/O peripherals use to communicate to external components, referred to as multiplexed I/O (MIO). If more than 78 pins are required by the I/O peripherals, the I/O pins in the PL can be used to extend the MPSoC interfacing capability, referred to as extended MIO (EMIO).

The number of I/O pins in UltraScale FPGAs and in the programmable logic of UltraScale+ MPSoCs varies depending on device and package. Each I/O is configurable and can comply with a large number of I/O standards. The I/Os are classed as high-range (HR), high-performance (HP), or high-density (HD). The HR I/Os offer the widest range of voltage support, from 1.2V to 3.3V. The HP I/Os are optimized for highest performance operation, from 1.0V to 1.8V. The HD I/Os are reduced-feature I/Os organized in banks of 24, providing voltage support from 1.2V to 3.3V.

All I/O pins are organized in banks, with 52 HP or HR pins per bank or 24 HD pins per bank. Each bank has one common $V_{CCO}$ output buffer power supply, which also powers certain input buffers. In addition, HR banks can be split into two half-banks, each with their own $V_{CCO}$ supply. Some single-ended input buffers require an internally generated or an externally applied reference voltage ($V_{REF}$). $V_{REF}$ pins can be driven directly from the PCB or internally generated using the internal $V_{REF}$ generator circuitry present in each bank.

## Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

## Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally "auto-adapt" to automatically learn and compensate for different interconnect characteristics. This enables even more margin for 10G+ and 25G+ backplanes.

## Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

# Integrated Interface Blocks for PCI Express Designs

The UltraScale architecture includes integrated blocks for PCIe technology that can be configured as an Endpoint or Root Port. UltraScale devices are compliant to the PCI Express Base Specification Revision 3.0. UltraScale+ devices are compliant to the PCI Express Base Specification Revision 3.1 for Gen3 and lower data rates, and compatible with the PCI Express Base Specification Revision 4.0 (rev 0.5) for Gen4 data rates.

The Root Port can be used to build the basis for a compatible Root Complex, to allow custom chip-to-chip communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the FPGA or MPSoC.

This block is highly configurable to system design requirements and can operate up to the maximum lane widths and data rates listed in Table 18.

*Table 18:* **PCIe Maximum Configurations**

| | Kintex UltraScale | Kintex UltraScale+ | Virtex UltraScale | Virtex UltraScale+ | Zynq UltraScale+ |
|---|---|---|---|---|---|
| Gen1 (2.5Gb/s) | x8 | x16 | x8 | x16 | x16 |
| Gen2 (5Gb/s) | x8 | x16 | x8 | x16 | x16 |
| Gen3 (8Gb/s) | x8 | x16 | x8 | x16 | x16 |
| Gen4 (16Gb/s)[1] | | x8 | | x8 | x8 |

**Notes:**

1. Transceivers in Kintex UltraScale and Virtex UltraScale devices are capable of operating at Gen4 data rates.

For high-performance applications, advanced buffering techniques of the block offer a flexible maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block for PCIe, the transceivers, block RAM, and clocking resources) into an Endpoint or Root Port solution. The system designer has control over many configurable parameters: link width and speed, maximum payload size, FPGA or MPSoC logic interface speeds, reference clock frequency, and base address register decoding and filtering.

## Cache Coherent Interconnect for Accelerators (CCIX)

CCIX is a chip-to-chip interconnect operating at data rates up to 25Gb/s that allows two or more devices to share memory in a cache coherent manner. Using PCIe for the transport layer, CCIX can operate at several standard data rates (2.5, 5, 8, and 16Gb/s) with an additional high-speed 25Gb/s option. The specification employs a subset of full coherency protocols and ensures that FPGAs used as accelerators can coherently share data with processors using different instruction set architectures.

Virtex UltraScale+ HBM devices support CCIX data rates up to 16Gb/s and contain four CCIX ports and at least four integrated blocks for PCIe. Each CCIX port requires the use of one integrated block for PCIe. If not used with a CCIX port, the integrated blocks for PCIe can still be used for PCIe communication.

## Integrated Block for Interlaken

Some UltraScale architecture-based devices include integrated blocks for Interlaken. Interlaken is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gb/s to 150Gb/s. The Interlaken integrated block in the UltraScale architecture is compliant to revision 1.2 of the Interlaken specification with data striping and de-striping across 1 to 12 lanes. Permitted configurations are: 1 to 12 lanes at up to 12.5Gb/s and 1 to 6 lanes at up to 25.78125Gb/s, enabling flexible support for up to 150Gb/s per integrated block. With multiple Interlaken blocks, certain UltraScale devices enable easy, reliable Interlaken switches and bridges.

## Integrated Block for 100G Ethernet

Compliant to the IEEE Std 802.3ba, the 100G Ethernet integrated blocks in the UltraScale architecture provide low latency 100Gb/s Ethernet ports with a wide range of user customization and statistics gathering. With support for 10 x 10.3125Gb/s (CAUI) and 4 x 25.78125Gb/s (CAUI-4) configurations, the integrated block includes both the 100G MAC and PCS logic with support for IEEE Std 1588v2 1-step and 2-step hardware timestamping.

In UltraScale+ devices, the 100G Ethernet blocks contain a Reed Solomon Forward Error Correction (RS-FEC) block, compliant to IEEE Std 802.3bj, that can be used with the Ethernet block or stand alone in user applications. These families also support OTN mapping mode in which the PCS can be operated without using the MAC.

# Stacked Silicon Interconnect (SSI) Technology

Many challenges associated with creating high-capacity devices are addressed by Xilinx with the second generation of the pioneering 3D SSI technology. SSI technology enables multiple super-logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders, to create a single device with more than 20,000 low-power inter-SLR connections. Dedicated interface tiles within the SLRs provide ultra-high bandwidth, low latency connectivity to other SLRs. Table 19 shows the number of SLRs in devices that use SSI technology and their dimensions.

*Table 19:* **UltraScale and UltraScale+ 3D IC SLR Count and Dimensions**

| | Kintex UltraScale | | Virtex UltraScale | | | | Virtex UltraScale+ | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Device | KU085 | KU115 | VU125 | VU160 | VU190 | VU440 | VU5P | VU7P | VU9P | VU11P | VU13P | VU31P | VU33P | VU35P | VU37P |
| # SLRs | 2 | 2 | 2 | 3 | 3 | 3 | 2 | 2 | 3 | 3 | 4 | 1 | 1 | 2 | 3 |
| SLR Width (in regions) | 6 | 6 | 6 | 6 | 6 | 9 | 6 | 6 | 6 | 8 | 8 | 8 | 8 | 8 | 8 |
| SLR Height (in regions) | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 4 | 4 | 4 | 4 | 4 | 4 |

# Clock Management

The clock generation and distribution components in UltraScale devices are located adjacent to the columns that contain the memory interface and input and output circuitry. This tight coupling of clocking and I/O provides low-latency clocking to the I/O for memory interfaces and other I/O protocols. Within every clock management tile (CMT) resides one mixed-mode clock manager (MMCM), two PLLs, clock distribution buffers and routing, and dedicated circuitry for implementing external memory interfaces.

## Mixed-Mode Clock Manager

The mixed-mode clock manager (MMCM) can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of the MMCM is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers (D, M, and O) that are programmable by configuration and during normal operation via the Dynamic Reconfiguration Port (DRP). The pre-divider D reduces the input frequency and feeds one input of the phase/frequency comparator. The feedback divider M acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each phase can be selected to drive one of the output dividers, and each divider is programmable by configuration to divide by any integer from 1 to 128.

The MMCM has three input-jitter filter options: low bandwidth, high bandwidth, or optimized mode. Low-Bandwidth mode has the best jitter attenuation. High-Bandwidth mode has the best phase offset. Optimized mode allows the tools to find the best setting.

# UltraRAM

UltraRAM is a high-density, dual-port, synchronous memory block available in UltraScale+ devices. Both of the ports share the same clock and can address all of the 4K x 72 bits. Each port can independently read from or write to the memory array. UltraRAM supports two types of write enable schemes. The first mode is consistent with the block RAM byte write enable mode. The second mode allows gating the data and parity byte writes separately. UltraRAM blocks can be connected together to create larger memory arrays. Dedicated routing in the UltraRAM column enables the entire column height to be connected together. If additional density is required, all the UltraRAM columns in an SLR can be connected together with a few fabric resources to create single instances of RAM approximately 100Mb in size. This makes UltraRAM an ideal solution for replacing external memories such as SRAM. Cascadable anywhere from 288Kb to 100Mb, UltraRAM provides the flexibility to fulfill many different memory requirements.

## Error Detection and Correction

Each 64-bit-wide UltraRAM can generate, store and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process.

# High Bandwidth Memory (HBM)

Virtex UltraScale+ HBM devices incorporate 4GB HBM stacks adjacent to the FPGA die. Using stacked silicon interconnect technology, the FPGA communicates to the HBM stacks through memory controllers that connect to dedicated low-inductance interconnect in the silicon interposer. Each Virtex UltraScale+ HBM FPGA contains one or two HBM stacks, resulting in up to 8GB of HBM per FPGA.

The FPGA has 32 HBM AXI interfaces used to communicate with the HBM. Through a built-in switch mechanism, any of the 32 HBM AXI interfaces can access any memory address on either one or both of the HBM stacks due to the flexible addressing feature. This flexible connection between the FPGA and the HBM stacks results in easy floorplanning and timing closure. The memory controllers perform read and write reordering to improve bus efficiency. Data integrity is ensured through error checking and correction (ECC) circuitry.

# Configurable Logic Block

Every Configurable Logic Block (CLB) in the UltraScale architecture contains 8 LUTs and 16 flip-flops. The LUTs can be configured as either one 6-input LUT with one output, or as two 5-input LUTs with separate outputs but common inputs. Each LUT can optionally be registered in a flip-flop. In addition to the LUTs and flip-flops, the CLB contains arithmetic carry logic and multiplexers to create wider logic functions.

Each CLB contains one slice. There are two types of slices: SLICEL and SLICEM. LUTs in the SLICEM can be configured as 64-bit RAM, as 32-bit shift registers (SRL32), or as two SRL16s. CLBs in the UltraScale architecture have increased routing and connectivity compared to CLBs in previous-generation Xilinx devices. They also have additional control signals to enable superior register packing, resulting in overall higher device utilization.

## Interconnect

Various length vertical and horizontal routing resources in the UltraScale architecture that span 1, 2, 4, 5, 12, or 16 CLBs ensure that all signals can be transported from source to destination with ease, providing support for the next generation of wide data buses to be routed across even the highest capacity devices while simultaneously improving quality of results and software run time.

## Digital Signal Processing

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All UltraScale devices have many dedicated, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 27 × 18 bit twos complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The 96-bit-wide XOR function, programmable to 12, 24, 48, or 96-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP also includes a 48-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

## System Monitor

The System Monitor blocks in the UltraScale architecture are used to enhance the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors and external channels to the ADC.

All UltraScale architecture-based devices contain at least one System Monitor. The System Monitor in UltraScale+ FPGAs and the PL of Zynq UltraScale+ MPSoCs is similar to the Kintex UltraScale and Virtex UltraScale devices but with additional features including a PMBus interface.

Zynq UltraScale+ MPSoCs contain an additional System Monitor block in the PS. See Table 20.

*Table 20:* **Key System Monitor Features**

| | Kintex UltraScale<br>Virtex UltraScale | Kintex UltraScale+<br>Virtex UltraScale+<br>Zynq UltraScale+ MPSoC PL | Zynq UltraScale+ MPSoC PS |
|---|---|---|---|
| ADC | 10-bit 200kSPS | 10-bit 200kSPS | 10-bit 1MSPS |
| Interfaces | JTAG, I2C, DRP | JTAG, I2C, DRP, PMBus | APB |

In FPGAs and the MPSoC PL, sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, PMBus, or I2C interfaces. The I2C interface and PMBus allow the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

The System Monitor in the MPSoC PS uses a 10-bit, 1 mega-sample-per-second (MSPS) ADC to digitize the sensor outputs. The measurements are stored in registers and are accessed via the Advanced Peripheral Bus (APB) interface by the processors and the platform management unit (PMU) in the PS.

# Configuration

The UltraScale architecture-based devices store their customized configuration in SRAM-type internal latches. The configuration storage is volatile and must be reloaded whenever the device is powered up. This storage can also be reloaded at any time. Several methods and data formats for loading configuration are available, determined by the mode pins, with more dedicated configuration datapath pins to simplify the configuration process.

UltraScale architecture-based devices support secure and non-secure boot with optional Advanced Encryption Standard - Galois/Counter Mode (AES-GCM) decryption and authentication logic. If only authentication is required, the UltraScale architecture provides an alternative form of authentication in the form of RSA algorithms. For RSA authentication support in the Kintex UltraScale and Virtex UltraScale families, go to UG570, *UltraScale Architecture Configuration User Guide*.

UltraScale architecture-based devices also have the ability to select between multiple configurations, and support robust field-update methodologies. This is especially useful for updates to a design after the end product has been shipped. Designers can release their product with an early version of the design, thus getting their product to market faster. This feature allows designers to keep their customers current with the most up-to-date design while the product is already deployed in the field.

## Booting MPSoCs

Zynq UltraScale+ MPSoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the AES-GCM, SHA-3/384 decryption/authentication, and 4096-bit RSA blocks decrypt and authenticate the image.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NAND, Quad-SPI, SD, eMMC, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. One of the CPUs, Cortex-A53 or Cortex-R5, executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip memory (OCM).

The ordering information shown in Figure 4 applies to all packages in the Kintex UltraScale+ and Virtex UltraScale+ FPGAs, and Figure 5 applies to Zynq UltraScale+s.

The -1L and -2L speed grades in the UltraScale+ families can run at one of two different $V_{CCINT}$ operating voltages. At 0.72V, they operate at similar performance to the Kintex UltraScale and Virtex UltraScale devices with up to 30% reduction in power consumption. At 0.85V, they consume similar power to the Kintex UltraScale and Virtex UltraScale devices, but operate over 30% faster.

For UltraScale+ devices, the information in this document is pre-release, provided ahead of silicon ordering availability. Please contact your Xilinx sales representative for more information on Early Access Programs.

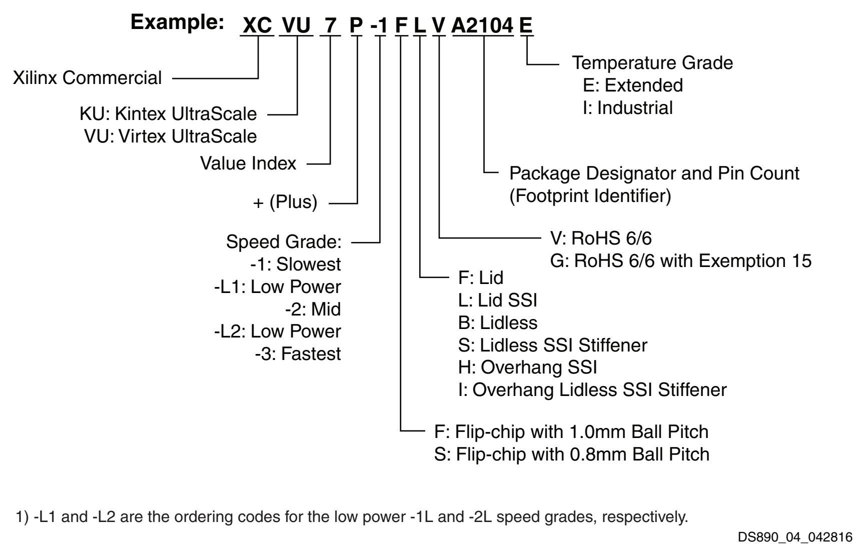


*Figure 4:* **UltraScale+ FPGA Ordering Information**

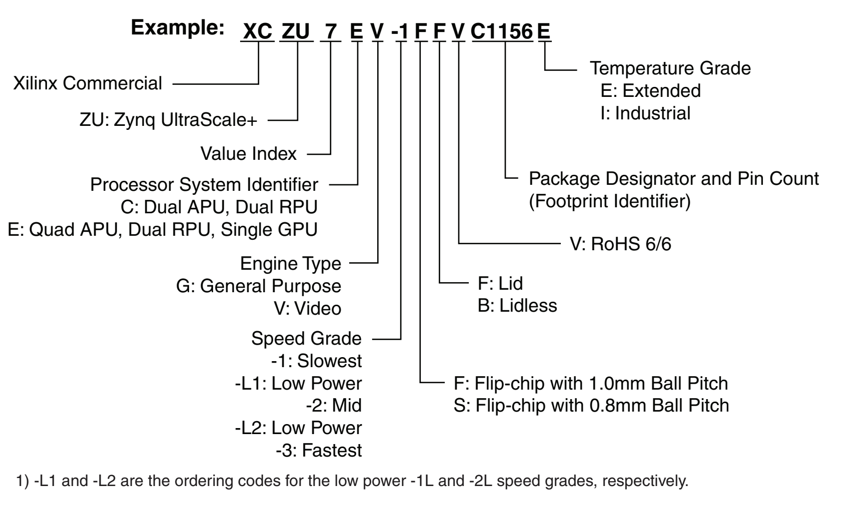


*Figure 5:* **Zynq UltraScale+ Ordering Information**

# Disclaimer



# Automotive Applications Disclaimer