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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |   |
|--------------------------------|---|
| Product Status                 | Active  |
| Number of LABs/CLBs            | 147780  |
| Number of Logic Elements/Cells | 2586150   |
| Total RAM Bits                 | 391168000   |
| Number of I/O                  | 702   |
| Number of Gates                | -   |
| Voltage - Supply               | 0.825V ~ 0.876V   |
| Mounting Type                  | Surface Mount   |
| Operating Temperature          | 0°C ~ 100°C (TJ)  |
| Package / Case                 | 2104-BBGA, FCBGA  |
| Supplier Device Package        | 2104-FCBGA (47.5x47.5)  |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/xilinx/xcvu9p-2flgb2104e">https://www.e-xfl.com/product-detail/xilinx/xcvu9p-2flgb2104e</a> |

# Summary of Features

## Processing System Overview

UltraScale+ MPSoCs feature dual and quad core variants of the ARM Cortex-A53 (APU) with dual-core ARM Cortex-R5 (RPU) processing system (PS). Some devices also include a dedicated ARM Mali™-400 MP2 graphics processing unit (GPU). See [Table 2](#).

*Table 2: Zynq UltraScale+ MPSoC Device Features*

|     | CG Devices               | EG Devices               | EV Devices               |
|-----|--------------------------|--------------------------|--------------------------|
| APU | Dual-core ARM Cortex-A53 | Quad-core ARM Cortex-A53 | Quad-core ARM Cortex-A53 |
| RPU | Dual-core ARM Cortex-R5  | Dual-core ARM Cortex-R5  | Dual-core ARM Cortex-R5  |
| GPU | –                        | Mali-400MP2              | Mali-400MP2              |
| VCU | –                        | –                        | H.264/H.265              |

To support the processors' functionality, a number of peripherals with dedicated functions are included in the PS. For interfacing to external memories for data or configuration storage, the PS includes a multi-protocol dynamic memory controller, a DMA controller, a NAND controller, an SD/eMMC controller and a Quad SPI controller. In addition to interfacing to external memories, the APU also includes a Level-1 (L1) and Level-2 (L2) cache hierarchy; the RPU includes an L1 cache and Tightly Coupled memory subsystem. Each has access to a 256KB on-chip memory.

For high-speed interfacing, the PS includes 4 channels of transmit (TX) and receive (RX) pairs of transceivers, called PS-GTR transceivers, supporting data rates of up to 6.0Gb/s. These transceivers can interface to the high-speed peripheral blocks to support PCIe Gen2 root complex or end point in x1, x2, or x4 configurations; Serial-ATA (SATA) at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates; and up to two lanes of Display Port at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s data rates. The PS-GTR transceivers can also interface to components over USB 3.0 and Serial Gigabit Media Independent Interface (SGMII).

For general connectivity, the PS includes: a pair of USB 2.0 controllers, which can be configured as host, device, or On-The-Go (OTG); an I2C controller; a UART; and a CAN2.0B controller that conforms to ISO11898-1. There are also four triple speed Ethernet MACs and 128 bits of GPIO, of which 78 bits are available through the MIO and 96 through the EMIO.

High-bandwidth connectivity based on the ARM AMBA® AXI4 protocol connects the processing units with the peripherals and provides interface between the PS and the programmable logic (PL).

For additional information, go to: [DS891](#), *Zynq UltraScale+ MPSoC Overview*.

## Migrating Devices

UltraScale and UltraScale+ families provide footprint compatibility to enable users to migrate designs from one device or family to another. Any two packages with the same footprint identifier code are footprint compatible. For example, Kintex UltraScale devices in the A1156 packages are footprint compatible with Kintex UltraScale+ devices in the A1156 packages. Likewise, Virtex UltraScale devices in the B2104 packages are compatible with Virtex UltraScale+ devices and Kintex UltraScale devices in the B2104 packages. All valid device/package combinations are provided in the Device-Package Combinations and Maximum I/Os tables in this document. Refer to [UG583](#), *UltraScale Architecture PCB Design User Guide* for more detail on migrating between UltraScale and UltraScale+ devices and packages.

# Kintex UltraScale FPGA Feature Summary

Table 3: Kintex UltraScale FPGA Feature Summary

|  | KU025 <sup>(1)</sup> | KU035   | KU040   | KU060   | KU085     | KU095     | KU115     |
|--|----------------------|---------|---------|---------|-----------|-----------|-----------|
| System Logic Cells                       | 318,150              | 444,343 | 530,250 | 725,550 | 1,088,325 | 1,176,000 | 1,451,100 |
| CLB Flip-Flops                           | 290,880              | 406,256 | 484,800 | 663,360 | 995,040   | 1,075,200 | 1,326,720 |
| CLB LUTs                                 | 145,440              | 203,128 | 242,400 | 331,680 | 497,520   | 537,600   | 663,360   |
| Maximum Distributed RAM (Mb)             | 4.1                  | 5.9     | 7.0     | 9.1     | 13.4      | 4.7       | 18.3      |
| Block RAM Blocks                         | 360                  | 540     | 600     | 1,080   | 1,620     | 1,680     | 2,160     |
| Block RAM (Mb)                           | 12.7                 | 19.0    | 21.1    | 38.0    | 56.9      | 59.1      | 75.9      |
| CMTs (1 MMCM, 2 PLLs)                    | 6                    | 10      | 10      | 12      | 22        | 16        | 24        |
| I/O DLLs                                 | 24                   | 40      | 40      | 48      | 56        | 64        | 64        |
| Maximum HP I/Os <sup>(2)</sup>           | 208                  | 416     | 416     | 520     | 572       | 650       | 676       |
| Maximum HR I/Os <sup>(3)</sup>           | 104                  | 104     | 104     | 104     | 104       | 52        | 156       |
| DSP Slices                               | 1,152                | 1,700   | 1,920   | 2,760   | 4,100     | 768       | 5,520     |
| System Monitor                           | 1                    | 1       | 1       | 1       | 2         | 1         | 2         |
| PCIe Gen3 x8                             | 1                    | 2       | 3       | 3       | 4         | 4         | 6         |
| 150G Interlaken                          | 0                    | 0       | 0       | 0       | 0         | 2         | 0         |
| 100G Ethernet                            | 0                    | 0       | 0       | 0       | 0         | 2         | 0         |
| GTH 16.3Gb/s Transceivers <sup>(4)</sup> | 12                   | 16      | 20      | 32      | 56        | 32        | 64        |
| GTY 16.3Gb/s Transceivers <sup>(5)</sup> | 0                    | 0       | 0       | 0       | 0         | 32        | 0         |
| Transceiver Fractional PLLs              | 0                    | 0       | 0       | 0       | 0         | 16        | 0         |

## Notes:

1. Certain advanced configuration features are not supported in the KU025. Refer to the [Configuring FPGAs](#) section for details.
2. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
3. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
4. GTH transceivers in SF/FB packages support data rates up to 12.5Gb/s. See [Table 4](#).
5. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s. See [Table 4](#).

# Virtex UltraScale FPGA Feature Summary

Table 7: Virtex UltraScale FPGA Feature Summary

|                                | VU065   | VU080   | VU095     | VU125     | VU160     | VU190     | VU440     |
|--------------------------------|---------|---------|-----------|-----------|-----------|-----------|-----------|
| System Logic Cells             | 783,300 | 975,000 | 1,176,000 | 1,566,600 | 2,026,500 | 2,349,900 | 5,540,850 |
| CLB Flip-Flops                 | 716,160 | 891,424 | 1,075,200 | 1,432,320 | 1,852,800 | 2,148,480 | 5,065,920 |
| CLB LUTs                       | 358,080 | 445,712 | 537,600   | 716,160   | 926,400   | 1,074,240 | 2,532,960 |
| Maximum Distributed RAM (Mb)   | 4.8     | 3.9     | 4.8       | 9.7       | 12.7      | 14.5      | 28.7      |
| Block RAM Blocks               | 1,260   | 1,421   | 1,728     | 2,520     | 3,276     | 3,780     | 2,520     |
| Block RAM (Mb)                 | 44.3    | 50.0    | 60.8      | 88.6      | 115.2     | 132.9     | 88.6      |
| CMT (1 MMCM, 2 PLLs)           | 10      | 16      | 16        | 20        | 28        | 30        | 30        |
| I/O DLLs                       | 40      | 64      | 64        | 80        | 120       | 120       | 120       |
| Maximum HP I/Os <sup>(1)</sup> | 468     | 780     | 780       | 780       | 650       | 650       | 1,404     |
| Maximum HR I/Os <sup>(2)</sup> | 52      | 52      | 52        | 104       | 52        | 52        | 52        |
| DSP Slices                     | 600     | 672     | 768       | 1,200     | 1,560     | 1,800     | 2,880     |
| System Monitor                 | 1       | 1       | 1         | 2         | 3         | 3         | 3         |
| PCIe Gen3 x8                   | 2       | 4       | 4         | 4         | 4         | 6         | 6         |
| 150G Interlaken                | 3       | 6       | 6         | 6         | 8         | 9         | 0         |
| 100G Ethernet                  | 3       | 4       | 4         | 6         | 9         | 9         | 3         |
| GTH 16.3Gb/s Transceivers      | 20      | 32      | 32        | 40        | 52        | 60        | 48        |
| GTY 30.5Gb/s Transceivers      | 20      | 32      | 32        | 40        | 52        | 60        | 0         |
| Transceiver Fractional PLLs    | 10      | 16      | 16        | 20        | 26        | 30        | 0         |

## Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

# Virtex UltraScale Device-Package Combinations and Maximum I/Os

Table 8: Virtex UltraScale Device-Package Combinations and Maximum I/Os

| Package <sup>(1)(2)(3)</sup> | Package Dimensions (mm) | VU065              | VU080              | VU095              | VU125              | VU160              | VU190              | VU440              |
|------------------------------|-------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
|                              |                         | HR, HP<br>GTH, GTY | HR, HP<br>GTH, GTY | HR, HP<br>GTH, GTY | HR, HP<br>GTH, GTY | HR, HP<br>GTH, GTY | HR, HP<br>GTH, GTY | HR, HP<br>GTH, GTY |
| FFVC1517                     | 40x40                   | 52, 468<br>20, 20  | 52, 468<br>20, 20  | 52, 468<br>20, 20  |                    |                    |                    |                    |
| FFVD1517                     | 40x40                   |                    | 52, 286<br>32, 32  | 52, 286<br>32, 32  |                    |                    |                    |                    |
| FLVD1517                     | 40x40                   |                    |                    |                    | 52, 286<br>40, 32  |                    |                    |                    |
| FFVB1760                     | 42.5x42.5               |                    | 52, 650<br>32, 16  | 52, 650<br>32, 16  |                    |                    |                    |                    |
| FLVB1760                     | 42.5x42.5               |                    |                    |                    | 52, 650<br>36, 16  |                    |                    |                    |
| FFVA2104                     | 47.5x47.5               |                    | 52, 780<br>28, 24  | 52, 780<br>28, 24  |                    |                    |                    |                    |
| FLVA2104                     | 47.5x47.5               |                    |                    |                    | 52, 780<br>28, 24  |                    |                    |                    |
| FFVB2104                     | 47.5x47.5               |                    | 52, 650<br>32, 32  | 52, 650<br>32, 32  |                    |                    |                    |                    |
| FLVB2104                     | 47.5x47.5               |                    |                    |                    | 52, 650<br>40, 36  |                    |                    |                    |
| FLGB2104                     | 47.5x47.5               |                    |                    |                    |                    | 52, 650<br>40, 36  | 52, 650<br>40, 36  |                    |
| FFVC2104                     | 47.5x47.5               |                    |                    | 52, 364<br>32, 32  |                    |                    |                    |                    |
| FLVC2104                     | 47.5x47.5               |                    |                    |                    | 52, 364<br>40, 40  |                    |                    |                    |
| FLGC2104                     | 47.5x47.5               |                    |                    |                    |                    | 52, 364<br>52, 52  | 52, 364<br>52, 52  |                    |
| FLGB2377                     | 50x50                   |                    |                    |                    |                    |                    |                    | 52, 1248<br>36, 0  |
| FLGA2577                     | 52.5x52.5               |                    |                    |                    |                    |                    | 0, 448<br>60, 60   |                    |
| FLGA2892                     | 55x55                   |                    |                    |                    |                    |                    |                    | 52, 1404<br>48, 0  |

## Notes:

- Go to [Ordering Information](#) for package designation details.
- All packages have 1.0mm ball pitch.
- Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.

# Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 10: Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

| Package<br>(1)(2)(3) | Package<br>Dimensions<br>(mm) | VU3P    | VU5P    | VU7P    | VU9P     | VU11P   | VU13P    | VU31P   | VU33P   | VU35P   | VU37P   |
|----------------------|-------------------------------|---------|---------|---------|----------|---------|----------|---------|---------|---------|---------|
|                      |                               | HP, GTY | HP, GTY | HP, GTY | HP, GTY  | HP, GTY | HP, GTY  | HP, GTY | HP, GTY | HP, GTY | HP, GTY |
| FFVC1517             | 40x40                         | 520, 40 |         |         |          |         |          |         |         |         |         |
| FLGF1924(4)          | 45x45                         |         |         |         |          | 624, 64 |          |         |         |         |         |
| FLVA2104             | 47.5x47.5                     |         | 832, 52 | 832, 52 |          |         |          |         |         |         |         |
| FLGA2104             | 47.5x47.5                     |         |         |         | 832, 52  |         |          |         |         |         |         |
| FHGA2104             | 52.5x52.5(5)                  |         |         |         |          |         | 832, 52  |         |         |         |         |
| FLVB2104             | 47.5x47.5                     |         | 702, 76 | 702, 76 |          |         |          |         |         |         |         |
| FLGB2104             | 47.5x47.5                     |         |         |         | 702, 76  | 572, 76 |          |         |         |         |         |
| FHGB2104             | 52.5x52.5(5)                  |         |         |         |          |         | 702, 76  |         |         |         |         |
| FLVC2104             | 47.5x47.5                     |         | 416, 80 | 416, 80 |          |         |          |         |         |         |         |
| FLGC2104             | 47.5x47.5                     |         |         |         | 416, 104 | 416, 96 |          |         |         |         |         |
| FHGC2104             | 52.5x52.5(5)                  |         |         |         |          |         | 416, 104 |         |         |         |         |
| FSGD2104             | 47.5x47.5                     |         |         |         | 676, 76  | 572, 76 |          |         |         |         |         |
| FIGD2104             | 52.5x52.5(5)                  |         |         |         |          |         | 676, 76  |         |         |         |         |
| FLGA2577             | 52.5x52.5                     |         |         |         | 448, 120 | 448, 96 | 448, 128 |         |         |         |         |
| FSVH1924             | 45x45                         |         |         |         |          |         |          | 208, 32 |         |         |         |
| FSVH2104             | 47.5x47.5                     |         |         |         |          |         |          |         | 208, 32 | 416, 64 |         |
| FSVH2892             | 55x55                         |         |         |         |          |         |          |         |         | 416, 64 | 624, 96 |

## Notes:

- Go to [Ordering Information](#) for package designation details.
- All packages have 1.0mm ball pitch.
- Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the [UltraScale Architecture Product Selection Guide](#) for details on inter-family migration.
- GTY transceivers in the FLGF1924 package support data rates up to 16.3Gb/s.
- These 52.5x52.5mm overhang packages have the same PCB ball footprint as the corresponding 47.5x47.5mm packages (i.e., the same last letter and number sequence) and are footprint compatible.

# Zynq UltraScale+: CG Device Feature Summary

Table 11: Zynq UltraScale+: CG Device Feature Summary

|   | ZU2CG   | ZU3CG   | ZU4CG   | ZU5CG   | ZU6CG   | ZU7CG   | ZU9CG   |
|---|---|---------|---------|---------|---------|---------|---------|
| Application Processing Unit             | Dual-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache |         |         |         |         |         |         |
| Real-Time Processing Unit               | Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM                     |         |         |         |         |         |         |
| Embedded and External Memory            | 256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC                           |         |         |         |         |         |         |
| General Connectivity                    | 214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters                     |         |         |         |         |         |         |
| High-Speed Connectivity                 | 4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII   |         |         |         |         |         |         |
| System Logic Cells                      | 103,320   | 154,350 | 192,150 | 256,200 | 469,446 | 504,000 | 599,550 |
| CLB Flip-Flops                          | 94,464  | 141,120 | 175,680 | 234,240 | 429,208 | 460,800 | 548,160 |
| CLB LUTs                                | 47,232  | 70,560  | 87,840  | 117,120 | 214,604 | 230,400 | 274,080 |
| Distributed RAM (Mb)                    | 1.2   | 1.8     | 2.6     | 3.5     | 6.9     | 6.2     | 8.8     |
| Block RAM Blocks                        | 150   | 216     | 128     | 144     | 714     | 312     | 912     |
| Block RAM (Mb)                          | 5.3   | 7.6     | 4.5     | 5.1     | 25.1    | 11.0    | 32.1    |
| UltraRAM Blocks                         | 0   | 0       | 48      | 64      | 0       | 96      | 0       |
| UltraRAM (Mb)                           | 0   | 0       | 14.0    | 18.0    | 0       | 27.0    | 0       |
| DSP Slices                              | 240   | 360     | 728     | 1,248   | 1,973   | 1,728   | 2,520   |
| CMTs                                    | 3   | 3       | 4       | 4       | 4       | 8       | 4       |
| Max. HP I/O <sup>(1)</sup>              | 156   | 156     | 156     | 156     | 208     | 416     | 208     |
| Max. HD I/O <sup>(2)</sup>              | 96  | 96      | 96      | 96      | 120     | 48      | 120     |
| System Monitor                          | 2   | 2       | 2       | 2       | 2       | 2       | 2       |
| GTH Transceiver 16.3Gb/s <sup>(3)</sup> | 0   | 0       | 16      | 16      | 24      | 24      | 24      |
| GTY Transceivers 32.75Gb/s              | 0   | 0       | 0       | 0       | 0       | 0       | 0       |
| Transceiver Fractional PLLs             | 0   | 0       | 8       | 8       | 12      | 12      | 12      |
| PCIe Gen3 x16 and Gen4 x8               | 0   | 0       | 2       | 2       | 0       | 2       | 0       |
| 150G Interlaken                         | 0   | 0       | 0       | 0       | 0       | 0       | 0       |
| 100G Ethernet w/ RS-FEC                 | 0   | 0       | 0       | 0       | 0       | 0       | 0       |

## Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 12](#).



# Zynq UltraScale+: CG Device-Package Combinations and Maximum I/Os

Table 12: Zynq UltraScale+: CG Device-Package Combinations and Maximum I/Os

| Package<br>(1)(2)(3)(4)(5) | Package<br>Dimensions<br>(mm) | ZU2CG              | ZU3CG              | ZU4CG              | ZU5CG              | ZU6CG              | ZU7CG              | ZU9CG              |
|----------------------------|-------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
|                            |                               | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY | HD, HP<br>GTH, GTY |
| SBVA484(6)                 | 19x19                         | 24, 58<br>0, 0     | 24, 58<br>0, 0     |                    |                    |                    |                    |                    |
| SFVA625                    | 21x21                         | 24, 156<br>0, 0    | 24, 156<br>0, 0    |                    |                    |                    |                    |                    |
| SFVC784(7)                 | 23x23                         | 96, 156<br>0, 0    | 96, 156<br>0, 0    | 96, 156<br>4, 0    | 96, 156<br>4, 0    |                    |                    |                    |
| FBVB900                    | 31x31                         |                    |                    | 48, 156<br>16, 0   | 48, 156<br>16, 0   |                    | 48, 156<br>16, 0   |                    |
| FFVC900                    | 31x31                         |                    |                    |                    |                    | 48, 156<br>16, 0   |                    | 48, 156<br>16, 0   |
| FFVB1156                   | 35x35                         |                    |                    |                    |                    | 120, 208<br>24, 0  |                    | 120, 208<br>24, 0  |
| FFVC1156                   | 35x35                         |                    |                    |                    |                    |                    | 48, 312<br>20, 0   |                    |
| FFVF1517                   | 40x40                         |                    |                    |                    |                    |                    | 48, 416<br>24, 0   |                    |

## Notes:

1. Go to [Ordering Information](#) for package designation details.
2. FB/FF packages have 1.0mm ball pitch. SB/SF packages have 0.8mm ball pitch.
3. All device package combinations bond out 4 PS-GTR transceivers.
4. All device package combinations bond out 214 PS I/O except ZU2CG and ZU3CG in the SBVA484 and SFVA625 packages, which bond out 170 PS I/Os.
5. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined.
6. All 58 HP I/O pins are powered by the same  $V_{CCO}$  supply.
7. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s.

# Zynq UltraScale+: EG Device Feature Summary

Table 15: Zynq UltraScale+: EV Device Feature Summary

|   | ZU4EV   | ZU5EV   | ZU7EV   |
|---|---|---------|---------|
| Application Processing Unit             | Quad-core ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache |         |         |
| Real-Time Processing Unit               | Dual-core ARM Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM                     |         |         |
| Embedded and External Memory            | 256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC                           |         |         |
| General Connectivity                    | 214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters                     |         |         |
| High-Speed Connectivity                 | 4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII   |         |         |
| Graphic Processing Unit                 | ARM Mali-400 MP2; 64KB L2 Cache   |         |         |
| Video Codec                             | 1   | 1       | 1       |
| System Logic Cells                      | 192,150   | 256,200 | 504,000 |
| CLB Flip-Flops                          | 175,680   | 234,240 | 460,800 |
| CLB LUTs                                | 87,840  | 117,120 | 230,400 |
| Distributed RAM (Mb)                    | 2.6   | 3.5     | 6.2     |
| Block RAM Blocks                        | 128   | 144     | 312     |
| Block RAM (Mb)                          | 4.5   | 5.1     | 11.0    |
| UltraRAM Blocks                         | 48  | 64      | 96      |
| UltraRAM (Mb)                           | 14.0  | 18.0    | 27.0    |
| DSP Slices                              | 728   | 1,248   | 1,728   |
| CMTs                                    | 4   | 4       | 8       |
| Max. HP I/O <sup>(1)</sup>              | 156   | 156     | 416     |
| Max. HD I/O <sup>(2)</sup>              | 96  | 96      | 48      |
| System Monitor                          | 2   | 2       | 2       |
| GTH Transceiver 16.3Gb/s <sup>(3)</sup> | 16  | 16      | 24      |
| GTY Transceivers 32.75Gb/s              | 0   | 0       | 0       |
| Transceiver Fractional PLLs             | 8   | 8       | 12      |
| PCIe Gen3 x16 and Gen4 x8               | 2   | 2       | 2       |
| 150G Interlaken                         | 0   | 0       | 0       |
| 100G Ethernet w/ RS-FEC                 | 0   | 0       | 0       |

## Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in the SFVC784 package support data rates up to 12.5Gb/s. See [Table 16](#).

contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. Figure 2 is a representation of an FPGA divided into regions.

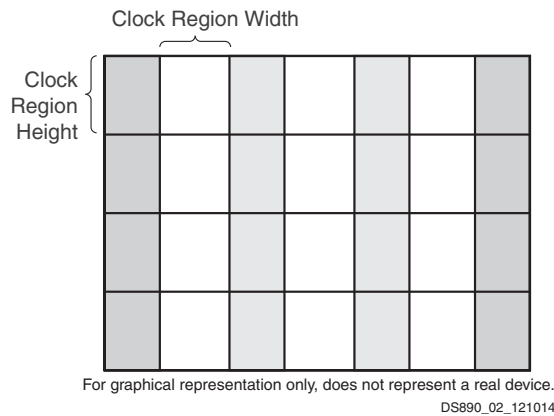


Figure 2: Column-Based FPGA Divided into Clock Regions

## Processing System (PS)

Zynq UltraScale+ MPSoCs consist of a PS coupled with programmable logic. The contents of the PS varies between the different Zynq UltraScale+ devices. All devices contain an APU, an RPU, and many peripherals for connecting the multiple processing engines to external components. The EG and EV devices contain a GPU and the EV devices contain a video codec unit (VCU). The components of the PS are connected together and to the PL through a multi-layered ARM AMBA AXI non-blocking interconnect that supports multiple simultaneous master-slave transactions. Traffic through the interconnect can be regulated by the quality of service (QoS) block in the interconnect. Twelve dedicated AXI 32-bit, 64-bit, or 128-bit ports connect the PL to high-speed interconnect and DDR in the PS via a FIFO interface.

There are four independently controllable power domains: the PL plus three within the PS (full power, lower power, and battery power domains). Additionally, many peripherals support clock gating and power gating to further reduce dynamic and static power consumption.

## Application Processing Unit (APU)

The APU has a feature-rich dual-core or quad-core ARM Cortex-A53 processor. Cortex-A53 cores are 32-bit/64-bit application processors based on ARM-v8A architecture, offering the best performance-to-power ratio. The ARMv8 architecture supports hardware virtualization. Each of the Cortex-A53 cores has: 32KB of instruction and data L1 caches, with parity and ECC protection respectively; a NEON SIMD engine; and a single and double precision floating point unit. In addition to these blocks, the APU consists of a snoop control unit and a 1MB L2 cache with ECC protection to enhance system-level performance. The snoop control unit keeps the L1 caches coherent thus eliminating the need of spending software bandwidth for coherency. The APU also has a built-in interrupt controller supporting virtual interrupts. The APU communicates to the rest of the PS through 128-bit AXI coherent extension (ACE) port via Cache Coherent Interconnect (CCI) block, using the System Memory Management Unit (SMMU). The APU is also connected to the Programmable Logic (PL), through the 128-bit accelerator coherency port

(ACP), providing a low latency coherent port for accelerators in the PL. To support real-time debug and trace, each core also has an Embedded Trace Macrocell (ETM) that communicates with the ARM CoreSight™ Debug System.

## Real-Time Processing Unit (RPU)

The RPU in the PS contains a dual-core ARM Cortex-R5 PS. Cortex-R5 cores are 32-bit real-time processor cores based on ARM-v7R architecture. Each of the Cortex-R5 cores has 32KB of level-1 (L1) instruction and data cache with ECC protection. In addition to the L1 caches, each of the Cortex-R5 cores also has a 128KB tightly coupled memory (TCM) interface for real-time single cycle access. The RPU also has a dedicated interrupt controller. The RPU can operate in either split or lock-step mode. In split mode, both processors run independently of each other. In lock-step mode, they run in parallel with each other, with integrated comparator logic, and the TCMs are used as 256KB unified memory. The RPU communicates with the rest of the PS via the 128-bit AXI-4 ports connected to the low power domain switch. It also communicates directly with the PL through 128-bit low latency AXI-4 ports. To support real-time debug and trace each core also has an embedded trace macrocell (ETM) that communicates with the ARM CoreSight Debug System.

## External Memory

The PS can interface to many types of external memories through dedicated memory controllers. The dynamic memory controller supports DDR3, DDR3L, DDR4, LPDDR3, and LPDDR4 memories. The multi-protocol DDR memory controller can be configured to access a 2GB address space in 32-bit addressing mode and up to 32GB in 64-bit addressing mode using a single or dual rank configuration of 8-bit, 16-bit, or 32-bit DRAM memories. Both 32-bit and 64-bit bus access modes are protected by ECC using extra bits.

The SD/eMMC controller supports 1 and 4 bit data interfaces at low, default, high-speed, and ultra-high-speed (UHS) clock rates. This controller also supports 1-, 4-, or 8-bit-wide eMMC interfaces that are compliant to the eMMC 4.51 specification. eMMC is one of the primary boot and configuration modes for Zynq UltraScale+ MPSoCs and supports boot from managed NAND devices. The controller has a built-in DMA for enhanced performance.

The Quad-SPI controller is one of the primary boot and configuration devices. It supports 4-byte and 3-byte addressing modes. In both addressing modes, single, dual-stacked, and dual-parallel configurations are supported. Single mode supports a quad serial NOR flash memory, while in double stacked and double parallel modes, it supports two quad serial NOR flash memories.

The NAND controller is based on ONFI3.1 specification. It has an 8-pin interface and provides 200Mb/s of bandwidth in synchronous mode. It supports 24 bits of ECC thus enabling support for SLC NAND memories. It has two chip-selects to support deeper memory and a built-in DMA for enhanced performance.

## I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards  $V_{CCO}$  or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100 $\Omega$  internal resistor. All UltraScale devices support differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL. UltraScale+ families add support for MIPI with a dedicated D-PHY in the I/O bank.

### ***3-State Digitally Controlled Impedance and Low Power I/O Features***

The 3-state Digitally Controlled Impedance (T\_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to  $V_{CCO}$  or split (Thevenin) termination to  $V_{CCO}/2$ . This allows users to eliminate off-chip termination for signals using T\_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

## I/O Logic

### ***Input and Output Delay***

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250ps of delay with a resolution of 5–15ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

### ***ISERDES and OSERDES***

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO interface.

# High-Speed Serial Transceivers

Serial data transmission between devices on the same PCB, over backplanes, and across even longer distances is becoming increasingly important for scaling to 100Gb/s and 400Gb/s line cards. Specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues are required at these high data rates.

Three types of transceivers are used in the UltraScale architecture: GTH and GTY in FPGAs and MPSoC PL, and PS-GTR in the MPSoC PS. All transceivers are arranged in groups of four, known as a transceiver Quad. Each serial transceiver is a combined transmitter and receiver. [Table 17](#) compares the available transceivers.

**Table 17: Transceiver Information**

|                | Kintex UltraScale   |   | Kintex UltraScale+  |   | Virtex UltraScale   |   | Virtex UltraScale+  | Zynq UltraScale+   |   |   |
|----------------|---|---|---|---|---|---|---|--|---|---|
| Type           | GTH   | GTY   | GTH   | GTY   | GTH   | GTY   | GTY   | PS-GTR   | GTH   | GTY   |
| Qty            | 16–64   | 0–32  | 20–60   | 0–60  | 20–60   | 0–60  | 40–128  | 4  | 0–44  | 0–28  |
| Max. Data Rate | 16.3Gb/s  | 16.3Gb/s  | 16.3Gb/s  | 32.75Gb/s   | 16.3Gb/s  | 30.5Gb/s  | 32.75Gb/s   | 6.0Gb/s  | 16.3Gb/s  | 32.75Gb/s   |
| Min. Data Rate | 0.5Gb/s   | 0.5Gb/s   | 0.5Gb/s   | 0.5Gb/s   | 0.5Gb/s   | 0.5Gb/s   | 0.5Gb/s   | 1.25Gb/s   | 0.5Gb/s   | 0.5Gb/s   |
| Key Apps       | <ul style="list-style-type: none"> <li>Backplane</li> <li>PCIe Gen4</li> <li>HMC</li> </ul> | <ul style="list-style-type: none"> <li>Backplane</li> <li>PCIe Gen4</li> <li>HMC</li> </ul> | <ul style="list-style-type: none"> <li>Backplane</li> <li>PCIe Gen4</li> <li>HMC</li> </ul> | <ul style="list-style-type: none"> <li>100G+ Optics</li> <li>Chip-to-Chip</li> <li>25G+ Backplane</li> <li>HMC</li> </ul> | <ul style="list-style-type: none"> <li>Backplane</li> <li>PCIe Gen4</li> <li>HMC</li> </ul> | <ul style="list-style-type: none"> <li>100G+ Optics</li> <li>Chip-to-Chip</li> <li>25G+ Backplane</li> <li>HMC</li> </ul> | <ul style="list-style-type: none"> <li>100G+ Optics</li> <li>Chip-to-Chip</li> <li>25G+ Backplane</li> <li>HMC</li> </ul> | <ul style="list-style-type: none"> <li>PCIe Gen2</li> <li>USB</li> <li>Ethernet</li> </ul> | <ul style="list-style-type: none"> <li>Backplane</li> <li>PCIe Gen4</li> <li>HMC</li> </ul> | <ul style="list-style-type: none"> <li>100G+ Optics</li> <li>Chip-to-Chip</li> <li>25G+ Backplane</li> <li>HMC</li> </ul> |

The following information in this section pertains to the GTH and GTY only.

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

## Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80 for the GTH and 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

## Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits in the GTH or 16, 20, 32, 40, 64, 80, 128, or 160 for the GTY. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally “auto-adapt” to automatically learn and compensate for different interconnect characteristics. This enables even more margin for 10G+ and 25G+ backplanes.

## Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

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## Cache Coherent Interconnect for Accelerators (CCIX)

CCIX is a chip-to-chip interconnect operating at data rates up to 25Gb/s that allows two or more devices to share memory in a cache coherent manner. Using PCIe for the transport layer, CCIX can operate at several standard data rates (2.5, 5, 8, and 16Gb/s) with an additional high-speed 25Gb/s option. The specification employs a subset of full coherency protocols and ensures that FPGAs used as accelerators can coherently share data with processors using different instruction set architectures.

Virtex UltraScale+ HBM devices support CCIX data rates up to 16Gb/s and contain four CCIX ports and at least four integrated blocks for PCIe. Each CCIX port requires the use of one integrated block for PCIe. If not used with a CCIX port, the integrated blocks for PCIe can still be used for PCIe communication.

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## Integrated Block for Interlaken

Some UltraScale architecture-based devices include integrated blocks for Interlaken. Interlaken is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gb/s to 150Gb/s. The Interlaken integrated block in the UltraScale architecture is compliant to revision 1.2 of the Interlaken specification with data striping and de-striping across 1 to 12 lanes. Permitted configurations are: 1 to 12 lanes at up to 12.5Gb/s and 1 to 6 lanes at up to 25.78125Gb/s, enabling flexible support for up to 150Gb/s per integrated block. With multiple Interlaken blocks, certain UltraScale devices enable easy, reliable Interlaken switches and bridges.

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## Integrated Block for 100G Ethernet

Compliant to the IEEE Std 802.3ba, the 100G Ethernet integrated blocks in the UltraScale architecture provide low latency 100Gb/s Ethernet ports with a wide range of user customization and statistics gathering. With support for 10 x 10.3125Gb/s (CAUI) and 4 x 25.78125Gb/s (CAUI-4) configurations, the integrated block includes both the 100G MAC and PCS logic with support for IEEE Std 1588v2 1-step and 2-step hardware timestamping.

In UltraScale+ devices, the 100G Ethernet blocks contain a Reed Solomon Forward Error Correction (RS-FEC) block, compliant to IEEE Std 802.3bj, that can be used with the Ethernet block or stand alone in user applications. These families also support OTN mapping mode in which the PCS can be operated without using the MAC.



## Stacked Silicon Interconnect (SSI) Technology

Many challenges associated with creating high-capacity devices are addressed by Xilinx with the second generation of the pioneering 3D SSI technology. SSI technology enables multiple super-logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders, to create a single device with more than 20,000 low-power inter-SLR connections. Dedicated interface tiles within the SLRs provide ultra-high bandwidth, low latency connectivity to other SLRs. Table 19 shows the number of SLRs in devices that use SSI technology and their dimensions.

Table 19: UltraScale and UltraScale+ 3D IC SLR Count and Dimensions

|                         | Kintex UltraScale |       | Virtex UltraScale |       |       |       | Virtex UltraScale+ |      |      |       |       |       |       |       |       |
|-------------------------|-------------------|-------|-------------------|-------|-------|-------|--------------------|------|------|-------|-------|-------|-------|-------|-------|
| Device                  | KU085             | KU115 | VU125             | VU160 | VU190 | VU440 | VU5P               | VU7P | VU9P | VU11P | VU13P | VU31P | VU33P | VU35P | VU37P |
| # SLRs                  | 2                 | 2     | 2                 | 3     | 3     | 3     | 2                  | 2    | 3    | 3     | 4     | 1     | 1     | 2     | 3     |
| SLR Width (in regions)  | 6                 | 6     | 6                 | 6     | 6     | 9     | 6                  | 6    | 6    | 8     | 8     | 8     | 8     | 8     | 8     |
| SLR Height (in regions) | 5                 | 5     | 5                 | 5     | 5     | 5     | 5                  | 5    | 5    | 4     | 4     | 4     | 4     | 4     | 4     |

## Clock Management

The clock generation and distribution components in UltraScale devices are located adjacent to the columns that contain the memory interface and input and output circuitry. This tight coupling of clocking and I/O provides low-latency clocking to the I/O for memory interfaces and other I/O protocols. Within every clock management tile (CMT) resides one mixed-mode clock manager (MMCM), two PLLs, clock distribution buffers and routing, and dedicated circuitry for implementing external memory interfaces.

### Mixed-Mode Clock Manager

The mixed-mode clock manager (MMCM) can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of the MMCM is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers (D, M, and O) that are programmable by configuration and during normal operation via the Dynamic Reconfiguration Port (DRP). The pre-divider D reduces the input frequency and feeds one input of the phase/frequency comparator. The feedback divider M acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each phase can be selected to drive one of the output dividers, and each divider is programmable by configuration to divide by any integer from 1 to 128.

The MMCM has three input-jitter filter options: low bandwidth, high bandwidth, or optimized mode. Low-Bandwidth mode has the best jitter attenuation. High-Bandwidth mode has the best phase offset. Optimized mode allows the tools to find the best setting.

The MMCM can have a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of 1/8 and can thus increase frequency synthesis capabilities by a factor of 8. The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency. At 1,600MHz, the phase-shift timing increment is 11.2ps.

## PLL

With fewer features than the MMCM, the two PLLs in a clock management tile are primarily present to provide the necessary clocks to the dedicated memory interface circuitry. The circuit at the center of the PLLs is similar to the MMCM, with PFD feeding a VCO and programmable M, D, and O counters. There are two divided outputs to the device fabric per PLL as well as one clock plus one enable signal to the memory interface circuitry.

UltraScale+ MPSoCs are equipped with five additional PLLs in the PS for independently configuring the four primary clock domains with the PS: the APU, the RPU, the DDR controller, and the I/O peripherals.

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## Clock Distribution

Clocks are distributed throughout UltraScale devices via buffers that drive a number of vertical and horizontal tracks. There are 24 horizontal clock routes per clock region and 24 vertical clock routes per clock region with 24 additional vertical clock routes adjacent to the MMCM and PLL. Within a clock region, clock signals are routed to the device logic (CLBs, etc.) via 16 gateable leaf clocks.

Several types of clock buffers are available. The BUFGCE and BUFCE\_LEAF buffers provide clock gating at the global and leaf levels, respectively. BUFGCTRL provides glitchless clock muxing and gating capability. BUFGCE\_DIV has clock gating capability and can divide a clock by 1 to 8. BUFG\_GT performs clock division from 1 to 8 for the transceiver clocks. In MPSoCs, clocks can be transferred from the PS to the PL using dedicated buffers.

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## Memory Interfaces

Memory interface data rates continue to increase, driving the need for dedicated circuitry that enables high performance, reliable interfacing to current and next-generation memory technologies. Every UltraScale device includes dedicated physical interfaces (PHY) blocks located between the CMT and I/O columns that support implementation of high-performance PHY blocks to external memories such as DDR4, DDR3, QDRII+, and RLDRAM3. The PHY blocks in each I/O bank generate the address/control and data bus signaling protocols as well as the precision clock/data alignment required to reliably communicate with a variety of high-performance memory standards. Multiple I/O banks can be used to create wider memory interfaces.

As well as external parallel memory interfaces, UltraScale FPGAs and MPSoCs can communicate to external serial memories, such as Hybrid Memory Cube (HMC), via the high-speed serial transceivers. All transceivers in the UltraScale architecture support the HMC protocol, up to 15Gb/s line rates. UltraScale devices support the highest bandwidth HMC configuration of 64 lanes with a single FPGA.

Zynq UltraScale+ MPSoCs contain an additional System Monitor block in the PS. See [Table 20](#).

**Table 20: Key System Monitor Features**

|            | Kintex UltraScale<br>Virtex UltraScale | Kintex UltraScale+<br>Virtex UltraScale+<br>Zynq UltraScale+ MPSoC PL | Zynq UltraScale+ MPSoC PS |
|------------|--|---|---------------------------|
| ADC        | 10-bit 200kSPS                         | 10-bit 200kSPS  | 10-bit 1MSPS              |
| Interfaces | JTAG, I2C, DRP                         | JTAG, I2C, DRP, PMBus   | APB                       |

In FPGAs and the MPSoC PL, sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, PMBus, or I2C interfaces. The I2C interface and PMBus allow the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

The System Monitor in the MPSoC PS uses a 10-bit, 1 mega-sample-per-second (MSPS) ADC to digitize the sensor outputs. The measurements are stored in registers and are accessed via the Advanced Peripheral Bus (APB) interface by the processors and the platform management unit (PMU) in the PS.

## Configuration

The UltraScale architecture-based devices store their customized configuration in SRAM-type internal latches. The configuration storage is volatile and must be reloaded whenever the device is powered up. This storage can also be reloaded at any time. Several methods and data formats for loading configuration are available, determined by the mode pins, with more dedicated configuration datapath pins to simplify the configuration process.

UltraScale architecture-based devices support secure and non-secure boot with optional Advanced Encryption Standard - Galois/Counter Mode (AES-GCM) decryption and authentication logic. If only authentication is required, the UltraScale architecture provides an alternative form of authentication in the form of RSA algorithms. For RSA authentication support in the Kintex UltraScale and Virtex UltraScale families, go to [UG570](#), *UltraScale Architecture Configuration User Guide*.

UltraScale architecture-based devices also have the ability to select between multiple configurations, and support robust field-update methodologies. This is especially useful for updates to a design after the end product has been shipped. Designers can release their product with an early version of the design, thus getting their product to market faster. This feature allows designers to keep their customers current with the most up-to-date design while the product is already deployed in the field.

## Booting MPSoCs

Zynq UltraScale+ MPSoCs use a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the AES-GCM, SHA-3/384 decryption/authentication, and 4096-bit RSA blocks decrypt and authenticate the image.

Upon reset, the device mode pins are read to determine the primary boot device to be used: NAND, Quad-SPI, SD, eMMC, or JTAG. JTAG can only be used as a non-secure boot source and is intended for debugging purposes. One of the CPUs, Cortex-A53 or Cortex-R5, executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip memory (OCM).

Table 21: Speed Grade and Temperature Grade (Cont'd)

| Device Family    | Devices   | Speed Grade and Temperature Grade |               |   |                                      |
|------------------|---|-----------------------------------|---------------|---|--------------------------------------|
|                  |   | Commercial (C)                    | Extended (E)  |   | Industrial (I)                       |
|                  |   | 0°C to +85°C                      | 0°C to +100°C | 0°C to +110°C                           | –40°C to +100°C                      |
| Zynq UltraScale+ | CG Devices  |                                   | -2E (0.85V)   |   | -2I (0.85V)                          |
|                  |   |                                   |               | -2LE <sup>(2)(3)</sup> (0.85V or 0.72V) |                                      |
|                  |   |                                   | -1E (0.85V)   |   | -1I (0.85V)                          |
|                  |   |                                   |               |   | -1LI <sup>(3)</sup> (0.85V or 0.72V) |
|                  | ZU2EG<br>ZU3EG  |                                   | -2E (0.85V)   |   | -2I (0.85V)                          |
|                  |   |                                   |               | -2LE <sup>(2)(3)</sup> (0.85V or 0.72V) |                                      |
|                  |   |                                   | -1E (0.85V)   |   | -1I (0.85V)                          |
|                  |   |                                   |               |   | -1LI <sup>(3)</sup> (0.85V or 0.72V) |
|                  | ZU4EG<br>ZU5EG<br>ZU6EG<br>ZU7EG<br>ZU9EG<br>ZU11EG<br>ZU15EG<br>ZU17EG<br>ZU19EG |                                   | -3E (0.90V)   |   |                                      |
|                  |   |                                   | -2E (0.85V)   |   | -2I (0.85V)                          |
|                  |   |                                   |               | -2LE <sup>(2)(3)</sup> (0.85V or 0.72V) |                                      |
|                  |   |                                   | -1E (0.85V)   |   | -1I (0.85V)                          |
|                  |   |                                   |               |   | -1LI <sup>(3)</sup> (0.85V or 0.72V) |
|                  |   |                                   |               |   |                                      |
|                  |   |                                   |               |   |                                      |
|                  |   |                                   |               |   |                                      |
|                  | EV Devices  |                                   | -3E (0.90V)   |   |                                      |
|                  |   |                                   | -2E (0.85V)   |   | -2I (0.85V)                          |
|                  |   |                                   |               | -2LE <sup>(2)(3)</sup> (0.85V or 0.72V) |                                      |
|                  |   |                                   | -1E (0.85V)   |   | -1I (0.85V)                          |
|                  |   |                                   |               |   | -1LI <sup>(3)</sup> (0.85V or 0.72V) |

**Notes:**

1. KU025 and KU095 are not available in -3E or -1LI speed/temperature grades.
2. In -2LE speed/temperature grade, devices can operate for a limited time with junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal at 0.85V or low voltage at 0.72V). Operation at 110°C Tj is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of device lifetime.
3. In Zynq UltraScale+ MPSoCs, when operating the PL at low voltage (0.72V), the PS operates at nominal voltage (0.85V).

| <b>Date</b> | <b>Version</b> | <b>Description of Revisions</b>   |
|-------------|----------------|---|
| 02/06/2014  | 1.1            | Updated PCIe information in <a href="#">Table 1</a> and <a href="#">Table 3</a> . Added FFVJ1924 package to <a href="#">Table 8</a> . |
| 12/10/2013  | 1.0            | Initial Xilinx release.   |