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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	13
Voltage - Supply	8V ~ 18V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	54-SSOP (0.295", 7.50mm Width) Exposed Pad
Supplier Device Package	54-SOIC-EP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e625acdwb

INTERNAL BLOCK DIAGRAM

Figure 2. 908E625 Simplified Internal Block Diagram

Table 1. 908E625 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 14.

Pin Function	Pin	Pin Name	Formal Name	Definition
MCU	42	PTE1/RXD	Port E I/O	This pin is a special function, bi-directional I/O port pin that can is shared with other functional modules in the MCU.
MCU	43 48	VREFL VREFH	ADC References	These pins are the reference voltage pins for the analog-to-digital converter (ADC).
MCU	44 47	VSSA VDDA	ADC Supply pins	These pins are the power supply pins for the analog-to-digital converter.
MCU	45 46	EVSS EVDD	MCU Power Supply Pins	These pins are the ground and power supply pins, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These pins are special function, bi-directional I/O port pins that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Pin	For test purposes only. Do not connect in the application.
Analog	15	FGEN	Current Limitation Frequency Input	This is the input pin for the half-bridge current limitation and the high side inrush current limiter PWM frequency.
Analog	16	BEMF	Back Electromagnetic Force Output	This pin gives the user information about back electromagnetic force (BEMF).
Analog	17	$\overline{\text{RST\_A}}$	Internal Reset	This pin is the bi-directional reset pin of the analog die.
Analog	18	$\overline{\text{IRQ\_A}}$	Internal Interrupt Output	This pin is the interrupt output pin of the analog die indicating errors or wake-up events.
Analog	19	$\overline{\text{SS}}$	Slave Select	This pin is the SPI slave select pin for the analog chip.
Analog	20	LIN	LIN Bus	This pin represents the single wire bus transmitter and receiver.
Analog	23 26 29 32	HB1 HB2 HB3 HB4	Half-bridge Outputs	This device includes power MOSFETs configured as four half-bridge driver outputs. These outputs may be configured for step motor drivers, DC motor drivers, or as high side and low side switches.
Analog	24 27 31	VSUP1 VSUP2 VSUP3	Power Supply Pins	These pins are device power supply pins.
Analog	25 30	GND1 GND2	Power Ground Pins	These pins are device power ground connections.
Analog	28	HS	High-Side Output	This output pin is a low $R_{DS(ON)}$ high side switch.
Analog	34	HVDD	Switchable V_{DD} Output	This pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; e.g., 3-pin Hall-effect sensors.
Analog	35 36 37	H3 H2 H1	Hall-effect Sensor Inputs	These pins provide inputs for Hall-effect sensors and switches.
Analog	38	VDD	Voltage Regulator Output	The +5.0 V voltage regulator output pin is intended to supply the embedded microcontroller.
Analog	39	PA1	Analog Input	This pin is an analog input port with selectable source values.
Analog	40	VSS	Voltage Regulator Ground	Ground pin for the connection of all non-power ground connections (microcontroller and sensors).
Analog	41	RXD	LIN Transceiver Output	This pin is the output of LIN transceiver.
–	EP	Exposed Pad	Exposed Pad	The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Sense Current					mA
Threshold	I_{HSCT}	6.9	8.8	11	
Hysteresis	I_{HSCH}	–	0.88	–	
Output Current Limitation	I_{HL}	–	90	–	mA
Over-current Warning HP_OCF Flag Threshold]	V_{HPOCT}	–	3.0	–	V
Dropout Voltage @ I_{LOAD} = 15 mA	V_{HPDO}	–	0.5	–	V
ANALOG INPUT (PA1)					
Current Source PA1					µA
CSSEL1 = 1, CSSEL0 = 1	I_{CSPA1}	570	670	770	
Selectable Scaling Factor Current Source PA1 (I(N) = I_{CSPA1}* N)					%
CSSEL1 = 0, CSSEL0 = 0	$N_{CSPA1-0}$	8.5	10	11.5	
CSSEL1 = 0, CSSEL0 = 1	$N_{CSPA1-1}$	28.5	30	31.5	
CSSEL1 = 1, CSSEL0 = 0	$N_{CSPA1-2}$	58.5	60	61.5	

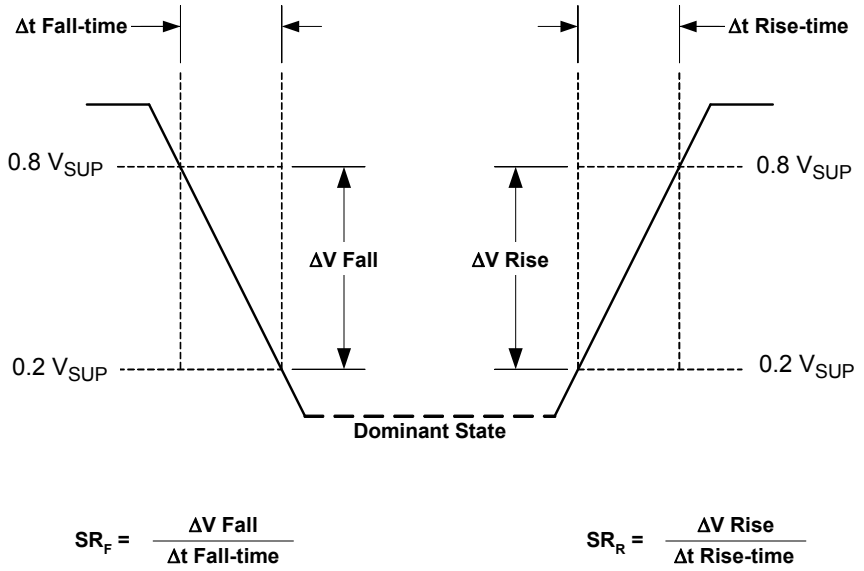

Figure 5. LIN Slew Rate Description

ELECTRICAL PERFORMANCE CURVES

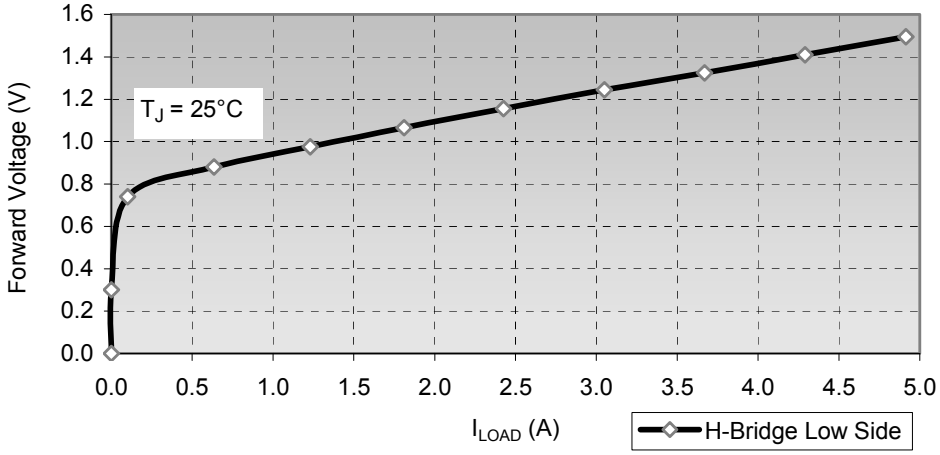

Figure 6. Free Wheel Diode Forward Voltage vs. I_{LOAD}

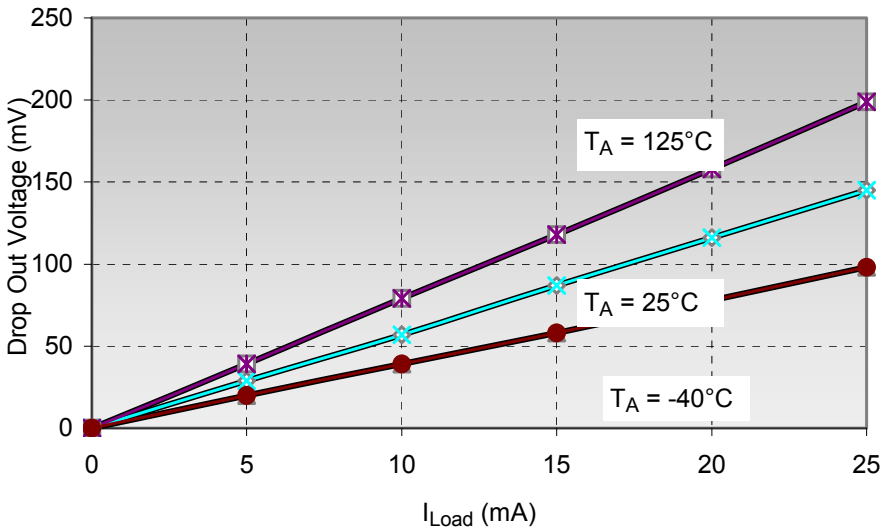

Figure 7. Dropout Voltage on HVDD vs. I_{LOAD}

real PWM input pin; it should just supply the period of the PWM. The duty cycle will be generate automatically.

Important The recommended FGEN frequency should be in the range of 0.1 kHz to 20 kHz.

BACK ELECTROMAGNETIC FORCE OUTPUT PIN (BEMF)

This pin gives the user information about back electromagnetic force (BEMF). This feature is mainly used in step motor applications for detecting a stalled motor. In order to evaluate this signal the pin must be directly connected to pin PTD0/TACH0/BEMF.

RESET PIN ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the bi-directional reset pin of the analog die. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{RST}}$ pin of the MCU.

INTERRUPT PIN ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output pin of the analog die indicating errors or wake-up events. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{IRQ}}$ pin of the MCU.

SLAVE SELECT PIN ($\overline{\text{SS}}$)

This pin is the SPI Slave Select pin for the analog chip. All other SPI connections are done internally. $\overline{\text{SS}}$ must be connected to PTB1 or any other logic I/O of the microcontroller.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

HALF-BRIDGE OUTPUT PINS (HB1:HB4)

The 908E625 device includes power MOSFETs configured as four half-bridge driver outputs. The HB1:HB4 outputs may be configured for step motor drivers, DC motor drivers, or as high side and low-side switches.

The HB1:HB4 outputs are short-circuit and over-temperature protected, and they feature current recopy, current limitation, and BEMF generation. Current limitation and recopy are done on the low side MOSFETs.

POWER SUPPLY PINS (VSUP1:VSUP3)

VSUP1:VSUP3 are device power supply pins. The nominal input voltage is designed for operation from 12 V systems. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high side output driver, multiple VSUP pins are provided.

All VSUP pins must be connected to get full chip functionality.

POWER GROUND PINS (GND1 AND GND2)

GND1 and GND2 are device power ground connections. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high side output driver, multiple pins are provided.

GND1 and GND2 pins must be connected to get full chip functionality.

HIGH SIDE OUTPUT PIN (HS)

The HS output pin is a low $R_{DS(ON)}$ high side switch. The switch is protected against over-temperature and over-current. The output is capable of limiting the inrush current with an automatic PWM generation using the FGEN module.

SWITCHABLE VDD OUTPUT PIN (HVDD)

The HVDD pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; e.g., 3-pin Hall-effect sensors. The output is short-circuit protected.

HALL-EFFECT SENSOR INPUT PINS (H1:H3)

The Hall-effect sensor input pins H1:H3 provide inputs for Hall-effect sensors and switches.

+5.0 V VOLTAGE REGULATOR OUTPUT PIN (VDD)

The VDD pin is needed to place an external capacitor to stabilize the regulated output voltage. The VDD pin is intended to supply the embedded microcontroller.

Important The VDD pin should not be used to supply other loads; use the HVDD pin for this purpose. The VDD, EVDD, VDDA, and VREFH pins must be connected together.

ANALOG INPUT PIN (PA1)

This pin is an analog input port with selectable current source values.

VOLTAGE REGULATOR GROUND PIN (VSS)

The VSS pin is the ground pin for the connection of all non-power ground connections (microcontroller and sensors).

Important VSS, EVSS, VSSA, and VREFL pins must be connected together.

LIN TRANSCEIVER OUTPUT PIN (RXD)

This pin is the output of LIN transceiver. The pin must be connected to the microcontroller's Enhanced Serial Communications Interface (ESCI) module (RXD pin).

ADC REFERENCE PINS (VREFL AND VREFH)

VREFL and VREFH are the reference voltage pins for the ADC. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VREFH is the high reference supply for the ADC and should be tied to the same potential as VDDA via separate traces. VREFL is the low reference supply for the

ADC and should be tied to the same potential as VSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

ADC SUPPLY PINS (VDDA AND VSSA)

VDDA and VSSA are the power supply pins for the analog-to-digital converter (ADC). It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VDDA is the supply for the ADC and should be tied to the same potential as EVDD via separate traces. VSSA is the ground pin for the ADC and should be tied to the same potential as EVSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

MCU POWER SUPPLY PINS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details refer to the 68HC908EY16 datasheet.

TEST PIN (FLSVPP)

This pin is for test purposes only. This pin should be either left open (not connected) or connected to GND.

EXPOSED PAD PIN

The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board. For thermal performance the pad must be soldered to the PCB board. It is recommended that the pad be connected to the ground potential.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

INTERRUPTS

The 908E625 has seven different interrupt sources as described in the following paragraphs. The interrupts can be disabled or enabled via the SPI. After reset all interrupts are automatically disabled.

LOW VOLTAGE INTERRUPT

The low voltage interrupt (LVI) is related to the external supply voltage, V_{SUP}. If this voltage falls below the LVI threshold, it will set the LVI flag. If the low voltage interrupt is enabled, an interrupt will be initiated.

With LVI the H-Bridges (high side MOSFET only) and the high side driver are switched off. All other modules are not influenced by this interrupt.

During STOP mode the LVI circuitry is disabled.

HIGH VOLTAGE INTERRUPT

The high voltage interrupt (HVI) is related to the external supply voltage, V_{SUP}. If this voltage rises above the HVI threshold, it will set the HVI flag. If the high voltage interrupt is enabled, an interrupt will be initiated.

With HVI the H-Bridges (high side MOSFET only) and the high side driver are switched off. All other modules are not influenced by this interrupt.

During STOP mode the HVI circuitry is disabled.

HIGH TEMPERATURE INTERRUPT

The high temperature interrupt (HTI) is generated by the on-chip temperature sensors. If the chip temperature is above the HTI threshold, the HTI flag will be set. If the high temperature interrupt is enabled, an interrupt will be initiated.

During STOP mode the HTI circuitry is disabled.

AUTONOMOUS WATCHDOG INTERRUPT (AWD)

Refer to Autonomous Watchdog Autonomous Watchdog (AWD) on page 36.

LIN INTERRUPT

If the LINIE bit is set, a falling edge on the LIN pin will generate an interrupt. During STOP mode this interrupt will initiate a system wake-up.

HALL-EFFECT SENSOR INPUT PIN INTERRUPT

If the PHIE bit is set, the enabled Hall-effect sensor input pins H1:H3 can generate an interrupt if a current above the threshold is detected. During Stop mode this interrupt, combined with the cyclic wake-up feature of the AWD, can wake up the system. Refer to pin Hall-Effect Sensor Input Pins (H1:H3).

OVER-CURRENT INTERRUPT

If an over-current condition on a half-bridge occurs, the high side or the HVDD output is detected and the OCIE bit is set and an interrupt generated.

SYSTEM WAKE-UP

System wake-up can be initiated by any of four events:

- A falling edge on the LIN pin
- A wake-up signal from the AWD
- A Logic [1] at Hall-effect sensor input pin during cyclic check via AWD
- An LVR condition

If one of these wake-up events occurs and the interrupt mask bit for this event is set, the interrupt will wake-up the microcontroller as well as the main voltage regulator (MREG) (Figure 8).

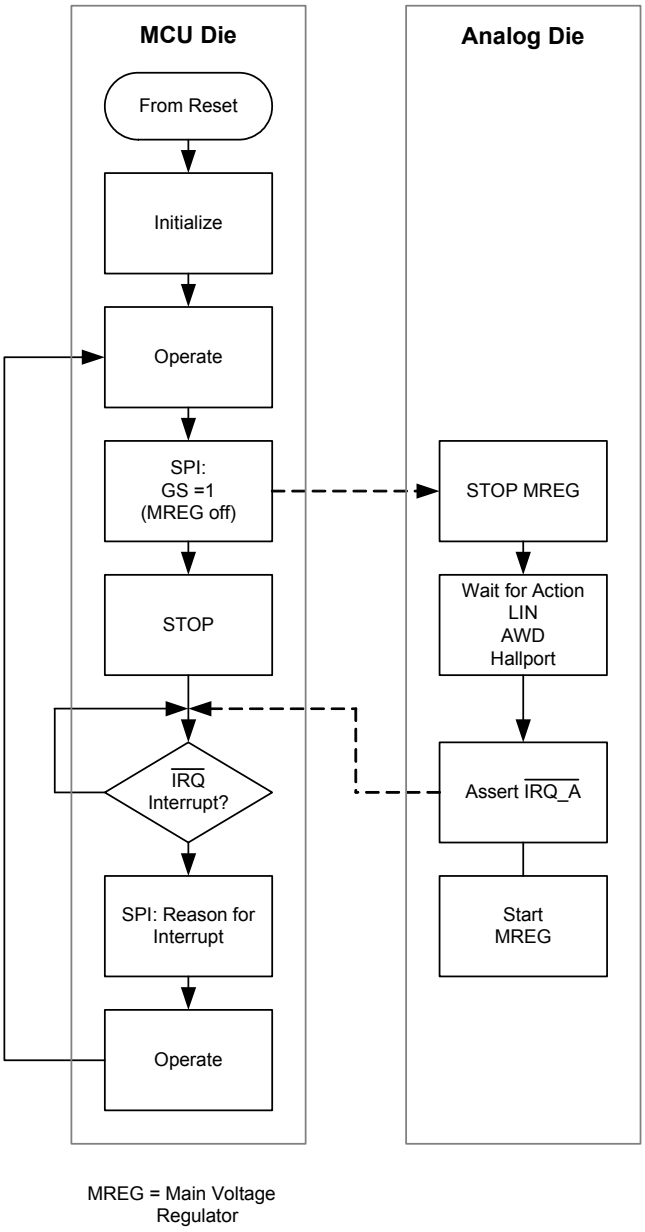

Figure 8. STOP Mode/Wake-up Procedure

SERIAL SPI INTERFACE

The SPI creates the communication link between the microcontroller and the 908E625. The interface consists of four pins. See Figure 9:

- $\overline{SS}$—Slave Select
- MOSI—Master-Out Slave-In
- MISO—Master-In Slave-Out
- SPSCK—Serial Clock

A complete data transfer via the SPI consists of 2 bytes. The master sends address and data, slave system status, and data of the selected address.

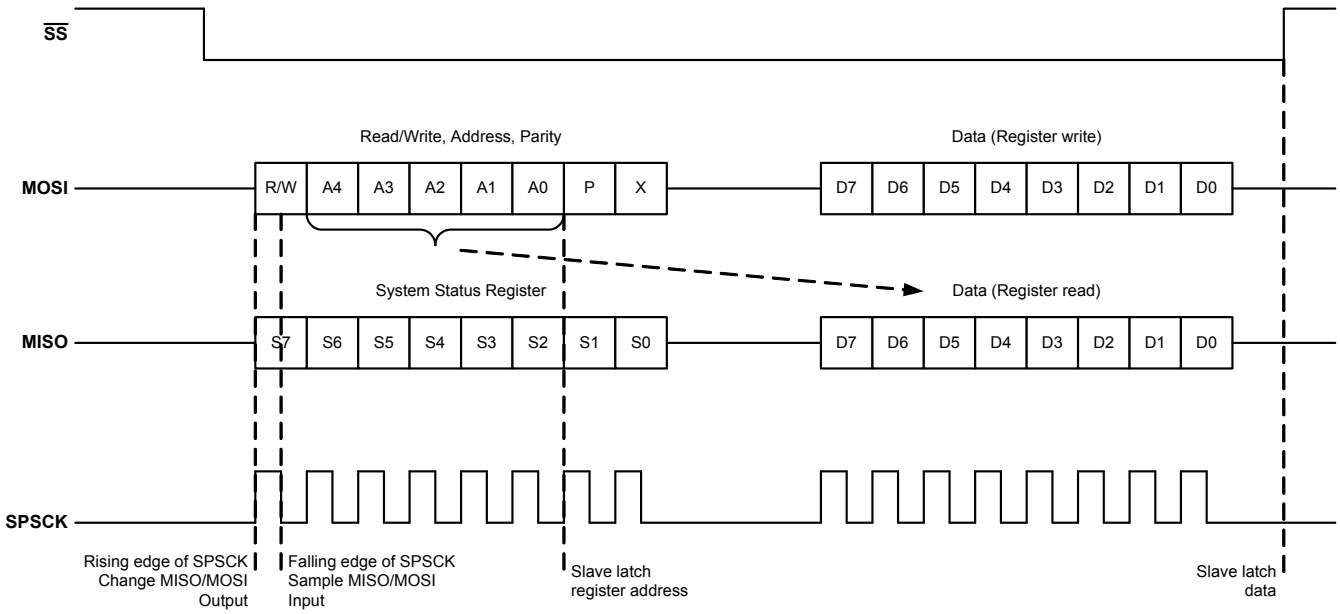

Figure 9. SPI Protocol

During the inactive phase of $\overline{SS}$, the new data transfer is prepared. The falling edge on the $\overline{SS}$ line indicates the start of a new data transfer and puts MISO in the low-impedance mode. The first valid data are moved to MISO with the rising edge of SPSCK.

The MISO output changes data on a rising edge of SPSCK. The MOSI input is sampled on a falling edge of SPSCK. The data transfer is only valid if exactly 16 sample clock edges are present in the active phase of $\overline{SS}$.

After a write operation, the transmitted data is latched into the register by the rising edge of $\overline{SS}$. Register read data is internally latched into the SPI at the time when the parity bit is transferred. $\overline{SS}$ HIGH forces MISO to high impedance.

A4:A0

Contains the address of the desired register.

R/$\overline{W}$

Contains information about a read or a write operation.

- If R/$\overline{W}$ = 1, the second byte of master contains no valid information, slave just transmits back register data.
- If R/$\overline{W}$ = 0, the master sends data to be written in the second byte, slave sends concurrently contents of selected register prior to write operation, write data is latched in the *SMARTMOS* register on rising edge of $\overline{SS}$.

PARITY P

The parity bit is equal to 0 if the number of 1 bits is an even number contained within R/$\overline{W}$, A4:A0. If the number of 1 bits is odd, P equals 1. For example, if R/$\overline{W}$ = 1, A4:A0 = 00001, then P equals 0.

The parity bit is only evaluated during a write operation.

BIT X

Not used.

MASTER DATA BYTE

Contains data to be written or no valid data during a read operation.

SLAVE STATUS BYTE

Contains the contents of the System Status Register ($0c) independent of whether it is a write or read operation or which register was selected.

SLAVE DATA BYTE

Contains the contents of selected register. During a write operation it includes the register content prior to a write operation.

SPI REGISTER OVERVIEW

Table 6 summarizes the SPI register addresses and the bit names of each register.

Table 6. List of Registers

Addr	Register Name	R/W	Bit							
			7	6	5	4	3	2	1	0
$01	H-Bridge Output (HBOUT)	R	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
		W								
$02	H-Bridge Control (HBCTL)	R	OFC_EN	CSA	0	0	0	CLS2	CLS1	CLS0
		W								
$03	System Control (SYSCTL)	R	PSON	SRS1	SRS0	0	0	0	0	0
		W								GS
$04	Interrupt Mask (IMR)	R	0	HPIE	LINIE	HTIE	LVIE	HVIE	OCIE	0
		W								
$05	Interrupt Flag (IFR)	R	0	HPF	LINF	HTF	LVF	HVF	OCF	0
		W								
$06	Reset Mask (RMR)	R	TTEST	0	0	0	0	0	HVRE	HTRE
		W								
$07	Analog Multiplexer Configuration (ADMUX)	R	0	0	0	0	SS3	SS2	SS1	SS0
		W								
$08	Hall-Effect Sensor Input Pin Control (HACTL)	R	0	0	0	0	0	H3EN	H2EN	H1EN
		W								
$09	Hall-Effect Sensor Input Pin Status (HASTAT)	R	0	0	0	0	0	H3F	H2F	H1F
		W								
$0a	AWD Control (AWDCTL)	R	0	0	0	AWDRE	AWDIE	AWDCC	AWDF	AWDR
		W			AWDRST					
$0b	Power Output (POUT)	R	0	0	CSSEL1	CSSEL0	CSEN1	CSEN0	HVDDON	HS_ON
		W								
$0c	System Status (SYSSTAT)	R	HP_OCF	LINCL	HVDD_OCF	HS_OCF	LVF	HVF	HB_OCF	HTF
		W								

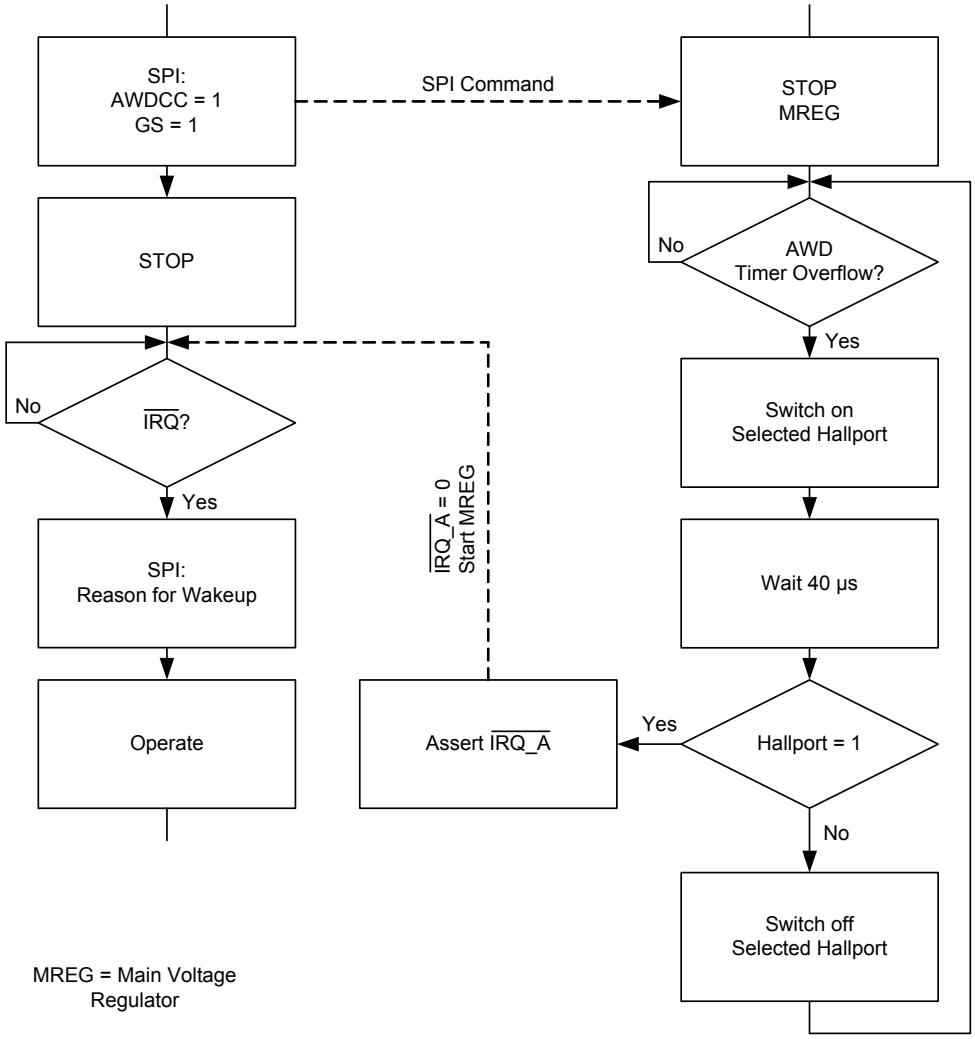

Figure 16. Hall-effect Sensor Input Pin Cyclic Check Wake-up Feature

HALL-EFFECT SENSOR INPUT PIN CONTROL REGISTER (HACTL)

Register Name and Address: HACTL - $08

Bits	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	H3EN	H2EN	H1EN
Write								
Reset	0	0	0	0	0	0	0	0

Hall-Effect Sensor Input Pin Enable Bits (H3EN:H1EN)

These read/write bits enable the Hall-effect sensor input pins. Reset clears the H3EN:H1EN bits.

- 1 = Hall-effect sensor input pin Hx switched on and sensed
- 0 = Hall-effect sensor input pin Hx disabled

HALL-EFFECT SENSOR INPUT PIN STATUS REGISTER (HASTAT)

Register Name and Address: HASTAT - $09

Bits	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	H3F	H2F	H1F
Write								
Reset	0	0	0	0	0	0	0	0

Hall-Effect Sensor Input Pin Flag Bits (H3F:H1F)

These read-only flag bits reflect the input Hx while the Hall-effect sensor input pin Hx is enabled (HxEN = 1). Reset clears the H3F:H1F bits.

- 1 = Hall-effect sensor input pin current above threshold
- 0 = Hall-effect sensor input pin current below threshold

STOP Mode

During STOP mode the STOP mode regulator supplies a regulated output voltage. The STOP mode regulator has a very limited output current capability. The output voltage will be lower than the output voltage of the main voltage regulator.

FACTORY TRIMMING AND CALIBRATION

To enhance the ease-of-use of the 908E625, various parameters (e.g. ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the *empty* (0xFF) state:

- 0xFD80:0xFDDF Trim and Calibration Values
- 0xFFFE:0xFFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

Trim Values

Below the usage of the trim values located in the flash memory is explained

Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller without using any external components. The untrimmed frequency of the low frequency base clock (IBASE), will vary as much as ±25 percent due to process, temperature, and voltage dependencies. To compensate this dependencies a ICG trim values is located at address $FDC2. After trimming the ICG is a range of typ. ±2% (±3% max.) at nominal conditions (filtered (100 nF) and stabilized (4,7 µF) V_{DD} = 5.0 V, $T_{AMBIENT}$~25 °C) and will vary over temperature and voltage (V_{DD}) as indicated in the 68HC908EY16 datasheet.

To trim the ICG this values has to be copied to the ICG Trim Register ICGTR at address $38 of the MCU.

Important The value has to copied after every reset.

TYPICAL APPLICATIONS

DEVELOPMENT SUPPORT

As the 908E625 has the MC68HC908EY16 MCU embedded typically all the development tools available for the MCU also apply for this device, however due to the fact of the additional analog die circuitry and the nominal +12 V supply voltage some additional items have to be considered:

- nominal 12 V rather than 5.0 V or 3.0 V supply
- high voltage V_{TST} might be applied not only to $\overline{IRQ}$ pin, but $\overline{IRQ\_A}$ pin

For a detailed information on the MCU related development support see the MC68HC908EY16 datasheet - section development support.

The programming is principally possible at two stages in the manufacturing process - first on chip level, before the IC is soldered onto a pcb board and second after the IC is soldered onto the pcb board.

Chip level programming

On Chip level the easiest way is to only power the MCU with +5.0 V (see Figure 23) and not to provide the analog chip with VSUP, in this setup all the analog pin should be left open (e.g. VSUP[1:3]) and interconnections between MCU and analog die have to be separated (e.g. $\overline{IRQ}$ - $\overline{IRQ\_A}$).

This mode is well described in the MC68HC908EY16 datasheet - section development support.

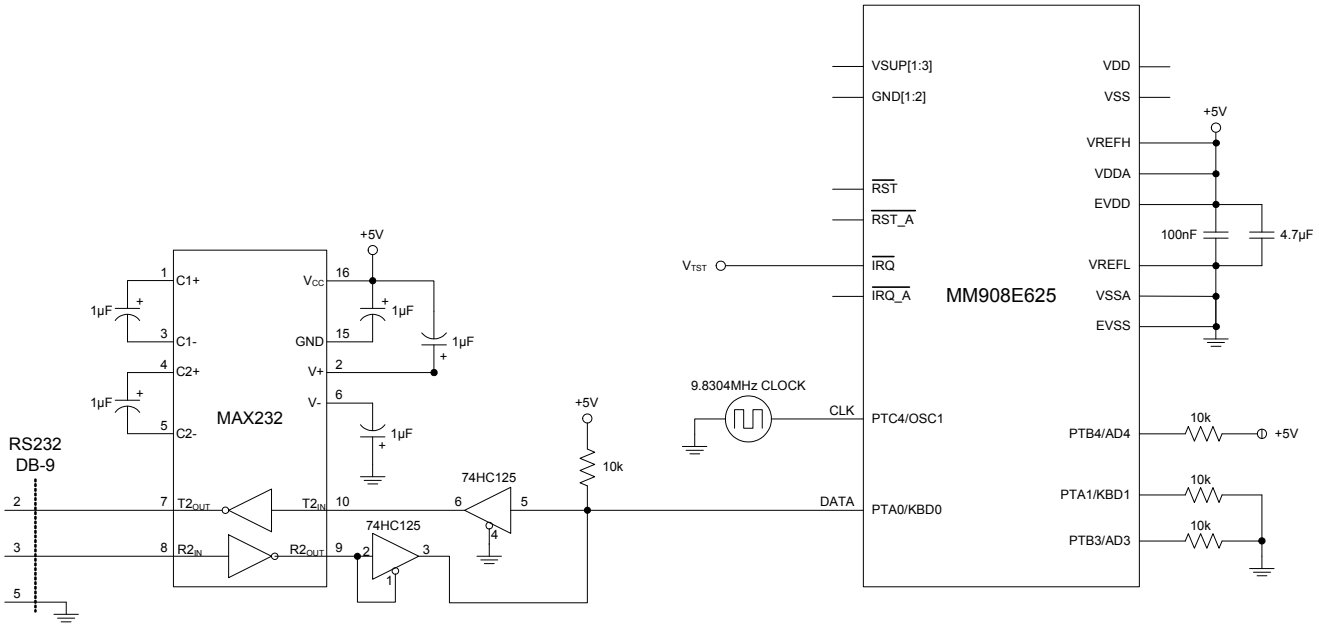

Figure 23. Normal Monitor Mode Circuit (MCU only)

Of course its also possible to supply the whole system with Vsup (12 V) instead as described in Figure 24, page 40.

PCB level programming

If the IC is soldered onto the pcb board its typically not possible to separately power the MCU with +5.0 V, the whole system has to be powered up providing V_{SUP} (see Figure 24).

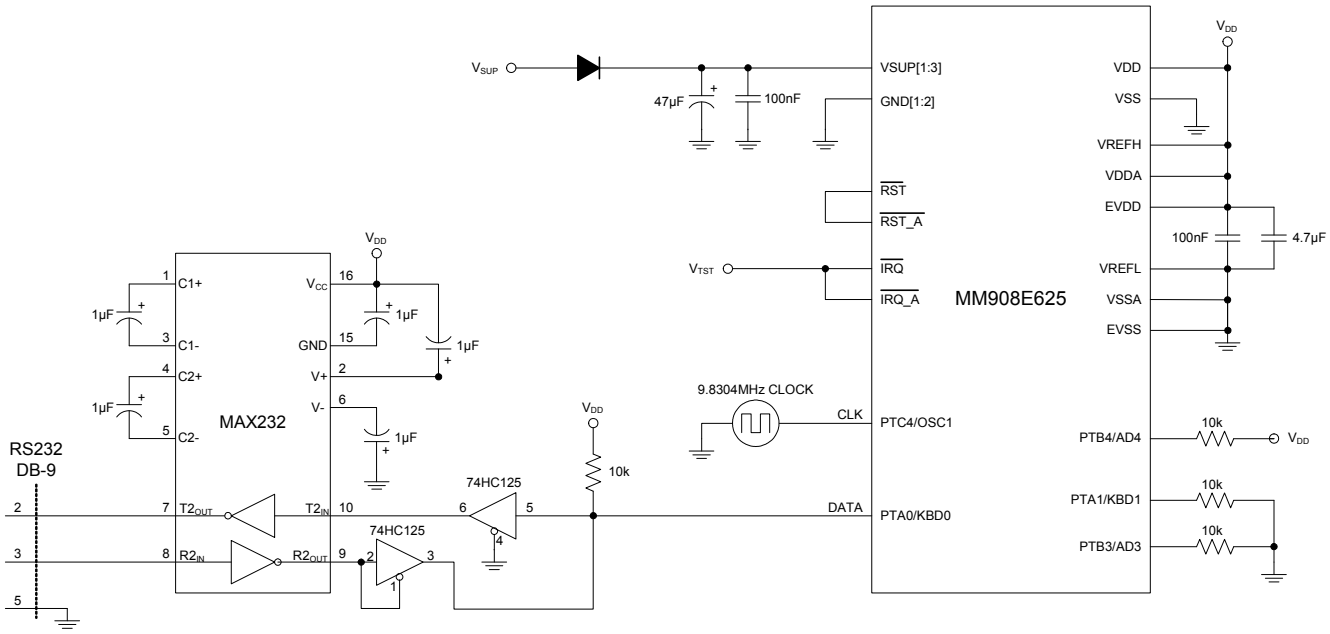

Figure 24. Normal Monitor Mode Circuit

Table 12 summarizes the possible configurations and the necessary setups.

Table 12. Monitor Mode Signal Requirements and Options

Mode	IRQ	RST	Reset Vector	Serial Communication		Mode Selection		ICG	COP	Normal Request Timeout	Communication Speed		
				PTA0	PTA1	PTB3	PTB4				External Clock	Bus Frequency	Baud Rate
Normal Monitor	V_{TST}	V_{DD}	X	1	0	0	1	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
Forced Monitor	V_{DD}	V_{DD}	$FFFF (blank)	1	0	X	X	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
	GND							ON	disabled	disabled	—	Nominal 1.6MHz	Nominal 6300
User	V_{DD}	V_{DD}	not $FFFF (not blank)	X	X	X	X	ON	enabled	enabled	—	Nominal 1.6MHz	Nominal 6300

Notes

1. PTA0 must have a pull-up resistor to V_{DD} in monitor mode
2. External clock is a 4.9152 MHz, 9.8304 MHz or 19.6608 MHz canned oscillator on OCS1
3. Communication speed with external clock is depending on external clock value. Baud rate is bus frequency / 256
4. X = don't care
5. V_{TST} is a high voltage $V_{DD} + 3.5\ V \leq V_{TST} \leq V_{DD} + 4.5\ V$

EMC/EMI RECOMMENDATIONS

This paragraph gives some device specific recommendations to improve EMC/EMI performance. Further generic design recommendations can be e.g. found on the Freescale web site www.freescale.com.

VSUP pins (VSUP1:VSUP3)

Its recommended to place a high-quality ceramic decoupling capacitor close to the VSUP pins to improve EMC/EMI behavior.

LIN pin

For DPI (Direct Power Injection) and ESD (Electro Static Discharge) its recommended to place a high quality ceramic decoupling capacitor near the LIN pin. An additional varistor will further increase the immunity against ESD. A ferrite in the LIN line will suppress some of the noise induced.

Voltage regulator output pins (VDD and AGND)

Use a high quality ceramic decoupling capacitor to stabilize the regulated voltage.

MCU digital supply pins (EVDD and EVSS)

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

MCU analog supply pins (VREFH, VDDA and VREFL, VSSA)

To avoid noise on the analog supply pins its important to take special care on the layout. The MCU digital and analog supplies should be tied to the same potential via separate traces and connected to the voltage regulator output.

Figure 25 and Figure 26 show the recommendations on schematics and layout level and Table 13 indicates recommended external components and layout considerations.

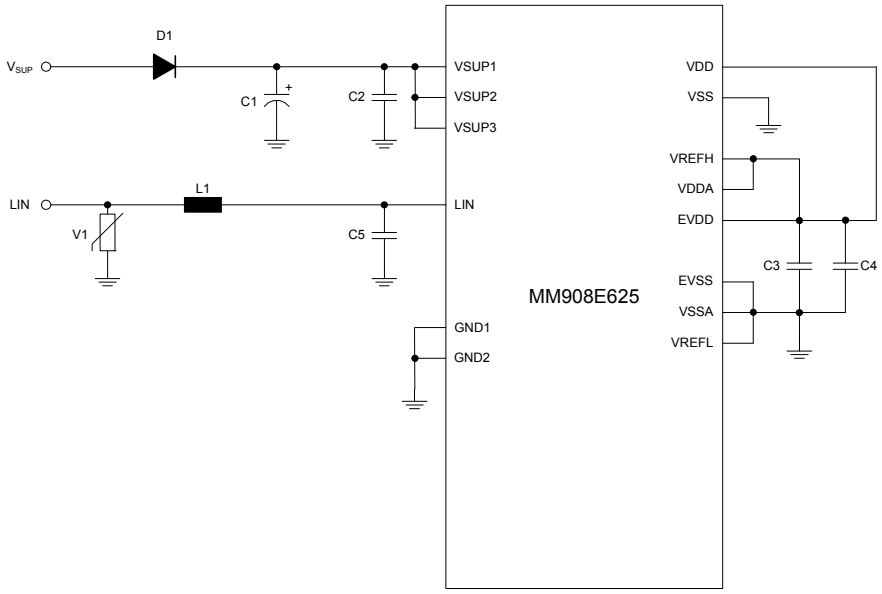

Figure 25. EMC/EMI Recommendations

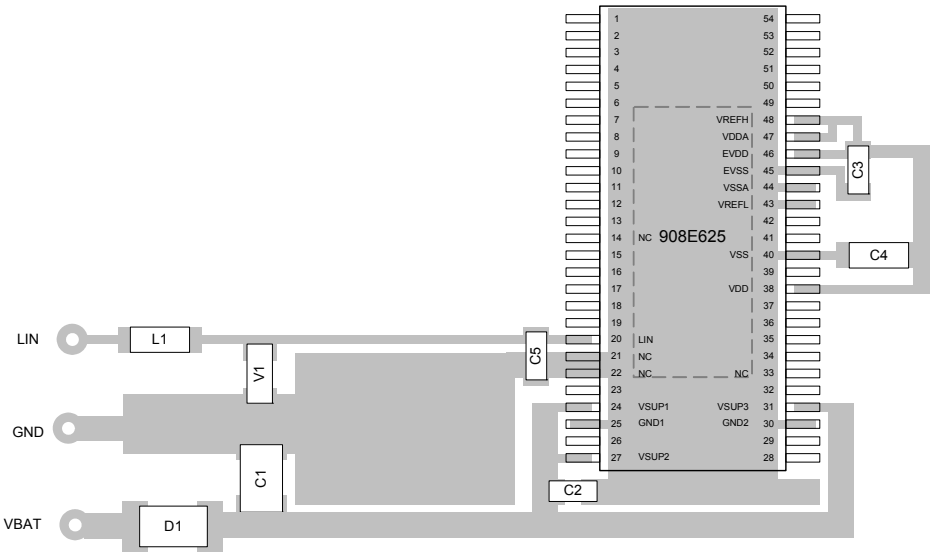

Figure 26. PCB Layout Recommendations

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Table 13. Component Value Recommendation

Component	Recommended Value[1]	Comments / Signal routing
D1		reverse battery protection
C1	Bulk Capacitor	
C2	100nF, SMD Ceramic, Low ESR	Close (<5mm) to VSUP1, VSUP2 pins with good ground return
C3	100nF, SMD Ceramic, Low ESR	Close (<3mm) to digital supply pins (EVDD, EVSS) with good ground return. The positive analog (VREFH, VDDA) and the digital (EVDD) supply should be connected right at the C3.
C4	4,7uF, SMD Ceramic, Low ESR	Bulk Capacitor
C5	180pF, SMD Ceramic, Low ESR	Close (<5.0 mm) to LIN pin. Total Capacitance on LIN has to be below 220 pF. (C_{total} = $C_{LIN-Pin}$ + C5 + $C_{Varistor}$ ~ 10 pF + 180 pF + 15 pF)
V1[2]	Varistor Type TDK AVR-M1608C270MBAAB	Optional (close to LIN connector)
L1[2]	SMD Ferrite Bead Type TDK MMZ2012Y202B	Optional, (close to LIN connector)

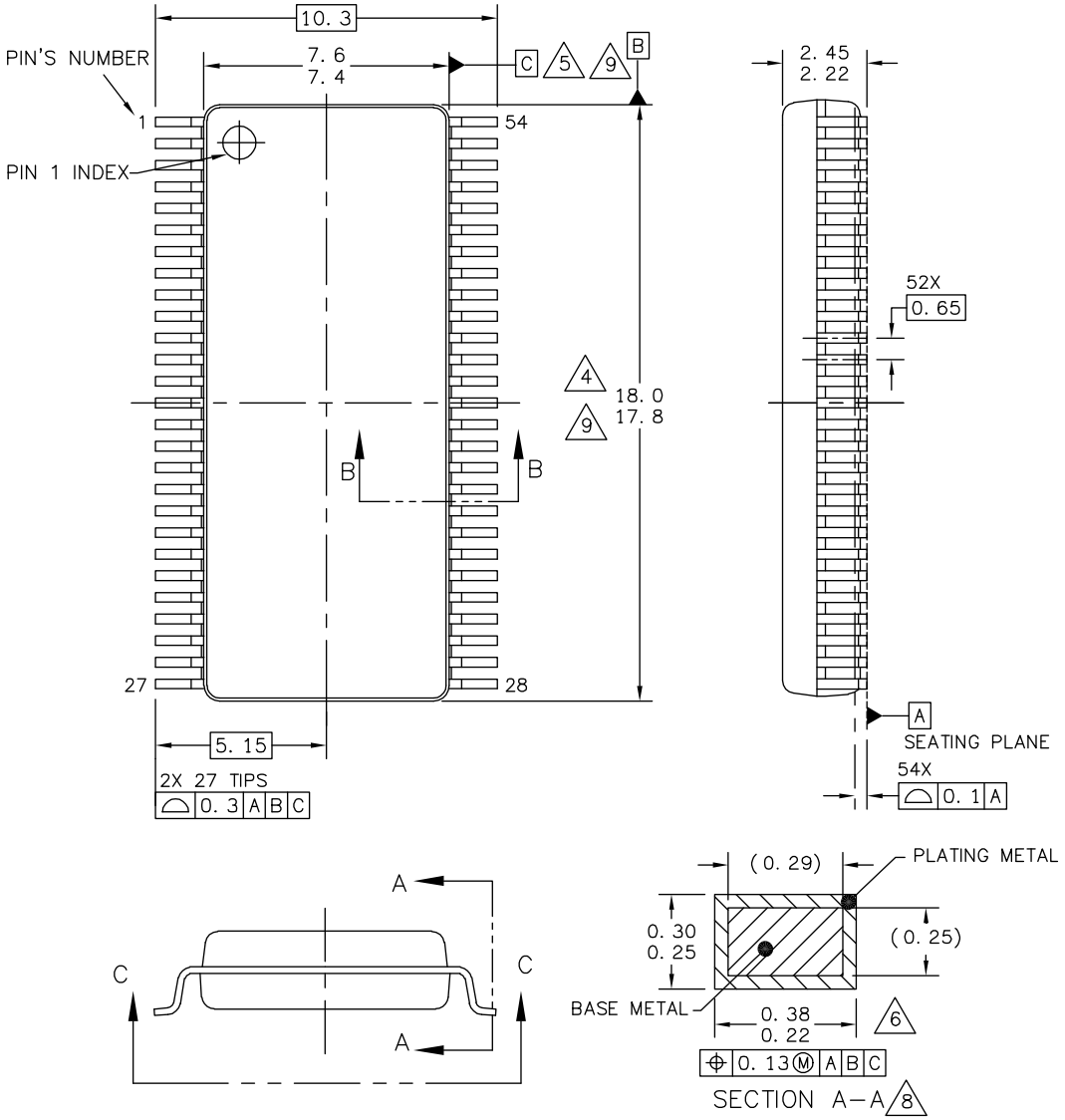
Notes

1. Freescale does not assume liability, endorse, or want components from external manufactures that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
2. Components are recommended to improve EMC and ESD performance.

PACKAGING

PACKAGING DIMENSIONS

Important: For the most current revision of the package, visit www.freescale.com and do a keyword search on the 98ARL10519D drawing number below. Dimensions shown are provided for reference ONLY.



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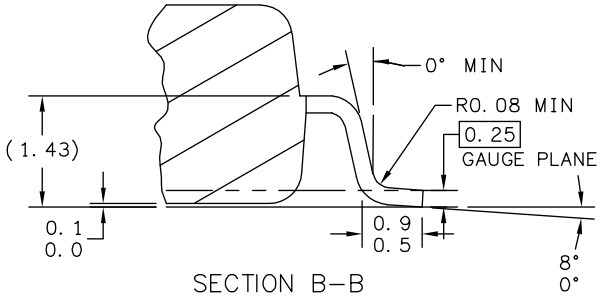
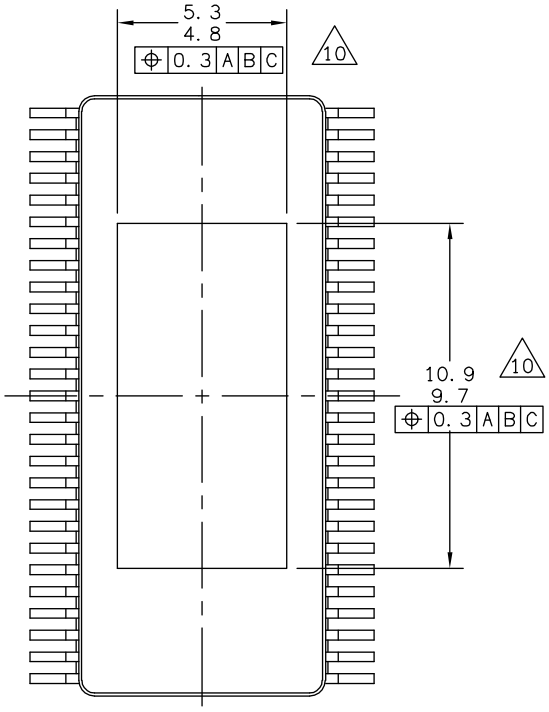
TITLE: 54LD SOIC W/B, 0.65 PITCH 5.1 X 10.3 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ARL10519D	REV: D
	CASE NUMBER: 1400–03	02 MAY 2008
	STANDARD: NON–JEDEC	

EK SUFFIX (PB-FREE)
54-PIN
98ARL10519D
ISSUE D

908E625



SECTION B–B



VIEW C–C

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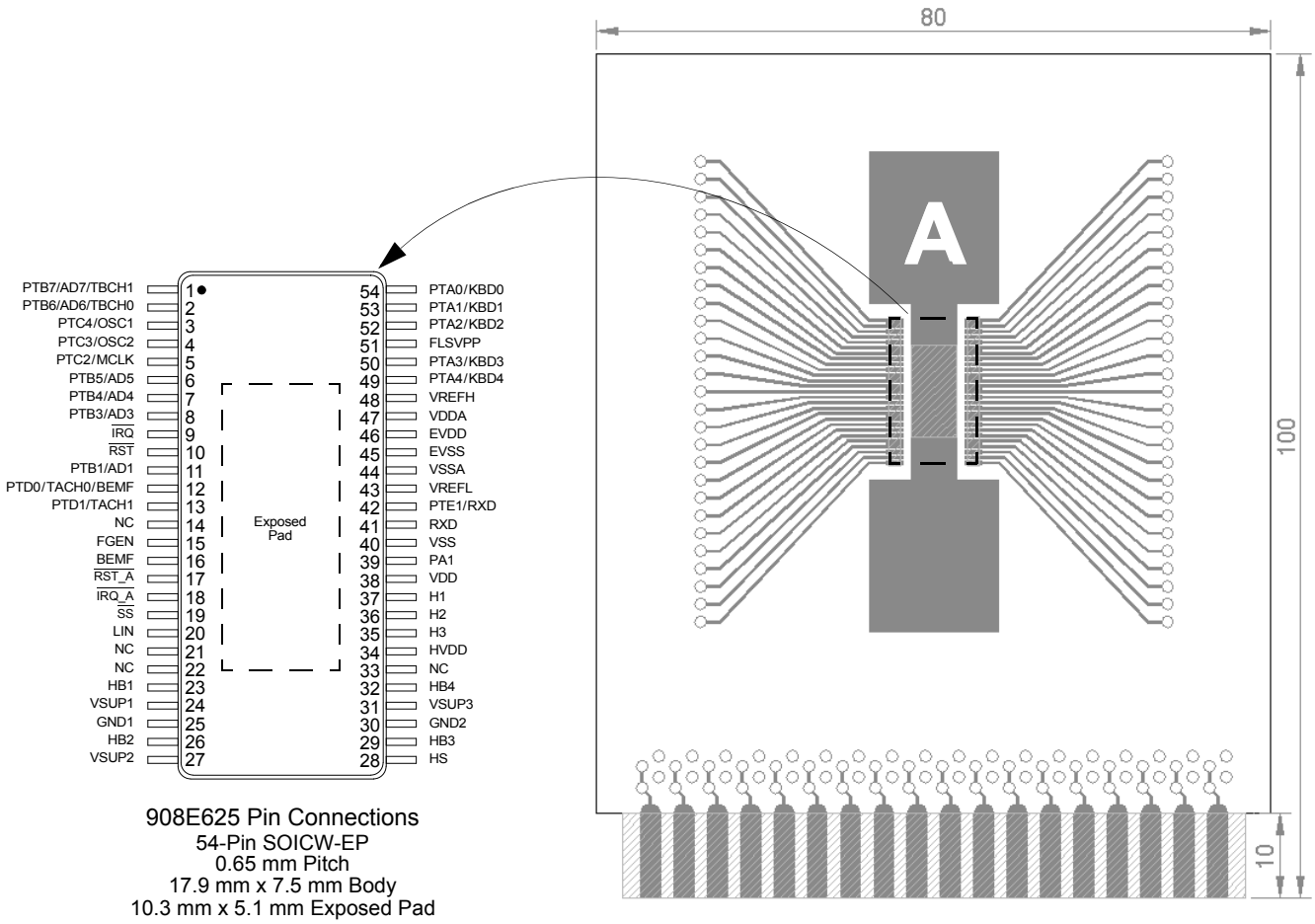
TITLE: 54LD SOIC W/B, 0.65 PITCH 5.1 X 10.3 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ARL10519D	REV: D
	CASE NUMBER: 1400–03	02 MAY 2008
	STANDARD: NON–JEDEC	

EK SUFFIX (PB-FREE)
54-PIN
98ARL10519D
ISSUE D



908E625 Pin Connections
54-Pin SOICW-EP
0.65 mm Pitch
17.9 mm x 7.5 mm Body
10.3 mm x 5.1 mm Exposed Pad

Figure 27. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area **A**:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 14. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		m = 1, *n* = 1	*m* = 1, *n* = 2 *m* = 2, *n* = 1	*m* = 2, *n* = 2
$R_{\theta JAmn}$	0	53	48	53
	300	39	34	38
	600	35	30	34
$R_{\theta JSmn}$	0	21	16	20
	300	15	11	15
	600	14	9.0	13

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

$R_{\theta JSmn}$ is the thermal resistance between die junction and the reference location on the board surface near a center lead of the package.

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.