Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	13
Voltage - Supply	8V ~ 18V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	54-SSOP (0.295", 7.50mm Width) Exposed Pad
Supplier Device Package	54-SOIC-EP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e625acek

INTERNAL BLOCK DIAGRAM

Figure 2. 908E625 Simplified Internal Block Diagram

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage Analog Chip Supply Voltage under Normal Operation, Steady State Analog Chip Supply Voltage under Transient Conditions (1) Microcontroller Chip Supply Voltage	 $V_{SUP(SS)}$ $V_{SUP(PK)}$ V_{DD}	 -0.3 to 28 -0.3 to 40 -0.3 to 6.0	V
Input Pin Voltage Analog Chip Microcontroller Chip	 $V_{IN(ANALOG)}$ $V_{IN(MCU)}$	 -0.3 to 5.5 V_{SS}-0.3 to V_{DD}+0.3	V
Maximum Microcontroller Current per Pin All Pins Except VDD, VSS, PTA0:PTA6, PTC0:PTC1 Pins PTA0:PTA6, PTC0:PTC1	 $I_{PIN(1)}$ $I_{PIN(2)}$	 ±15 ±25	mA
Maximum Microcontroller V_{SS} Output Current	I_{MVSS}	100	mA
Maximum Microcontroller V_{DD} Input Current	I_{MVDD}	100	mA
LIN Supply Voltage Normal Operation (Steady-State) Transient Conditions (1)	 $V_{BUS(SS)}$ $V_{BUS(DYNAMIC)}$	 -18 to 28 40	V
ESD Voltage Human Body Model (HBM)(2) Machine Model (MM)(3) Charge Device Model (CDM)(4)	V_{ESD}	 ±3000 ±150 ±500	V
THERMAL RATINGS			
Storage Temperature	T_{STG}	-40 to 150	°C
Ambient Operating Temperature	T_A	-40 to 85	°C
Operating Case Temperature (5)	T_C	-40 to 85	°C
Operating Junction Temperature(6)	T_J	-40 to 125	°C
Peak Package Reflow Temperature During Reflow(7)(8)	T_{PPRT}	Note 8	°C

Notes

1. Transient capability for pulses with a time of t < 0.5 sec.
2. ESD voltage testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω)
3. ESD voltage testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω)
4. ESD voltage testing is performed in accordance with Charge Device Model, robotic (C_{ZAP} = 4.0 pF).
5. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.
6. The temperature of analog and MCU die is strongly linked via the package, but can differ in dynamic load conditions, usually because of higher power dissipation on the analog die. The analog die temperature must not exceed 150 °C under these conditions.
7. Pin soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
8. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN Receiver					V
Recessive	V_{IH}	0.6 V_{LIN}	–	V_{SUP}	
Dominant	V_{IL}	0.0	–	0.4 V_{LIN}	
Threshold	V_{ITH}	–	V_{SUP}/2	–	
Input Hysteresis	V_{IHY}	0.01 V_{SUP}	–	0.1 V_{SUP}	
LIN Wake-up Threshold	V_{WTH}	–	V_{SUP}/2	–	V
HIGH SIDE OUTPUT (HS)					
Switch ON Resistance @ T_J = 25 °C with I_{LOAD} = 1.0 A	$R_{DS(ON)HS}$	–	600	700	mΩ
High Side Over-current Shutdown	I_{HSOC}	3.9	–	7.0	A
HALF-BRIDGE OUTPUTS (HB1:HB4)					
Switch ON Resistance @ T_J = 25 °C with I_{LOAD} = 1.0 A					mΩ
High Side	$R_{DS(ON)HB\_HS}$	–	425	500	
Low Side	$R_{DS(ON)HB\_LS}$	–	400	500	
High Side Over-current Shutdown	I_{HBHSOC}	4.0	–	7.5	A
Low Side Over-current Shutdown	I_{HBLSOC}	2.8	–	7.5	A
Low Side Current Limitation @ T_J = 25°C					mA
Current Limit 1 (CLS2 = 0, CLS1 = 1, CLS0 = 1)	I_{CL1}	–	55	–	
Current Limit 2 (CLS2 = 1, CLS1 = 0, CLS0 = 0)	I_{CL2}	210	260	315	
Current Limit 3 (CLS2 = 1, CLS1 = 0, CLS0 = 1)	I_{CL3}	300	370	440	
Current Limit 4 (CLS2 = 1, CLS1 = 1, CLS0 = 0)	I_{CL4}	450	550	650	
Current Limit 5 (CLS2 = 1, CLS1 = 1, CLS0 = 1)	I_{CL5}	600	740	880	
Half-bridge Output High Threshold for BEMF Detection	V_{BEMFH}	–	-30	0	V
Half-bridge Output Low Threshold for BEMF Detection	V_{BEMFL}	–	-60	-5.0	mV
Hysteresis for BEMF Detection	V_{BEMFHY}	–	30	–	mV
Low Side Current-to-Voltage Ratio (V_{ADOUT} [V]/I_{HB} [A])					V/A
CSA = 1	$RATIO_H$	7.0	12.0	14.0	
CSA = 0	$RATIO_L$	1.0	2.0	3.0	
SWITCHABLE V_{DD} OUTPUT (PH.D.)					
Over-current Shutdown Threshold	$I_{HVDDOCT}$	24	30	40	mA
V_{SUP} DOWN-SCALER					
Voltage Ratio ($RATIO_{VSUP}$ = V_{SUP} /V_{ADOUT})	$RATIO_{VSUP}$	4.8	5.1	5.35	–
INTERNAL DIE TEMPERATURE SENSOR					
Voltage/Temperature Slope	S_{TTOV}	–	19	–	mV/°C
Output Voltage @ 25 °C	V_{T25}	1.7	2.1	2.5	V
HALL-EFFECT SENSOR INPUTS (H1:H3)					
Output Voltage					V
V_{SUP} < 16.2 V	V_{HALL1}	–	V_{SUP}-1.2	–	
V_{SUP} > 16.2 V	V_{HALL2}	–	–	15	

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

All characteristics are for the analog chip only. Please refer to the specification for 68HC908EY16 for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Propagation Delay (13), (14)					µs
TXD Low to LIN Low	$t_{TXD-LIN-low}$	–	–	6.0	
TXD High to LIN High	$t_{TXD-LIN-high}$	–	–	6.0	
LIN Low to RXD Low	$t_{LIN-RXD-low}$	–	4.0	8.0	
LIN High to RXD High	$t_{LIN-RXD-high}$	–	4.0	8.0	
TXD Symmetry	$t_{TXD-SYM}$	-2.0	–	2.0	
RXD Symmetry	$t_{RXD-SYM}$	-2.0	–	2.0	
Output Falling Edge Slew Rate (13), (15)	SR_F				V/µs
80% to 20%		-1.0	-2.0	-3.0	
Output Rising Edge Slew Rate (13), (15)	SR_R				V/µs
20% to 80%, R_{BUS} > 1.0 kΩ, C_{BUS} < 10 nF		1.0	2.0	3.0	
LIN Rise/Fall Slew Rate Symmetry (13), (15)	SR_S	-2.0	–	2.0	µs
HALL-EFFECT SENSOR INPUTS (H1:H3)					
Propagation Delay	t_{HPPD}	–	1.0	–	µs
AUTONOMOUS WATCHDOG (AWD)					
AWD Oscillator Period	t_{OSC}	–	40	–	µs
AWD Period Low = 512 t_{OSC}	t_{AWDPH}				ms
T_J < 25 °C		16	27	34	
T_J ≥ 25 °C		16	22	28	
AWD Period High = 256 t_{OSC}	t_{AWDPL}				ms
T_J < 25 °C		8.0	13.5	17	
T_J ≥ 25 °C		8.0	11	14	
AWD Cyclic Wake-up On Time	$t_{AWDHPON}$	–	90	–	µs

Notes

13. All LIN characteristics are for initial LIN slew rate selection (20 kBaud) (SRS0:SRS1= 00).
14. See Figure 2.
15. See Figure 3.

MICROCONTROLLER PARAMETRICS

Table 5. Microcontroller Description

For a detailed microcontroller description, refer to the MC68HC908EY16 data sheet.

Module	Description
Core	High Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz
Timer	Two 16-Bit Timers with Two Channels (TIM A and TIM B)
Flash	16 K Bytes
RAM	512 Bytes
ADC	10-Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud Rate Adjustment
ICG	Internal Clock Generation Module (25% Accuracy with Trim Capability to 2%)
BEMF Counter	Special Counter for *SMARTMOS*™ BEMF Output

TIMING DIAGRAMS

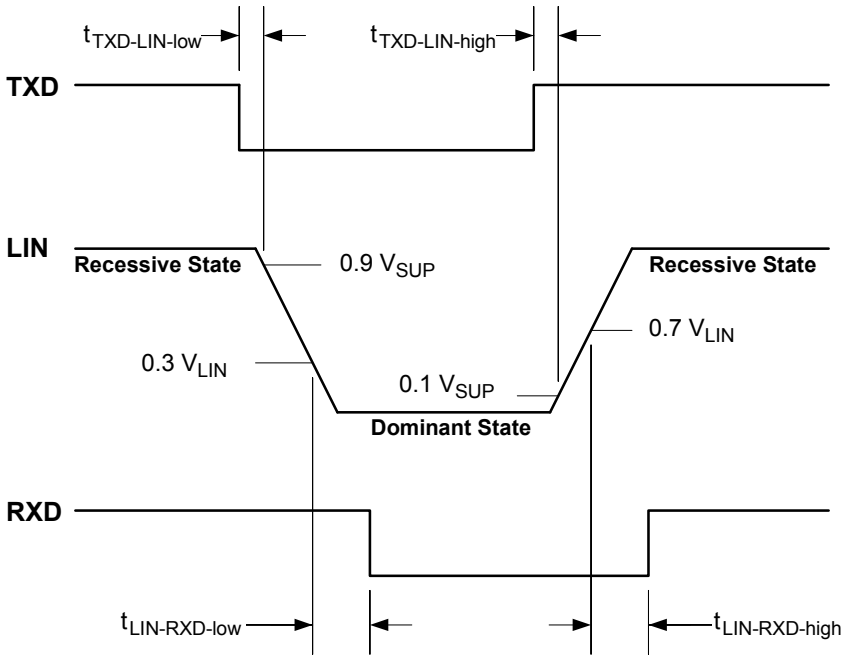


Figure 4. LIN Timing Description

real PWM input pin; it should just supply the period of the PWM. The duty cycle will be generate automatically.

Important The recommended FGEN frequency should be in the range of 0.1 kHz to 20 kHz.

BACK ELECTROMAGNETIC FORCE OUTPUT PIN (BEMF)

This pin gives the user information about back electromagnetic force (BEMF). This feature is mainly used in step motor applications for detecting a stalled motor. In order to evaluate this signal the pin must be directly connected to pin PTD0/TACH0/BEMF.

RESET PIN ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the bi-directional reset pin of the analog die. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{RST}}$ pin of the MCU.

INTERRUPT PIN ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output pin of the analog die indicating errors or wake-up events. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{IRQ}}$ pin of the MCU.

SLAVE SELECT PIN ($\overline{\text{SS}}$)

This pin is the SPI Slave Select pin for the analog chip. All other SPI connections are done internally. $\overline{\text{SS}}$ must be connected to PTB1 or any other logic I/O of the microcontroller.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

HALF-BRIDGE OUTPUT PINS (HB1:HB4)

The 908E625 device includes power MOSFETs configured as four half-bridge driver outputs. The HB1:HB4 outputs may be configured for step motor drivers, DC motor drivers, or as high side and low-side switches.

The HB1:HB4 outputs are short-circuit and over-temperature protected, and they feature current recopy, current limitation, and BEMF generation. Current limitation and recopy are done on the low side MOSFETs.

POWER SUPPLY PINS (VSUP1:VSUP3)

VSUP1:VSUP3 are device power supply pins. The nominal input voltage is designed for operation from 12 V systems. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high side output driver, multiple VSUP pins are provided.

All VSUP pins must be connected to get full chip functionality.

POWER GROUND PINS (GND1 AND GND2)

GND1 and GND2 are device power ground connections. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high side output driver, multiple pins are provided.

GND1 and GND2 pins must be connected to get full chip functionality.

HIGH SIDE OUTPUT PIN (HS)

The HS output pin is a low $R_{DS(ON)}$ high side switch. The switch is protected against over-temperature and over-current. The output is capable of limiting the inrush current with an automatic PWM generation using the FGEN module.

SWITCHABLE VDD OUTPUT PIN (HVDD)

The HVDD pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; e.g., 3-pin Hall-effect sensors. The output is short-circuit protected.

HALL-EFFECT SENSOR INPUT PINS (H1:H3)

The Hall-effect sensor input pins H1:H3 provide inputs for Hall-effect sensors and switches.

+5.0 V VOLTAGE REGULATOR OUTPUT PIN (VDD)

The VDD pin is needed to place an external capacitor to stabilize the regulated output voltage. The VDD pin is intended to supply the embedded microcontroller.

Important The VDD pin should not be used to supply other loads; use the HVDD pin for this purpose. The VDD, EVDD, VDDA, and VREFH pins must be connected together.

ANALOG INPUT PIN (PA1)

This pin is an analog input port with selectable current source values.

VOLTAGE REGULATOR GROUND PIN (VSS)

The VSS pin is the ground pin for the connection of all non-power ground connections (microcontroller and sensors).

Important VSS, EVSS, VSSA, and VREFL pins must be connected together.

LIN TRANSCEIVER OUTPUT PIN (RXD)

This pin is the output of LIN transceiver. The pin must be connected to the microcontroller's Enhanced Serial Communications Interface (ESCI) module (RXD pin).

ADC REFERENCE PINS (VREFL AND VREFH)

VREFL and VREFH are the reference voltage pins for the ADC. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VREFH is the high reference supply for the ADC and should be tied to the same potential as VDDA via separate traces. VREFL is the low reference supply for the

ADC and should be tied to the same potential as VSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

ADC SUPPLY PINS (VDDA AND VSSA)

VDDA and VSSA are the power supply pins for the analog-to-digital converter (ADC). It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VDDA is the supply for the ADC and should be tied to the same potential as EVDD via separate traces. VSSA is the ground pin for the ADC and should be tied to the same potential as EVSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

MCU POWER SUPPLY PINS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details refer to the 68HC908EY16 datasheet.

TEST PIN (FLSVPP)

This pin is for test purposes only. This pin should be either left open (not connected) or connected to GND.

EXPOSED PAD PIN

The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board. For thermal performance the pad must be soldered to the PCB board. It is recommended that the pad be connected to the ground potential.

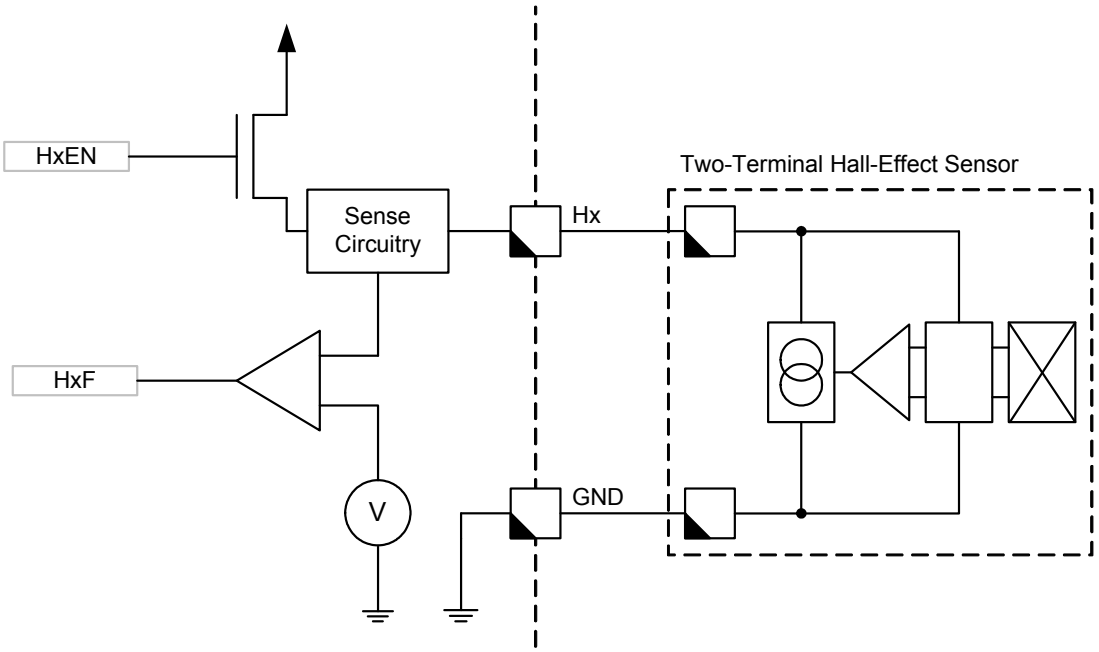


Figure 13. Hall-effect Sensor Input Pin Connected to Two Pin Hall-effect Sensor

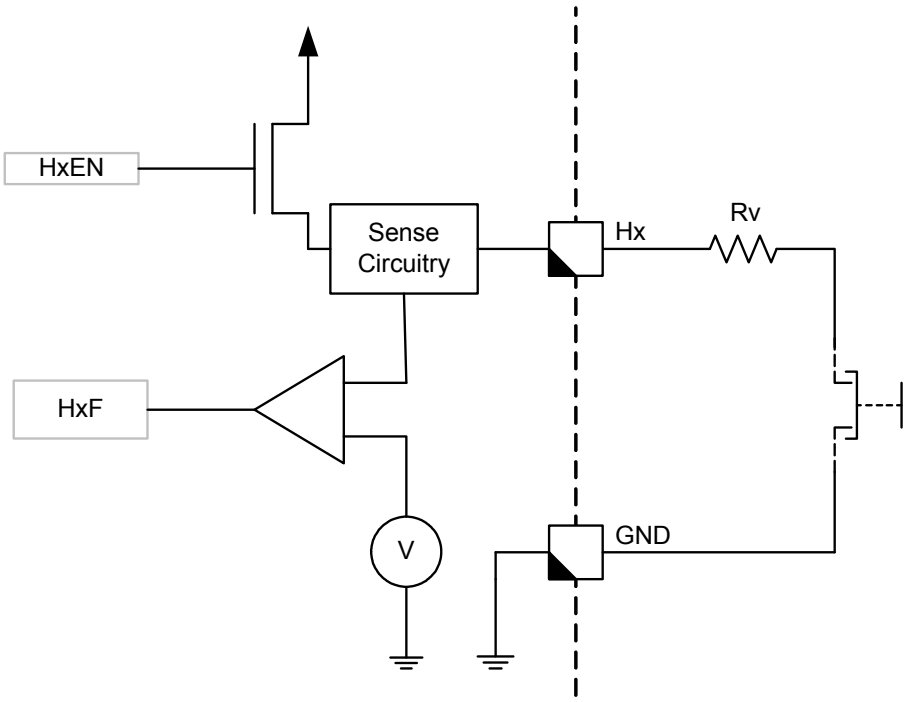


Figure 14. Hall-effect Sensor Input Pin Connected to Local Switch

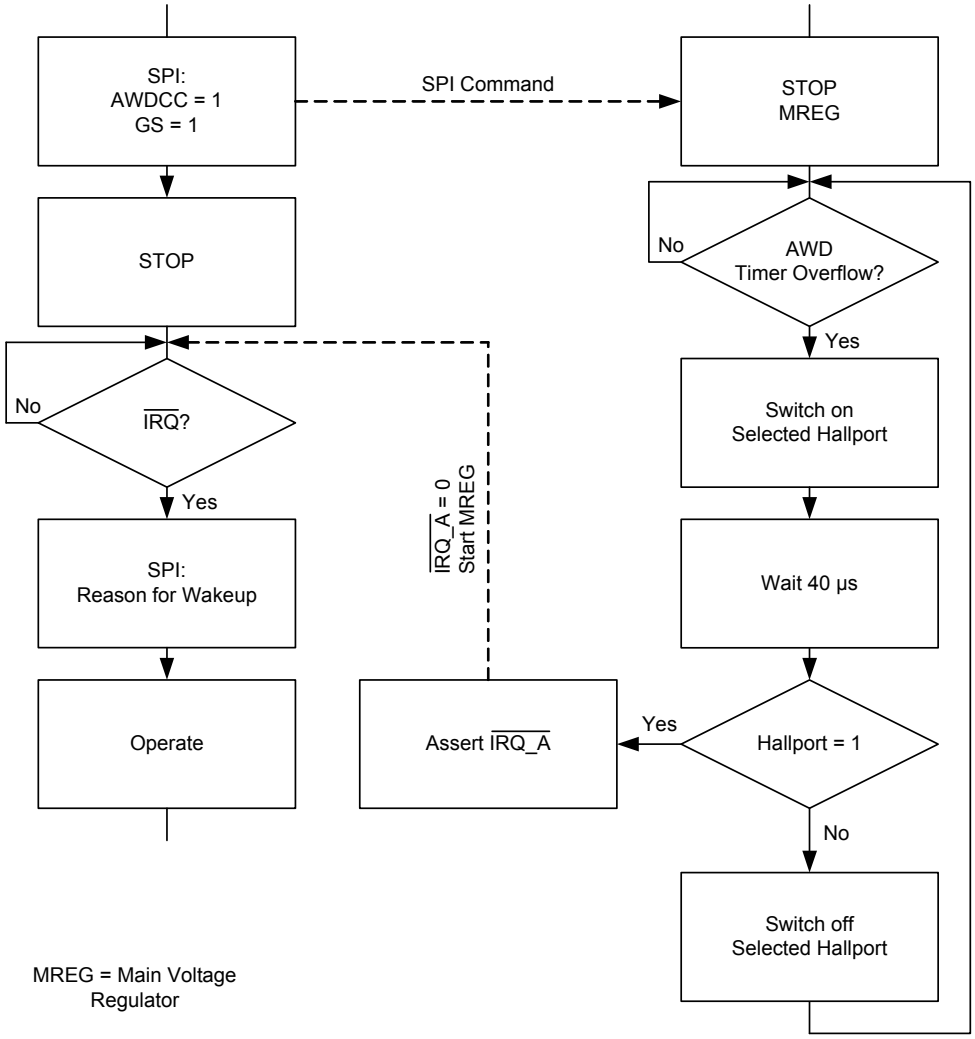


Figure 16. Hall-effect Sensor Input Pin Cyclic Check Wake-up Feature

HALL-EFFECT SENSOR INPUT PIN CONTROL REGISTER (HACTL)

Register Name and Address: HACTL - $08

Bits	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	H3EN	H2EN	H1EN
Write								
Reset	0	0	0	0	0	0	0	0

Hall-Effect Sensor Input Pin Enable Bits (H3EN:H1EN)

These read/write bits enable the Hall-effect sensor input pins. Reset clears the H3EN:H1EN bits.

- 1 = Hall-effect sensor input pin Hx switched on and sensed
- 0 = Hall-effect sensor input pin Hx disabled

HALL-EFFECT SENSOR INPUT PIN STATUS REGISTER (HASTAT)

Register Name and Address: HASTAT - $09

Bits	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	H3F	H2F	H1F
Write								
Reset	0	0	0	0	0	0	0	0

Hall-Effect Sensor Input Pin Flag Bits (H3F:H1F)

These read-only flag bits reflect the input Hx while the Hall-effect sensor input pin Hx is enabled (HxEN = 1). Reset clears the H3F:H1F bits.

- 1 = Hall-effect sensor input pin current above threshold
- 0 = Hall-effect sensor input pin current below threshold

HALF-BRIDGES

Outputs HB1:HB4 provide four low-resistive half-bridge output stages. The half-bridges can be used in H-Bridge, high side, or low side configurations.

Reset clears all bits in the H-Bridge output register (HBOUT) owing to the fact that all half-bridge outputs are switched off.

HB1:HB4 output features:

- Short-circuit (over-current) protection on high side and low side MOSFETs
- Current recopy feature (low side MOSFET)
- Over-temperature protection
- Over-voltage and under-voltage protection
- Current limitation feature (low side MOSFET)

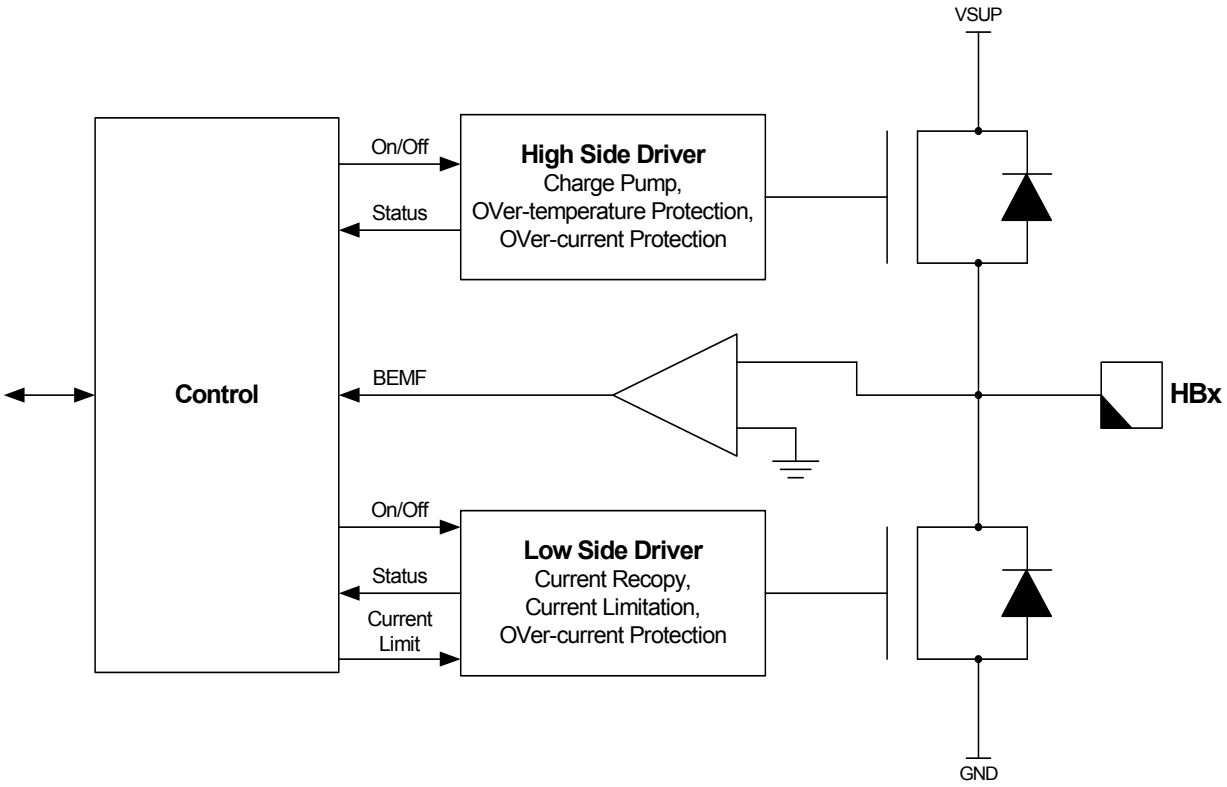


Figure 17. Half-bridge Push-Pull Output Driver

HALF-BRIDGE CONTROL

Each output MOSFET can be controlled individually. The general enable of the circuitry is done by setting PSON in the system control register (SYSCTL). HBx_L and HBx_H form one half-bridge. It is not possible to switch on both MOSFETs in one half-bridge at the same time. If both bits are set, the high-side MOSFET has a higher priority.

To avoid both MOSFETs (high side and low side) of one half-bridge being on at the same time, a break-before-make circuit exists. Switching the high side MOSFET on is inhibited as long as the potential between gate and V_{SS} is not below a certain threshold. Switching the low side MOSFET on is blocked as long as the potential between gate and source of the high-side MOSFET did not fall below a certain threshold.

HALF-BRIDGE OUTPUT REGISTER (HBOUT)

Register Name and Address: HBOUT - $01

Bits	7	6	5	4	3	2	1	0
Read Write	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
Reset	0	0	0	0	0	0	0	0

Low Side On/Off Bits (HBx_L)

These read/write bits turn on the low side MOSFETs. Reset clears the HBx_L bits.

- 1 = Low side MOSFET turned on for half-bridge output x
- 0 = Low side MOSFET turned off for half-bridge output x

OFFSET CHOPPING

If bit OFC_EN in the H-Bridge control register (HBCTL) is set, HB1 and HB2 will continue to switch on the low side MOSFETs with the rising edge of the FGEN signal and HB3 and HB4 will switch on the low side MOSFETs with the falling edge on the FGEN input. In step motor applications this feature allows the reduction of EMI due to a reduction of the di/dt (Figure 19).

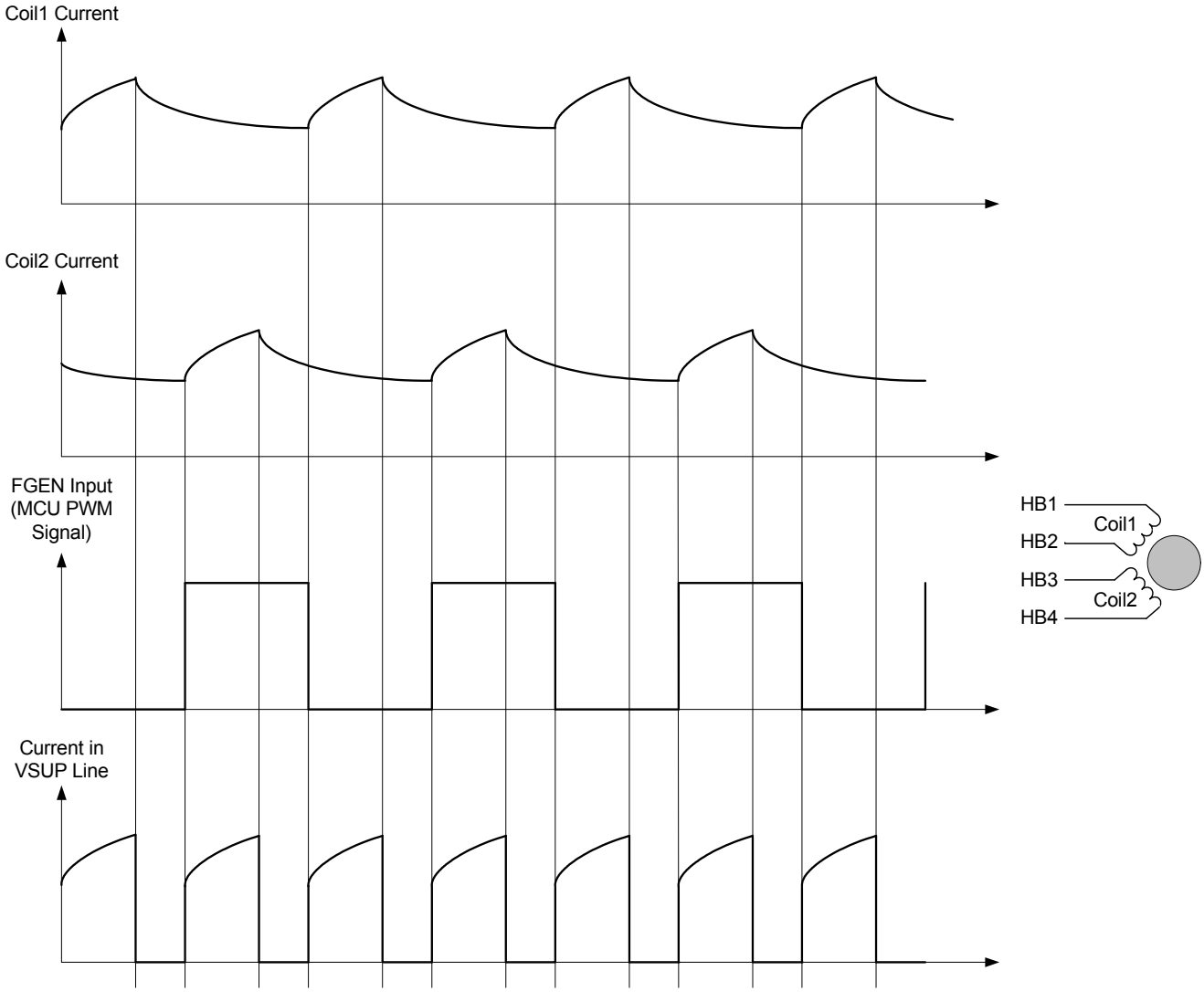


Figure 19. Offset Chopping for Step Motor Control

HALF-BRIDGE CURRENT RECOPY

Each low side MOSFET has an additional sense output to allow a current recopy feature. This sense source is internally connected to a shunt resistor. The drop voltage is amplified and switched to the analog multiplexer.

The factor for the current sense amplification can be selected via bit CSA in the system control register.

- CSA = 1: Low resolution selected (500 mA measurement range)
- CSA = 0: High resolution selected (2.5 A measurement range)

HALF-BRIDGE BEMF GENERATION

The BEMF output is set to 1 if a recirculation current is detected in any half-bridge. This recirculation current flows via the two freewheeling diodes of the power MOSFETs. The BEMF circuitry detects that and generates a HIGH on the BEMF output as long as a recirculation current is detected. This signal provides a flexible and reliable detection of stall in step motor applications. For this the BEMF circuitry takes advantage of the instability of the electrical and mechanical behavior of a step motor when blocked. In addition the signal can be used for open load detection (absence of this signal), see Figure 20.

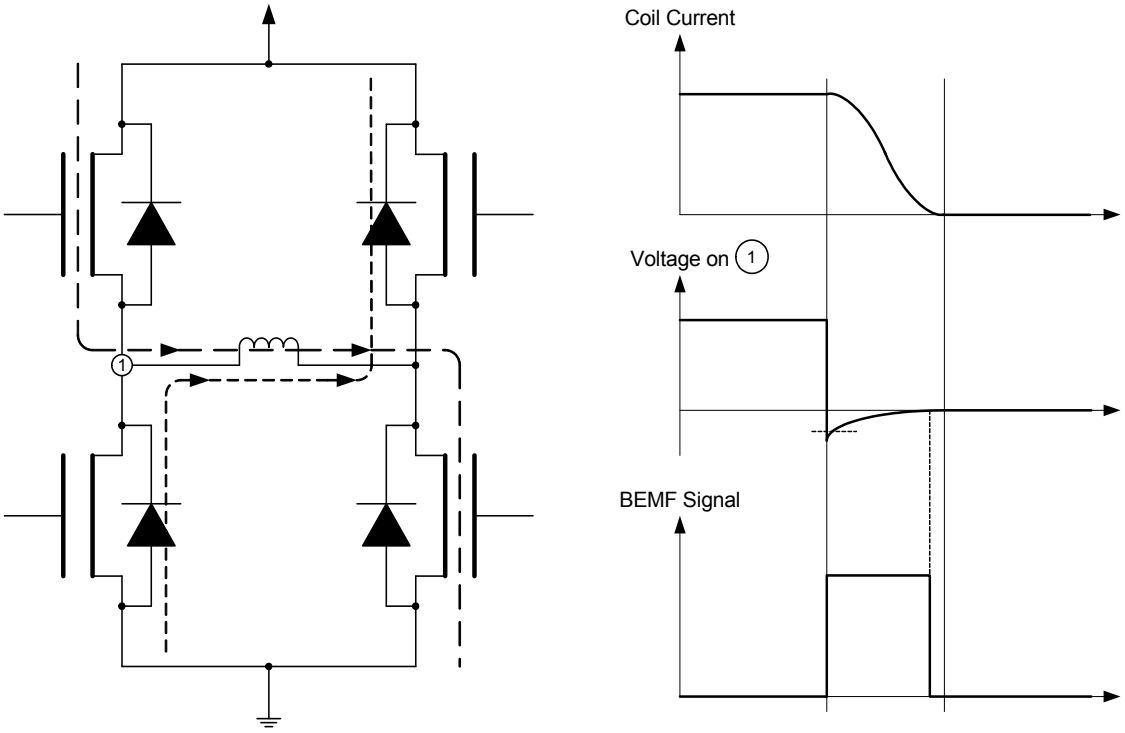


Figure 20. BEMF Signal Generation

HALF-BRIDGE OVER-TEMPERATURE PROTECTION

The half-bridge outputs provide an over-temperature pre-warning with the HTF in the Interrupt Flag Register (IFR). In order to protect the outputs against over-temperature, the high temperature reset must be enabled. If this value is reached, the part generates a reset and disables all power outputs.

HALF-BRIDGE OVER-CURRENT PROTECTION

The half-bridges are protected against short to GND, short to VSUP, and load shorts.

In the event an over-current on the high side is detected, the high side MOSFETs on all HB high side MOSFETs are switched off automatically. In the event an over-current on the low side is detected, all HB low side MOSFETs are switched off automatically. In both cases the over-current status flag HB_OCF in the system status register (SYSSTAT) is set.

The over-current status flag is cleared (and the outputs re-enabled) by writing a Logic [1] to the HB_OCF flag in the System status register or by reset.

HALF-BRIDGE OVER-VOLTAGE/UNDER-VOLTAGE

The half-bridge outputs are protected against under-voltage and over-voltage conditions. This protection is done by the low and high voltage interrupt circuitry. If one of these flags (LVF, HVF) is set, the outputs are automatically disabled.

The over-voltage/under-voltage status flags are cleared (and the outputs re-enabled) by writing a Logic [1] to the LVF/HVF flags in the interrupt flag register or by reset. Clearing this flag is useless as long as a high or low voltage condition is present.

HALF-BRIDGE CONTROL REGISTER (HBCTL)

Register Name and Address: HBCTL - $02

Bits	7	6	5	4	3	2	1	0
Read	OFC_EN	CSA	0	0	0	CLS2	CLS1	CLS0
Write								
Reset	0	0	0	0	0	0	0	0

H-Bridge Offset Chopping Enable Bit (OFC_EN)

This read/write bit enables offset chopping. Reset clears the OFC_EN bit.

- 1 = Offset chopping enabled
- 0 = Offset chopping disabled

H-Bridges Current Sense Amplification Select Bit (CSA)

This read/write bit selects the current sense amplification of the H-Bridges. Reset clears the CSA bit.

- 1 = Current sense amplification set for measuring 0.5 A.
- 0 = Current sense amplification set for measuring 2.5 A.

STOP Mode

During STOP mode the STOP mode regulator supplies a regulated output voltage. The STOP mode regulator has a very limited output current capability. The output voltage will be lower than the output voltage of the main voltage regulator.

FACTORY TRIMMING AND CALIBRATION

To enhance the ease-of-use of the 908E625, various parameters (e.g. ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the *empty* (0xFF) state:

- 0xFD80:0xFDDF Trim and Calibration Values
- 0xFFFE:0xFFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

Trim Values

Below the usage of the trim values located in the flash memory is explained

Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller without using any external components. The untrimmed frequency of the low frequency base clock (IBASE), will vary as much as ±25 percent due to process, temperature, and voltage dependencies. To compensate this dependencies a ICG trim values is located at address $FDC2. After trimming the ICG is a range of typ. ±2% (±3% max.) at nominal conditions (filtered (100 nF) and stabilized (4,7 µF) V_{DD} = 5.0 V, $T_{AMBIENT}$~25 °C) and will vary over temperature and voltage (V_{DD}) as indicated in the 68HC908EY16 datasheet.

To trim the ICG this values has to be copied to the ICG Trim Register ICGTR at address $38 of the MCU.

Important The value has to copied after every reset.

TYPICAL APPLICATIONS

DEVELOPMENT SUPPORT

As the 908E625 has the MC68HC908EY16 MCU embedded typically all the development tools available for the MCU also apply for this device, however due to the fact of the additional analog die circuitry and the nominal +12 V supply voltage some additional items have to be considered:

- nominal 12 V rather than 5.0 V or 3.0 V supply
- high voltage V_{TST} might be applied not only to $\overline{IRQ}$ pin, but $\overline{IRQ\_A}$ pin

For a detailed information on the MCU related development support see the MC68HC908EY16 datasheet - section development support.

The programming is principally possible at two stages in the manufacturing process - first on chip level, before the IC is soldered onto a pcb board and second after the IC is soldered onto the pcb board.

Chip level programming

On Chip level the easiest way is to only power the MCU with +5.0 V (see Figure 23) and not to provide the analog chip with VSUP, in this setup all the analog pin should be left open (e.g. VSUP[1:3]) and interconnections between MCU and analog die have to be separated (e.g. $\overline{IRQ}$ - $\overline{IRQ\_A}$).

This mode is well described in the MC68HC908EY16 datasheet - section development support.

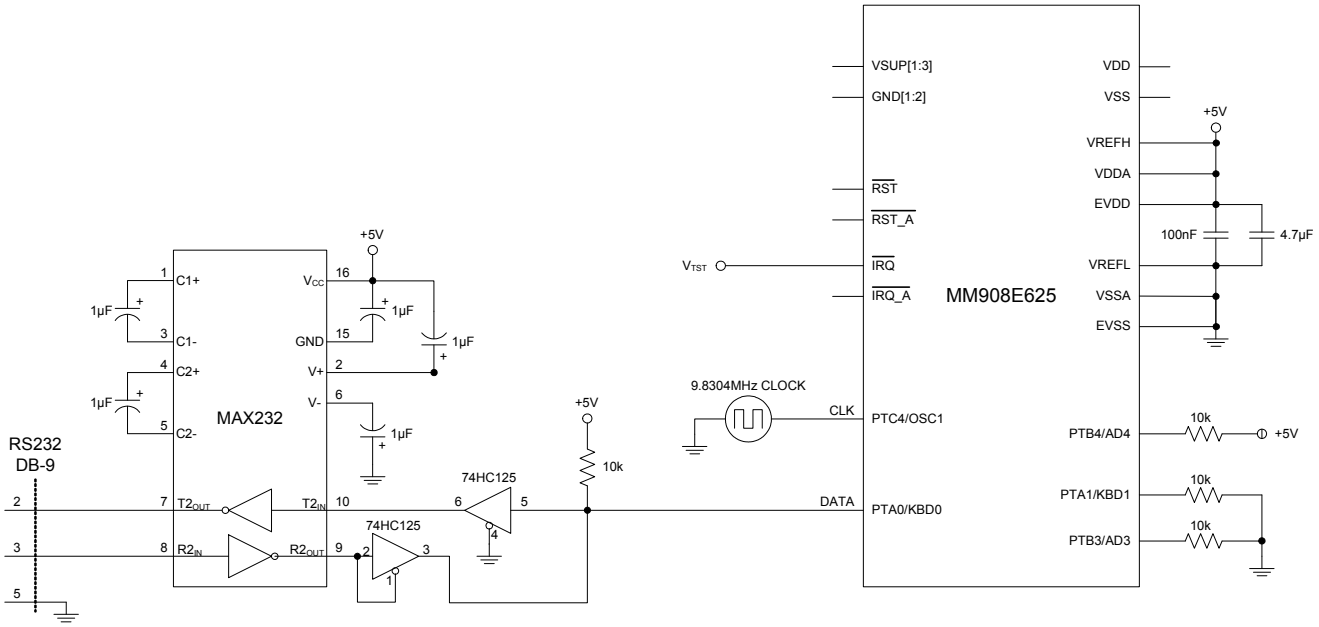


Figure 23. Normal Monitor Mode Circuit (MCU only)

Of course its also possible to supply the whole system with Vsup (12 V) instead as described in Figure 24, page 40.

PCB level programming

If the IC is soldered onto the pcb board its typically not possible to separately power the MCU with +5.0 V, the whole system has to be powered up providing V_{SUP} (see Figure 24).

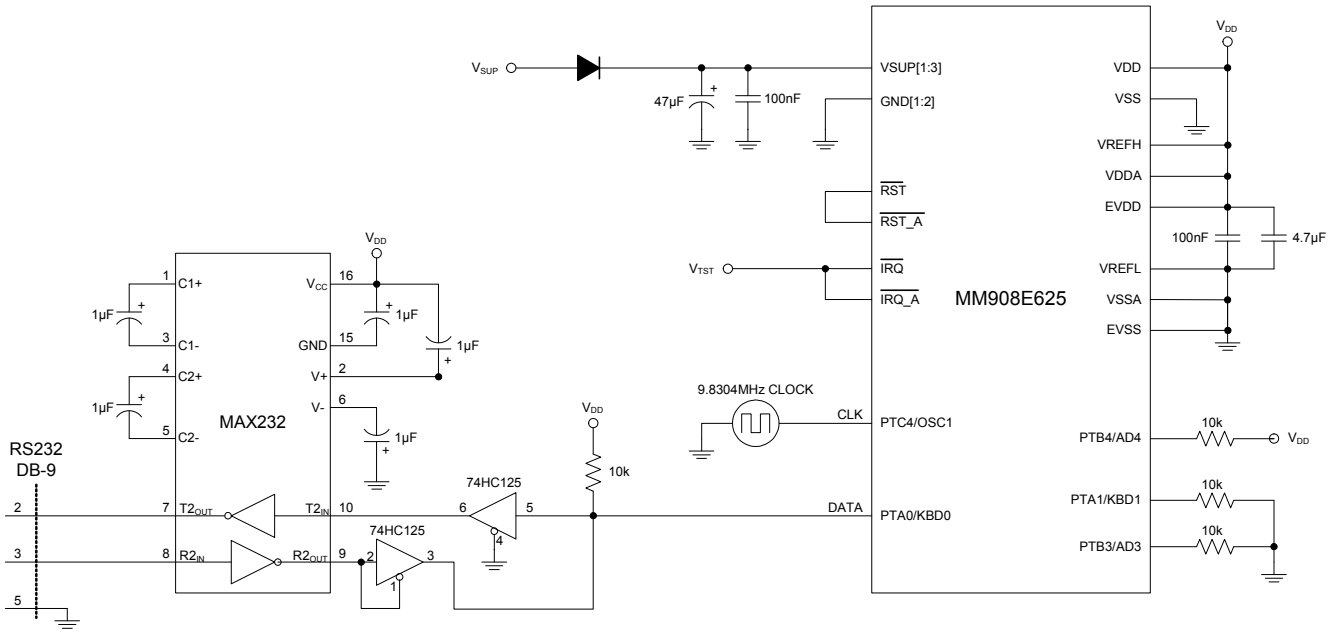


Figure 24. Normal Monitor Mode Circuit

Table 12 summarizes the possible configurations and the necessary setups.

Table 12. Monitor Mode Signal Requirements and Options

Mode	IRQ	RST	Reset Vector	Serial Communication		Mode Selection		ICG	COP	Normal Request Timeout	Communication Speed		
				PTA0	PTA1	PTB3	PTB4				External Clock	Bus Frequency	Baud Rate
Normal Monitor	V_{TST}	V_{DD}	X	1	0	0	1	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
Forced Monitor	V_{DD}	V_{DD}	$FFFF (blank)	1	0	X	X	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
	GND							ON	disabled	disabled	—	Nominal 1.6MHz	Nominal 6300
User	V_{DD}	V_{DD}	not $FFFF (not blank)	X	X	X	X	ON	enabled	enabled	—	Nominal 1.6MHz	Nominal 6300

Notes

1. PTA0 must have a pull-up resistor to V_{DD} in monitor mode
2. External clock is a 4.9152 MHz, 9.8304 MHz or 19.6608 MHz canned oscillator on OCS1
3. Communication speed with external clock is depending on external clock value. Baud rate is bus frequency / 256
4. X = don't care
5. V_{TST} is a high voltage $V_{DD} + 3.5\ V \leq V_{TST} \leq V_{DD} + 4.5\ V$

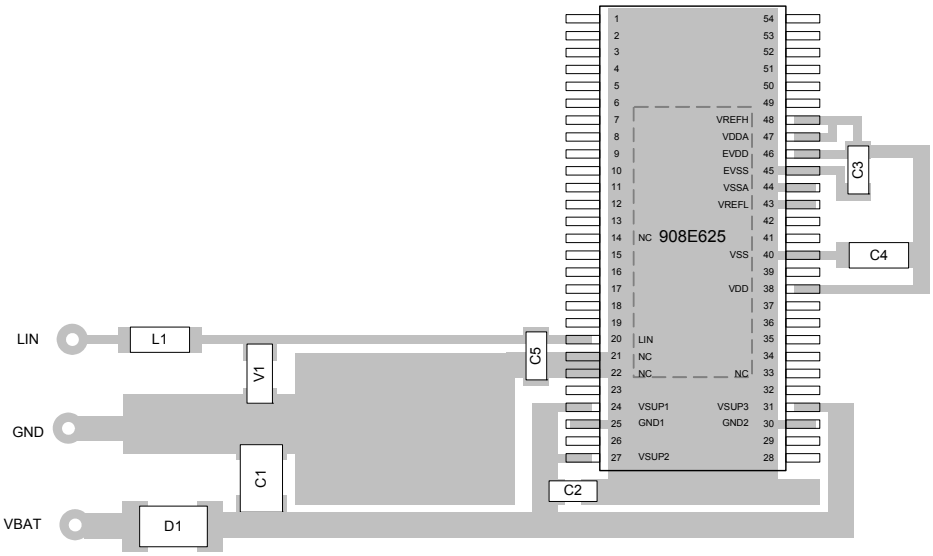


Figure 26. PCB Layout Recommendations

.

Table 13. Component Value Recommendation

Component	Recommended Value[1]	Comments / Signal routing
D1		reverse battery protection
C1	Bulk Capacitor	
C2	100nF, SMD Ceramic, Low ESR	Close (<5mm) to VSUP1, VSUP2 pins with good ground return
C3	100nF, SMD Ceramic, Low ESR	Close (<3mm) to digital supply pins (EVDD, EVSS) with good ground return. The positive analog (VREFH, VDDA) and the digital (EVDD) supply should be connected right at the C3.
C4	4,7uF, SMD Ceramic, Low ESR	Bulk Capacitor
C5	180pF, SMD Ceramic, Low ESR	Close (<5.0 mm) to LIN pin. Total Capacitance on LIN has to be below 220 pF. (C_{total} = $C_{LIN-Pin}$ + C5 + $C_{Varistor}$ ~ 10 pF + 180 pF + 15 pF)
V1[2]	Varistor Type TDK AVR-M1608C270MBAAB	Optional (close to LIN connector)
L1[2]	SMD Ferrite Bead Type TDK MMZ2012Y202B	Optional, (close to LIN connector)

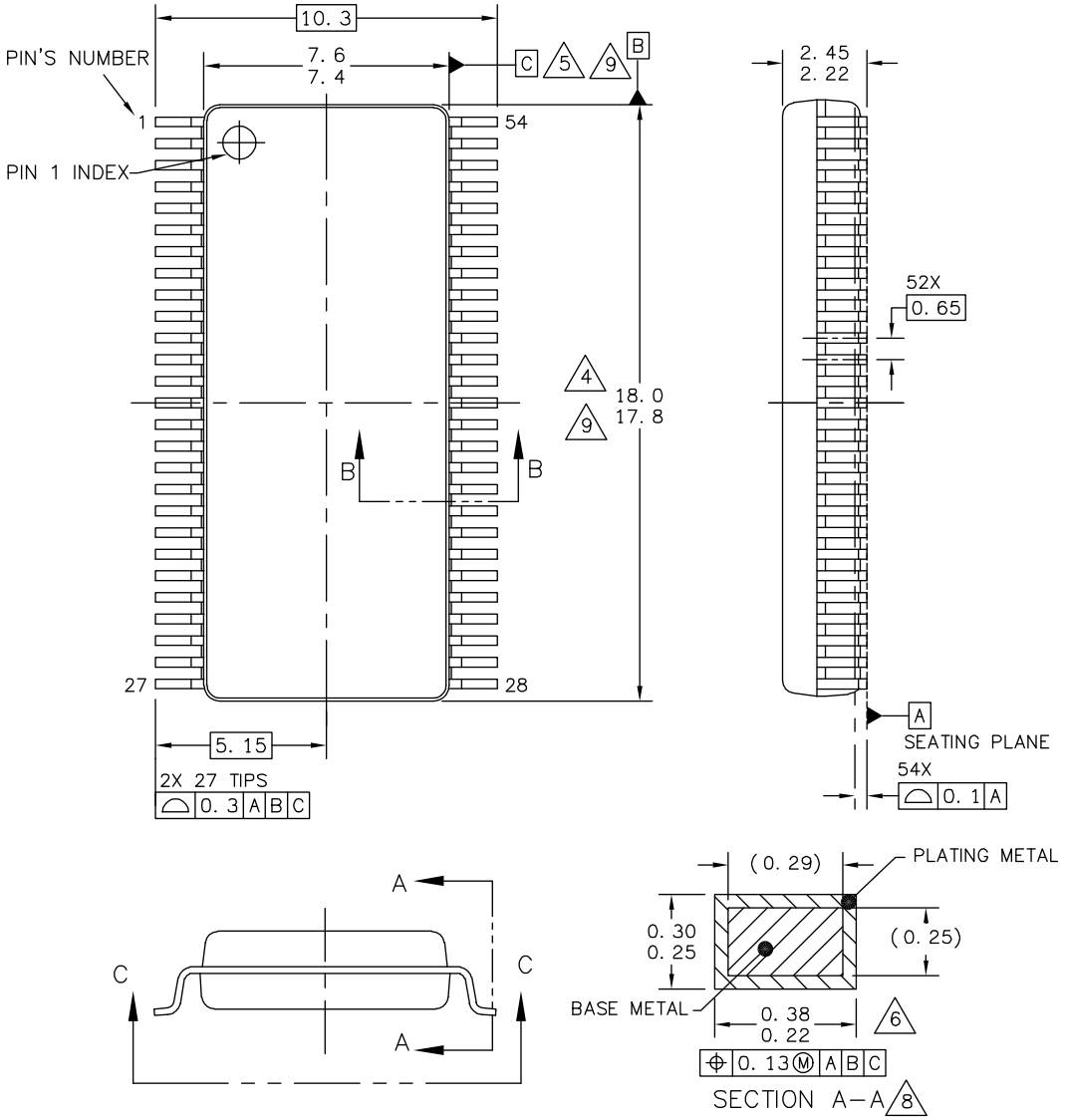
Notes

1. Freescale does not assume liability, endorse, or want components from external manufactures that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
2. Components are recommended to improve EMC and ESD performance.

PACKAGING

PACKAGING DIMENSIONS

Important: For the most current revision of the package, visit www.freescale.com and do a keyword search on the 98ARL10519D drawing number below. Dimensions shown are provided for reference ONLY.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 54LD SOIC W/B, 0.65 PITCH 5.1 X 10.3 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ARL10519D	REV: D
	CASE NUMBER: 1400–03	02 MAY 2008
	STANDARD: NON–JEDEC	

EK SUFFIX (PB-FREE)
54-PIN
98ARL10519D
ISSUE D

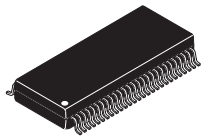
908E625

ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 2.0)

908E625

54-PIN SOICW-EP



EK SUFFIX (Pb-Free)
98ARL10519D
54-PIN SOICW-EP

Note For package dimensions, refer to 98ARL10519D.

Introduction

This thermal addendum ia provided as a supplement to the MM908E625 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application and packaging information is provided in the data sheet.

Package and Thermal Considerations

This MM908E625 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

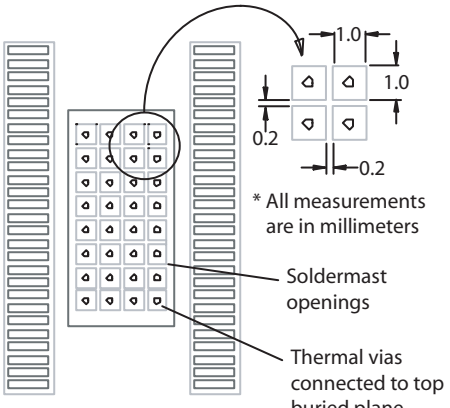
The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 1. Thermal Performance Comparison

Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$ (1)(2)	23	20	24
$R_{\theta JBmn}$ (2)(3)	9.0	6.0	10
$R_{\theta JAmn}$ (1)(4)	52	47	52
$R_{\theta JCmn}$ (5)	1.0	0	2.0

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.



54 Terminal SOIC-EP
0.65 mm Pitch
17.9 mm x 7.5 mm Body
10.3 mm x 5.1 mm Exposed Pad

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
7.0	9/2010	• Implemented Revision History page • Changed Peak Package Reflow Temperature During Reflow(7)(8) description. • Added note (8)
8.0	7/2011	• Changes to AWD Period Low = 512 tOSC and AWD Period High = 256 tOSC • Change to LIN Timing Description • Change to Stop Mode Output Voltage (Maximum Output Current 100 μA) • Added MM908E625ACEK and MM908E625ACPEK to the ordering information • Removed part numbers with DWB suffix • Updated Freescale form and style • Updated packaging information
9.0	10/2011	• Change to LIN Timing Description
10.0	04/2012	• Removed part number MM908E625ACEK. • Updated Freescale form and style

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: MM908E625
Rev 10
04/2012