What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.48x11.48)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc9321fa-112

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.

- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.

- Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.

- In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.

- Watchdog timer with separate on-chip oscillator, nominal 400 kHz, calibrated to ±5 %, requiring no external components. The watchdog prescaler is selectable from eight values.

- High-accuracy internal RC oscillator option, with clock doubler option, allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable.

- Switching on the fly among internal RC oscillator, watchdog oscillator, external clock source provides optimal support of minimal power active mode with fast switching to maximum performance.

- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).

- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A software reset function is also available.

- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.

- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.

- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.

- High current sourcing/sinking (20 mA) on eight I/O pins (P0.3 to P0.7, P1.4, P1.6, P1.7). All other port pins have high sinking capability (20 mA). A maximum limit is specified for the entire chip.

- Port 'input pattern match' detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.

- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.

- Only power and ground connections are required to operate the P89LPC9321 when internal reset option is selected.

- Four interrupt priority levels.

- Eight keypad interrupt inputs, plus two additional external interrupt inputs.

- Schmitt trigger port inputs.

- Second data pointer.

- Emulation support.

Table 4. **Special function registers** *…continued*
* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses		Reset value	
			MSB	LSB	Hex	Binary
WDL	Watchdog load	C1H			FF	1111 1111
WFEED1	Watchdog feed 1	C2H				
WFEED2	Watchdog feed 2	C3H				

[1] All ports are in input only (high-impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[3] The RSTSRC register reflects the cause of the P89LPC9321 reset except BOIF bit. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is x011 0000.

[4] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset and watchdog reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset sources that affect these SFRs are power-on reset and watchdog reset.

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Table 5.   Extended special function registers[1]

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							**LSB**	**Hex**	**Binary**
BODCFG	BOD configuration register	FFC8H	-	-	-	-	-	-	BOICFG1	BOICFG0	[2]	
CLKCON	CLOCK Control register	FFDEH	CLKOK	-	-	XTALWD	CLKDBL	FOSC2	FOSC1	FOSC0	[3]	1000 0100
PGACON1	PGA1 control register	FFE1H	ENPGA1	PGASEL11	PGASEL10	PGATRIM1	-	-	PGAG11	PGAG10	00	0000 0000
PGACON1B	PGA1 control register B	FFE4H	-	-	-	-	-	-	-	PGAENOFF1	00	0000 0000
PGA1TRIM8X16X	PGA1 trim register	FFE3H	16XTRIM3	16XTRIM2	16XTRIM1	16XTRIM0	8XTRIM3	8XTRIM2	8XTRIM1	8XTRIM0	[4]	
PGA1TRIM2X4X	PGA1 trim register	FFE2H	4XTRIM3	4XTRIM2	4XTRIM1	4XTRIM0	2XTRIM3	2XTRIM2	2XTRIM1	2XTRIM0	[4]	
RTCDATH	Real-time clock data register high	FFBFH									00	0000 0000
RTCDATL	Real-time clock data register low	FFBEH									00	0000 0000

[1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A,@DPTR and MOVX @DPTR,A instructions are used to access these extended SFRs.

[2] The BOICFG1/0 will be copied from UCFG1.5 and UCFG1.3 when power-on reset.

[3] CLKCON register reset value comes from UCFG1 and UCFG2. The reset value of CLKCON.2 to CLKCON.0 come from UCFG1.2 to UCFG1.0 and reset value of CLKDBL bit comes from UCFG2.7.

[4] On power-on reset and watchdog reset, the PGAxTRIM8X16X and PGAxTRIM2X4X registers are initialized with a factory preprogrammed value. Other resets will not cause initialization.

7.2 Enhanced CPU

The P89LPC9321 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

7.3 Clocks

7.3.1 Clock definitions

The P89LPC9321 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 6) and can also be optionally divided to a slower frequency (see Section 7.11 "CCLK modification: DIVM register").

Remark: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output. The clock doubler option, when enabled, provides an output frequency of 14.746 MHz.

PCLK — Clock for the various peripheral devices and is $^{CCLK}/_2$.

7.3.2 CPU clock (OSCCLK)

The P89LPC9321 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source.

7.4 External crystal oscillator option

The external crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 18 MHz. It can be the clock source of OSCCLK and RTC. Low speed oscillator option can be the clock source of WDT.

7.4.1 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

7.4.2 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

7.4.3 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration.
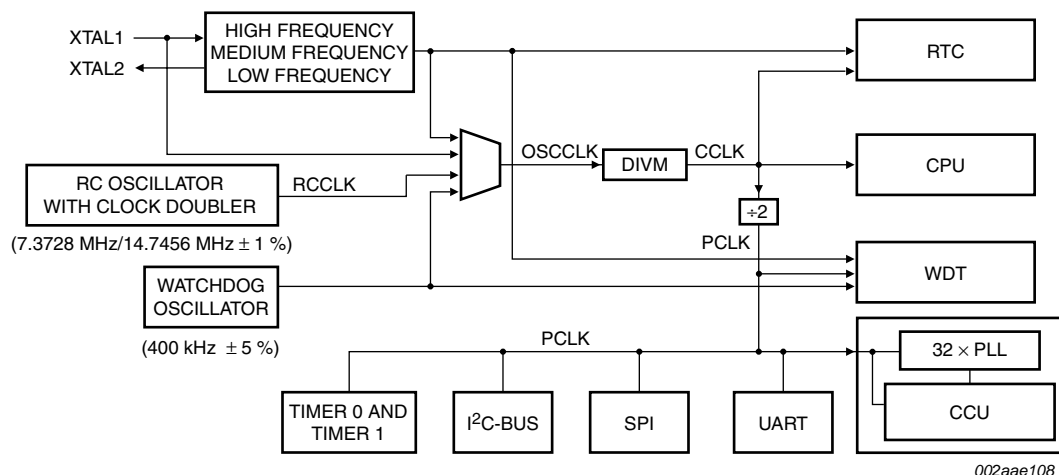
Fig 6. **Block diagram of oscillator control**

7.10 CCLK wake-up delay

The P89LPC9321 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 1024 OSCCLK cycles plus 60 μs to 100 μs. If the clock source is the internal RC oscillator, the delay is 200 μs to 300 μs. If the clock source is watchdog oscillator or external clock, the delay is 32 OSCCLK cycles.

7.11 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

7.12 Low power select

The P89LPC9321 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

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7.13 Memory organization

The various P89LPC9321 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- XDATA

  'External' Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the DPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC9321 has 512 bytes of on-chip XDATA memory, plus extended SFRs located in XDATA.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC9321 has 8 kB of on-chip Code memory.

The P89LPC9321 also has 512 bytes of on-chip data EEPROM that is accessed via SFRs (see Section 7.14).

7.14 Data RAM arrangement

The 768 bytes of on-chip RAM are organized as shown in Table 6.

Table 6.   On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256
XDATA	Auxiliary ('External Data') on-chip memory that is accessed using the MOVX instructions	512

7.15 Interrupts

The P89LPC9321 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC9321 supports 15 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port TX, serial port RX, combined serial port RX/TX, brownout detect, watchdog/RTC, I^{2}C-bus, keyboard, comparators 1 and 2, SPI, CCU, data EEPROM write completion.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

7.19.1 Reset vector

Following reset, the P89LPC9321 will fetch instructions from either address 0000H or the Boot address. The Boot address is formed by using the boot vector as the high byte of the address and the low byte of the address = 00H.

The boot address will be used if a UART break reset occurs, or the non-volatile boot status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see P89LPC9321 *User manual*). Otherwise, instructions will be fetched from address 0000H.

7.20 Timers/counters 0 and 1

The P89LPC9321 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters. An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'Timer' function, the register is incremented every machine cycle.

In the 'Counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (Modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

7.20.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

7.20.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

7.20.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

7.20.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

7.20.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

Fig 9.   Symmetrical PWM
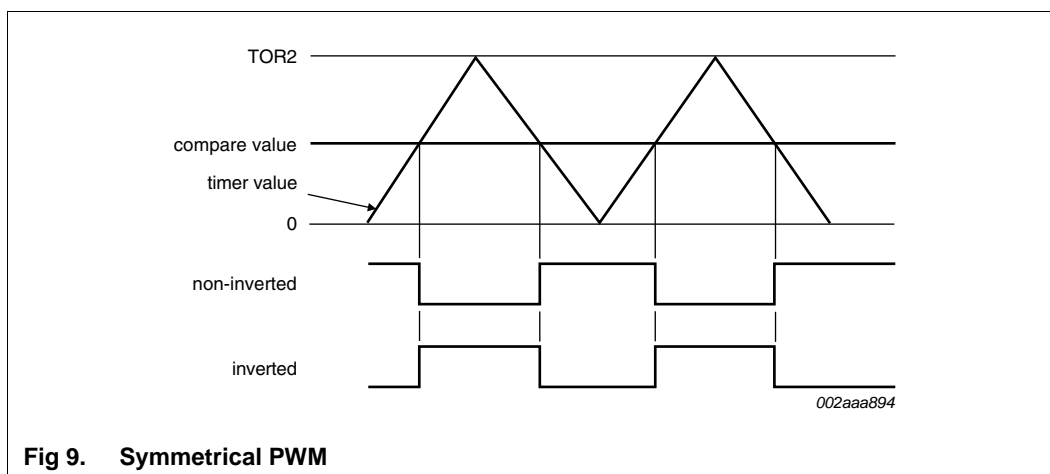
7.22.7 Alternating output mode

In asymmetrical mode, the user can set up PWM channels A/B and C/D as alternating pairs for bridge drive control. In this mode the output of these PWM channels are alternately gated on every counter cycle.
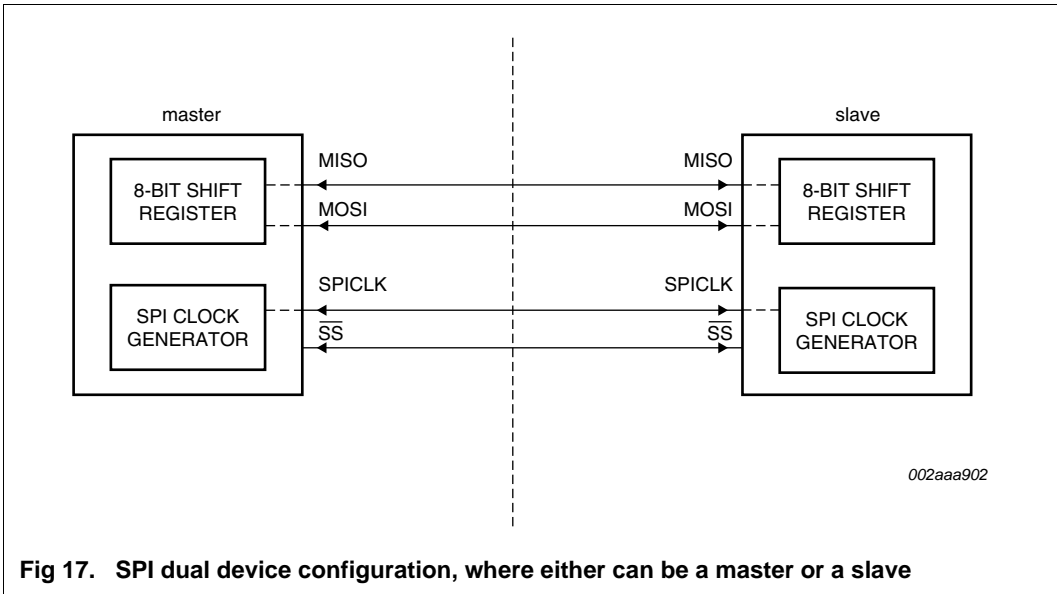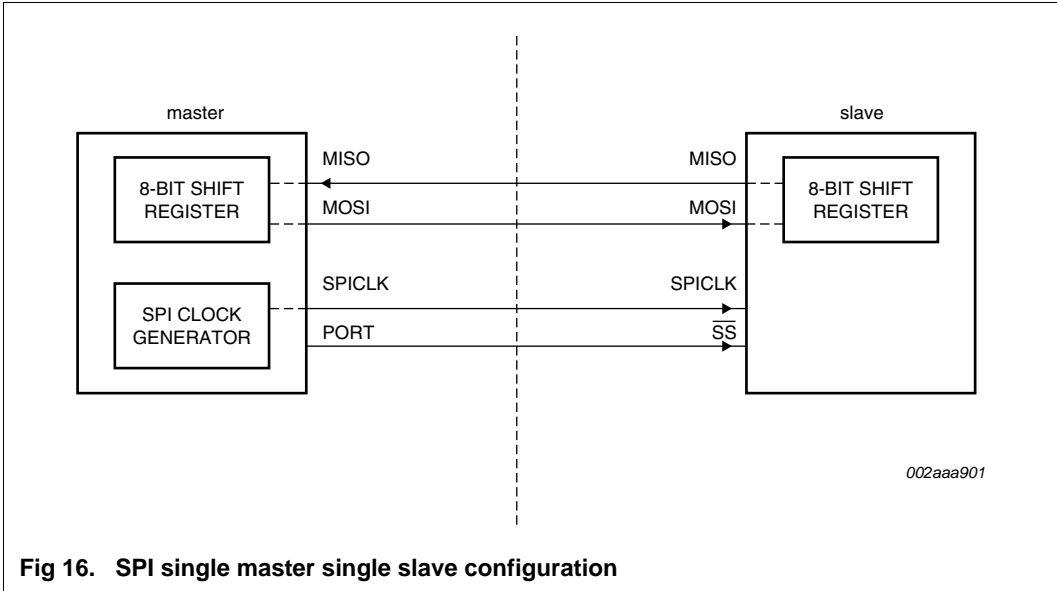

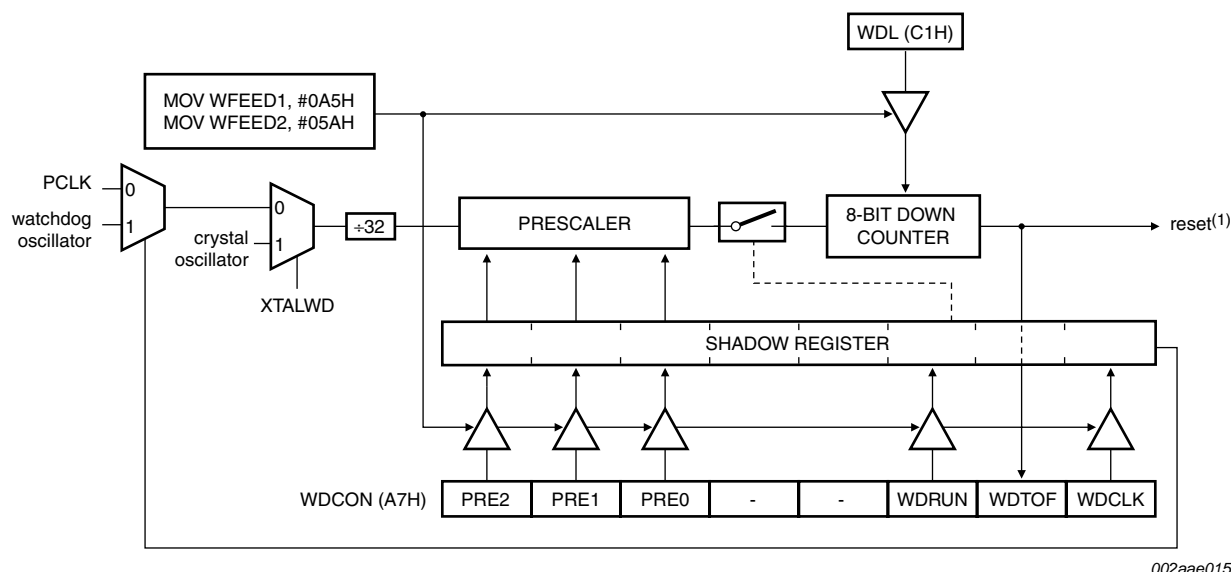**Fig 10.   Alternate output mode**
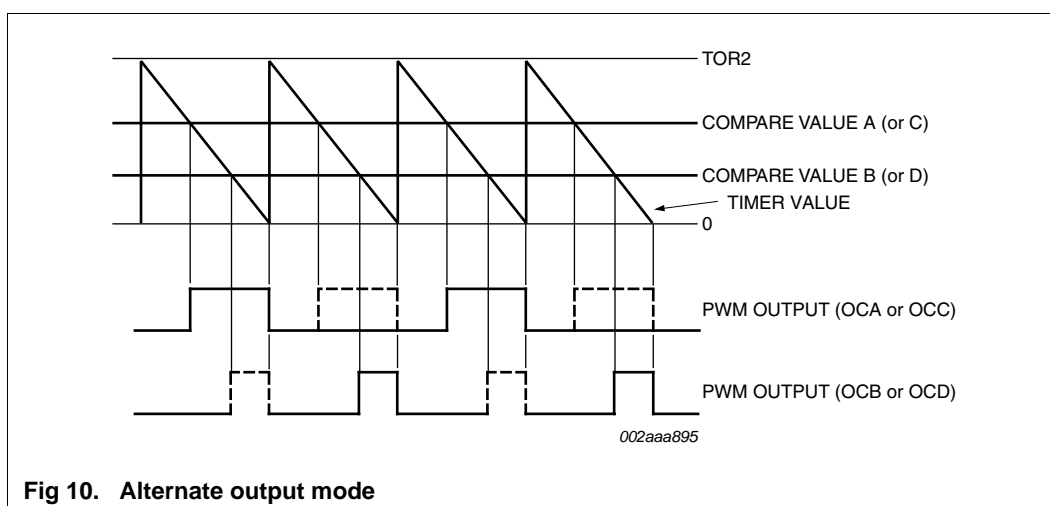
7.22.8 PLL operation

The PWM module features a Phase Locked Loop that can be used to generate a CCUCLK frequency between 16 MHz and 32 MHz. At this frequency the PWM module provides ultrasonic PWM frequency with 10-bit resolution provided that the crystal frequency is 1 MHz or higher. The PLL is fed an input signal from 0.5 MHz to 1 MHz and generates an output signal of 32 times the input frequency. This signal is used to clock the timer. The user will have to set a divider that scales PCLK by a factor from 1 to 16. This divider is found in the SFR register TCR21. The PLL frequency can be expressed as shown in Equation 1:

$$\text{PLL frequency} = \frac{\text{PCLK}}{(N + 1)} \tag{1}$$

Where: N is the value of PLLDV3:0.

7.25.1 Typical SPI configurations

Fig 16. SPI single master single slave configuration

Fig 17. SPI dual device configuration, where either can be a master or a slave

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(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 20. Watchdog timer in Watchdog mode (WDTE = 1)

7.29 Additional features

7.29.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

7.29.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

7.29.3 Data EEPROM

The P89LPC9321 has 512 bytes of on-chip Data EEPROM. The Data EEPROM is SFR based, byte readable, byte writable, and erasable (via row fill and sector fill). The user can read, write and fill the memory via SFRs and one interrupt. This Data EEPROM provides 100,000 minimum erase/program cycles for each byte.

- Byte mode: In this mode, data can be read and written one byte at a time.
- Row fill: In this mode, the addressed row (64 bytes) is filled with a single value. The entire row can be erased by writing 00H.
- Sector fill: In this mode, all 512 bytes are filled with a single value. The entire sector can be erased by writing 00H.

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7.30.8 ISP

ISP is performed without removing the microcontroller from the system. The ISP facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC9321 through the serial port. This firmware is provided by NXP and embedded within each P89LPC9321 device. The NXP ISP facility has made in-system programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

7.30.9 Power-on reset code execution

The P89LPC9321 contains two special flash elements: the Boot Vector and the Boot Status bit. Following reset, the P89LPC9321 examines the contents of the Boot Status bit. If the Boot Status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status bit is set to a value other than zero, the contents of the Boot Vector are used as the high byte of the execution address and the low byte is set to 00H.

Table 8 shows the factory default Boot Vector setting for these devices. A factory-provided boot loader is pre-programmed into the address space indicated and uses the indicated boot loader entry point to perform ISP functions. This code can be erased by the user.

Remark: Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector that contains this boot loader. Instead, the page erase function can be used to erase the first eight 64-byte pages located in this sector.

A custom boot loader can be written with the Boot Vector set to the custom boot loader, if desired.

Table 8.   Default boot vector values and ISP entry points

Device	Default boot vector	Default boot loader entry point	Default boot loader code range	1 kB sector range
P89LPC9321	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH

7.30.10 Hardware activation of the boot loader

The boot loader can also be executed by forcing the device into ISP mode during a power-on sequence (see the P89LPC9321 *User manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the boot vector (1FH) is changed, it will no longer point to the factory pre-programmed ISP boot loader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

7.31 User configuration bytes

Some user-configurable features of the P89LPC9321 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1 and UCFG2. Please see the P89LPC9321 *User's Manual* for additional details.

Table 10. **Static characteristics** *…continued*
V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 ℃ to +85 ℃ for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{THL}	HIGH-LOW transition current	all ports; V_I = 1.5 V at V_{DD} = 3.6 V	[9]	−30	-	−450	μA
$R_{RST\_N(int)}$	internal pull-up resistance on pin $\overline{RST}$	pin $\overline{RST}$		10	-	30	kΩ
BOD interrupt							
V_{trip}	trip voltage	falling stage					
		BOICFG1, BOICFG0 = 01		2.25	-	2.55	V
		BOICFG1, BOICFG0 = 10		2.60	-	2.80	V
		BOICFG1, BOICFG0 = 11		3.10	-	3.40	V
		rising stage					
		BOICFG1, BOICFG0 = 01		2.30	-	2.60	V
		BOICFG1, BOICFG0 = 10		2.70	-	2.90	V
		BOICFG1, BOICFG0 = 11		3.15	-	3.45	V
BOD reset							
V_{trip}	trip voltage	falling stage					
		BOE1, BOE0 = 01		2.10	-	2.30	V
		BOE1, BOE0 = 10		2.25	-	2.55	V
		BOE1, BOE0 = 11		2.80	-	3.20	V
		rising stage					
		BOE1, BOE0 = 01		2.20	-	2.40	V
		BOE1, BOE0 = 10		2.30	-	2.60	V
		BOE1, BOE0 = 11		2.90	-	3.30	V
BOD EEPROM/FLASH							
V_{trip}	trip voltage	falling stage		2.25	-	2.55	V
		rising stage		2.30	-	2.60	V
$V_{ref(bg)}$	band gap reference voltage			1.11	1.23	1.34	V
TC_{bg}	band gap temperature coefficient			-	10	20	ppm/℃

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 8 "Limiting values" for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] This specification can be applied to pins which have A/D input or analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS}.

[6] Pin capacitance is characterized but not tested.

[7] Measured with port in quasi-bidirectional mode.

[8] Measured with port in high-impedance mode.

[9] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

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10. Dynamic characteristics

Table 11.   Dynamic characteristics (12 MHz)
V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 ℃ to +85 ℃ for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	**Max**	**Min**	**Max**	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ±1 % at T_{amb} = 25 ℃; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON, V_{DD} = 2.7 V to 3.6 V	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	T_{amb} = 25 ℃	380	420	380	420	kHz
f_{osc}	oscillator frequency		0	12	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 22	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 22	33	$T_{cy(clk)} - t_{CLCX}$	33	-	ns
t_{CLCX}	clock LOW time	see Figure 22	33	$T_{cy(clk)} - t_{CHCX}$	33	-	ns
t_{CLCH}	clock rise time	see Figure 22	-	8	-	8	ns
t_{CHCL}	clock fall time	see Figure 22	-	8	-	8	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 21	$16T_{cy(clk)}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 21	$13T_{cy(clk)}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 21	-	$T_{cy(clk)} + 20$	-	103	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 21	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 21	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$CCLK/6$	0	2.0	MHz
	master		-	$CCLK/4$	-	3.0	MHz

Table 11. Dynamic characteristics (12 MHz) *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	**Max**	**Min**	**Max**	
T_{SPICYC}	SPI cycle time	see Figure 23, 24, 25, 26					
	slave		$6/_{CCLK}$	-	500	-	ns
	master		$4/_{CCLK}$	-	333	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 25, 26					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 25, 26					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 23, 24, 25, 26					
	master		$2/_{CCLK}$	-	165	-	ns
	slave		$3/_{CCLK}$	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 23, 24, 25, 26					
	master		$2/_{CCLK}$	-	165	-	ns
	slave		$3/_{CCLK}$	-	250	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 23, 24, 25, 26	100	-	100	-	ns
	master or slave						
t_{SPIDH}	SPI data hold time	see Figure 23, 24, 25, 26	100	-	100	-	ns
	master or slave						
t_{SPIA}	SPI access time	see Figure 25, 26					
	slave		0	120	0	120	ns
t_{SPIDIS}	SPI disable time	see Figure 25, 26					
	slave		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 23, 24, 25, 26					
	slave		-	240	-	240	ns
	master		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 23, 24, 25, 26	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 23, 24, 25, 26					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 23, 24, 25, 26					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

Table 12. Dynamic characteristics (18 MHz)

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ±1 % at T_{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	T_{amb} = 25 °C	380	420	380	420	kHz
f_{osc}	oscillator frequency		0	18	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 22	55	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 22	22	$T_{cy(clk)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 22	22	$T_{cy(clk)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 22	-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 22	-	5	-	5	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 21	$16T_{cy(clk)}$	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 21	$13T_{cy(clk)}$	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 21	-	$T_{cy(clk)} + 20$	-	75	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 21	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 21	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$CCLK/6$	0	3.0	MHz
	master		-	$CCLK/4$	-	4.5	MHz
T_{SPICYC}	SPI cycle time	see Figure 23, 24, 25, 26					
	slave		$6/CCLK$	-	333	-	ns
	master		$4/CCLK$	-	222	-	ns

12. Package outline

PLCC28: plastic leaded chip carrier; 28 leads

SOT261-2

DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A₁ min.	A₃	A₄ max.	bp	b₁	D(1)	E(1)	e	eD	eE	HD	HE	k	Lp	v	w	y	ZD(1) max.	ZE(1) max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.43 0.39	0.43 0.39	0.495 0.485	0.495 0.485	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT261-2	112E08	MS-018	EDR-7319			99-12-27 01-11-15

Fig 28. PLCC28 package outline (SOT261-2)

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13. Abbreviations

Table 16. Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
BOD	Brownout Detection
CPU	Central Processing Unit
CCU	Capture/Compare Unit
EPROM	Erasable Programmable Read-Only Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electro-Magnetic Interference
LSB	Least Significant Bit
MSB	Most Significant Bit
PGA	Programmable Gain Amplifier
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real-Time Clock
SCL	Serial Clock Line
SDA	Serial DAta Line
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

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