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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.48x11.48)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc9321fa-529

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
P89LPC9321FA	PLCC28	plastic leaded chip carrier; 28 leads	SOT261-2
P89LPC9321FDH	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
P89LPC9321FN	DIP28	plastic dual in-line package; 28 leads; (600 mil)	SOT117-1

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	Temperature range	Frequency
P89LPC9321FA	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9321FDH	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9321FN	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.7		I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 “Port configurations” and Table 10 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt trigger inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/ KBI0	3	I/O	**P0.0 —** Port 0 bit 0.
		O	**CMP2 —** Comparator 2 output
		I	**KBI0 —** Keyboard input 0.
P0.1/CIN2B/ KBI1	26	I/O	**P0.1 —** Port 0 bit 1.
		I	**CIN2B —** Comparator 2 positive input B.
		I	**KBI1 —** Keyboard input 1.
P0.2/CIN2A/ KBI2	25	I/O	**P0.2 —** Port 0 bit 2.
		I	**CIN2A —** Comparator 2 positive input A.
		I	**KBI2 —** Keyboard input 2.
P0.3/CIN1B/ KBI3	24	I/O	**P0.3 —** Port 0 bit 3. High current source.
		I	**CIN1B —** Comparator 1 positive input B.
		I	**KBI3 —** Keyboard input 3.
P0.4/CIN1A/ KBI4	23	I/O	**P0.4 —** Port 0 bit 4. High current source.
		I	**CIN1A —** Comparator 1 positive input A.
		I	**KBI4 —** Keyboard input 4.
P0.5/CMPREF/ KBI5	22	I/O	**P0.5 —** Port 0 bit 5. High current source.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0.6/CMP1/KBI6	20	I/O	**P0.6 —** Port 0 bit 6. High current source.
		O	**CMP1 —** Comparator 1 output.
		I	**KBI6 —** Keyboard input 6.
P0.7/T1/KBI7	19	I/O	**P0.7 —** Port 0 bit 7. High current source.
		I/O	**T1 —** Timer/counter 1 external count input or overflow output.
		I	**KBI7 —** Keyboard input 7.
P1.0 to P1.7		I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.16.1 “Port configurations” and Table 10 “Static characteristics” for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt trigger inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	18	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Transmitter output for serial port.
P1.1/RXD	17	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Receiver input for serial port.
P1.2/T0/SCL	12	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
		I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	**SCL —** I^2C-bus serial clock input/output.
P1.3/$\overline{\text{INT0}}$/SDA	11	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
		I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
		I/O	**SDA —** I^2C-bus serial data input/output.
P1.4/$\overline{\text{INT1}}$	10	I/O	**P1.4 —** Port 1 bit 4. High current source.
		I	**$\overline{\text{INT1}}$ —** External interrupt 1 input.
P1.5/$\overline{\text{RST}}$	6	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$ —** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode.
P1.6/OCB	5	I/O	**P1.6 —** Port 1 bit 6. High current source.
		O	**OCB —** Output Compare B
P1.7/OCC	4	I/O	**P1.7 —** Port 1 bit 7. High current source.
		O	**OCC —** Output Compare C.
P2.0 to P2.7		I/O	**Port 2:** Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 “Port configurations” and Table 10 “Static characteristics” for details. All pins have Schmitt trigger inputs. Port 2 also provides various special functions as described below:

7. Functional description

Remark: Please refer to the P89LPC9321 *User manual* for a more detailed functional description.

7.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I^2C-bus status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000
ICRAH	Input capture A register high	ABH									00	0000 0000
ICRAL	Input capture A register low	AAH									00	0000 0000
ICRBH	Input capture B register high	AFH									00	0000 0000
ICRBL	Input capture B register low	AEH									00	0000 0000
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1*	Interrupt enable 1	E8H	EIEE	EST	-	ECCU	ESPI	EC	EKBI	EI2C	00[1]	00x0 0000
	Bit address		**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/ PSRH	PT1H	PX1H	PT0H	PX0H	00[1]	x000 0000
	Bit address		**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**		
IP1*	Interrupt priority 1	F8H	PIEE	PST	-	PCCU	PSPI	PC	PKBI	PI2C	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	PIEEH	PSTH	-	PCCUH	PSPIH	PCH	PKBIH	PI2CH	00[1]	00x0 0000

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
P1*	Port 1	90H	OCC	OCB	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/SDA	T0/SCL	RXD	TXD	[1]	
	Bit address		**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**		
P2*	Port 2	A0H	ICA	OCA	SPICLK	$\overline{\text{SS}}$	MISO	MOSI	OCD	ICB	[1]	
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	[1]	
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[1]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[1]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[1]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[1]	00x0 xx00
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF[1]	1111 1111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00[1]	0000 0000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[1]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[1]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	-	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	DEEPD	VCPD	-	I2PD	SPPD	SPD	CCUPD	00[1]	0000 0000
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	BOIF	BOF	POF	R_BK	R_WD	R_SF	R_EX	[3]	
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1][6]	011x xx00

7.2 Enhanced CPU

The P89LPC9321 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

7.3 Clocks

7.3.1 Clock definitions

The P89LPC9321 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 6) and can also be optionally divided to a slower frequency (see Section 7.11 “CCLK modification: DIVM register”).

Remark: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output. The clock doubler option, when enabled, provides an output frequency of 14.746 MHz.

PCLK — Clock for the various peripheral devices and is $^{CCLK}/_{2}$.

7.3.2 CPU clock (OSCCLK)

The P89LPC9321 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source.

7.4 External crystal oscillator option

The external crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 18 MHz. It can be the clock source of OSCCLK and RTC. Low speed oscillator option can be the clock source of WDT.

7.4.1 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

7.4.2 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

7.4.3 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1 and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

7.15.1 External interrupt inputs

The P89LPC9321 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC9321 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 7.18 “Power reduction modes” for details.

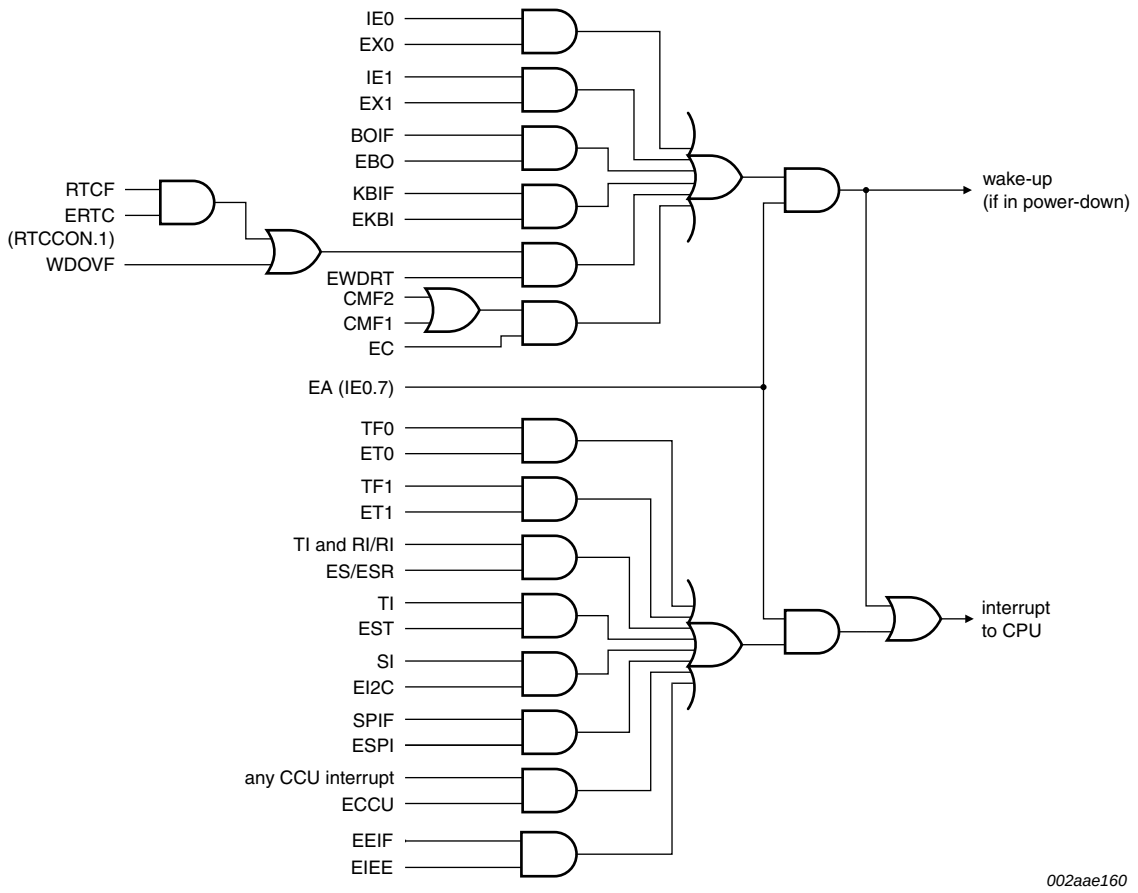

Fig 7. Interrupt sources, interrupt enables, and power-down wake-up sources

An open-drain port pin has a Schmitt trigger input that also has a glitch suppression circuit.

7.16.1.3 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt trigger input that also has a glitch suppression circuit.

7.16.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit. The P89LPC9321 device has high current source on eight pins in push-pull mode. See Table 9 “Limiting values”.

7.16.2 Port 0 analog functions

The P89LPC9321 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to logic 0s to enable digital functions.

7.16.3 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 are configurable for either input-only or open-drain.

Every output on the P89LPC9321 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 10 “Static characteristics” for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

7.17 Power monitoring functions

The P89LPC9321 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on detect and brownout detect.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: Brownout detect, watchdog timer, comparators (note that comparators can be powered down separately), and RTC/system timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

7.18.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

7.19 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either a LOW-active reset input or as a digital input, P1.5. The Reset Pin Enable (RPE) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this pin will function as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Note: During a power cycle, V_{DD} must fall below V_{POR} before power is reapplied, in order to ensure a power-on reset (see Table 10 “Static characteristics”).

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1)
- Power-on detect
- Brownout detect
- Watchdog timer
- Software reset
- UART break character detect reset

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- A Watchdog reset is similar to a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

7.23.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

7.23.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SnBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

7.23.9 Transmit interrupts with double buffering enabled (modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the TI interrupt is generated when the double buffer is ready to receive new data.

7.23.10 The 9th bit (bit 8) in double buffering (modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the TI interrupt.

If double buffering is enabled, TB **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

7.24 I^{2}C-bus serial interface

The I^{2}C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I^{2}C-bus may be used for test and diagnostic purposes.

A typical I^{2}C-bus configuration is shown in Figure 13. The P89LPC9321 device provides a byte-oriented I^{2}C-bus interface that supports data transfers up to 400 kHz.

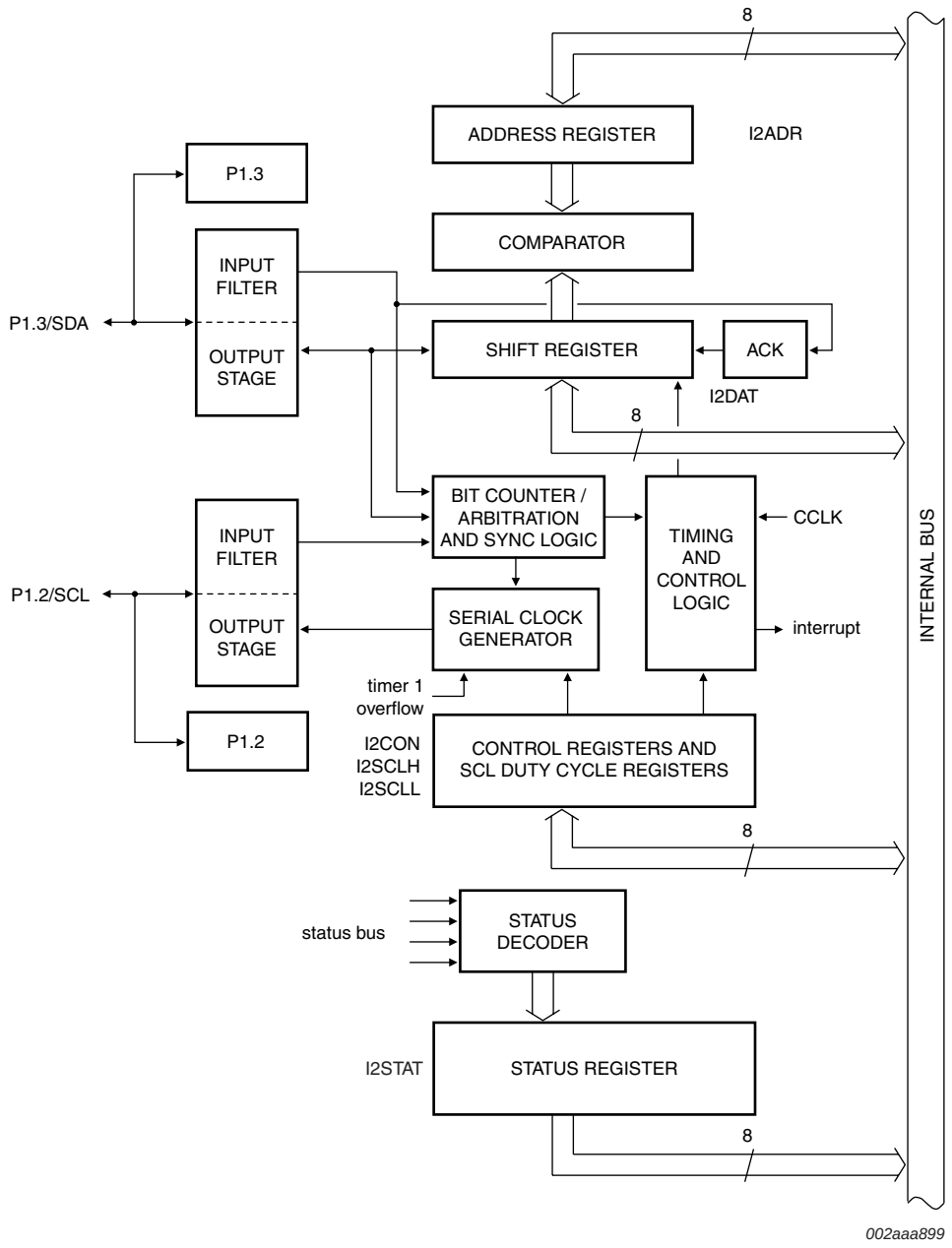

Fig 14. I²C-bus serial interface block diagram

After the operation finishes, the hardware will set the EEIF bit, which if enabled will generate an interrupt. The flag is cleared by software.

Remark: When voltage supply is lower than 2.4 V, the BOD FLASH is tripped and Data EEPROM program or erase is blocked. EWERR1 and EWERR0 bits are used to indicate the write error for BOD EEPROM. Both can be cleared by power on reset, watchdog reset or software write.

7.30 Flash program memory

7.30.1 General description

The P89LPC9321 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC9321 flash reliably stores memory contents even after 100,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC9321 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms. When voltage supply is lower than 2.4 V, the BOD FLASH is tripped and flash erase/program is blocked.

7.30.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ISP/IAP/ICP.
- Internal fixed boot ROM, containing low-level IAP routines available to user code.
- Default loader providing ISP via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- 100,000 typical erase/program cycles for each byte.
- 10 year minimum data retention.

7.30.3 Flash organization

The program memory consists of eight 1 kB sectors on the P89LPC9321 devices. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

7.30.4 Using flash as data storage

The flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

7.30.5 Flash programming and erasing

Four different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock/serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing for the device to be programmed in circuit through the serial port. The flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit Cyclic Redundancy Check (CRC) result on either a sector or the entire user code space.

Remark: When voltage supply is lower than 2.4 V, the BOD FLASH is tripped and flash erase/program is blocked.

7.30.6 ICP

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC9321 through a two-wire serial interface. The NXP ICP facility has made in-circuit programming in an embedded application - using commercially available programmers - possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC9321 *User manual*.

7.30.7 IAP

IAP is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The NXP IAP has made in-application programming in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a Boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF03H. The Boot ROM occupies the program memory space at the top of the address space from FF00H to FEFFH, thereby not conflicting with the user program memory space.

In addition, IAP operations can be accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC9321 *User manual*.

8. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		−55	+125	°C
T_{stg}	storage temperature		−65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per input/output pin		-	20	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	20	mA
$I_{I/Otot(max)}$	maximum total input/output current		-	100	mA
V_{xtal}	crystal voltage	on XTAL1, XTAL2 pin to V_{SS}	-	V_{DD} + 0.5	V
V_n	voltage on any other pin	except XTAL1, XTAL2 to V_{SS}	−0.5	+5.5	V
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins [2]	−3000	+3000	V
		charged device model; all pins	−700	+700	V

[1] The following applies to Table 9:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over ambient temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Table 10. Static characteristics *…continued*
V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{THL}	HIGH-LOW transition current	all ports; V_I = 1.5 V at V_{DD} = 3.6 V	[9]	−30	-	−450	μA
$R_{RST\_N(int)}$	internal pull-up resistance on pin $\overline{RST}$	pin $\overline{RST}$		10	-	30	kΩ
BOD interrupt							
V_{trip}	trip voltage	falling stage					
		BOICFG1, BOICFG0 = 01		2.25	-	2.55	V
		BOICFG1, BOICFG0 = 10		2.60	-	2.80	V
		BOICFG1, BOICFG0 = 11		3.10	-	3.40	V
		rising stage					
		BOICFG1, BOICFG0 = 01		2.30	-	2.60	V
		BOICFG1, BOICFG0 = 10		2.70	-	2.90	V
		BOICFG1, BOICFG0 = 11		3.15	-	3.45	V
BOD reset							
V_{trip}	trip voltage	falling stage					
		BOE1, BOE0 = 01		2.10	-	2.30	V
		BOE1, BOE0 = 10		2.25	-	2.55	V
		BOE1, BOE0 = 11		2.80	-	3.20	V
		rising stage					
		BOE1, BOE0 = 01		2.20	-	2.40	V
		BOE1, BOE0 = 10		2.30	-	2.60	V
		BOE1, BOE0 = 11		2.90	-	3.30	V
BOD EEPROM/FLASH							
V_{trip}	trip voltage	falling stage		2.25	-	2.55	V
		rising stage		2.30	-	2.60	V
$V_{ref(bg)}$	band gap reference voltage			1.11	1.23	1.34	V
TC_{bg}	band gap temperature coefficient			-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 8 “Limiting values” for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

10. Dynamic characteristics

Table 11. Dynamic characteristics (12 MHz)

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ±1 % at T_{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON, V_{DD} = 2.7 V to 3.6 V	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	T_{amb} = 25 °C	380	420	380	420	kHz
f_{osc}	oscillator frequency		0	12	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 22	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{\text{RST}}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{\text{RST}}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{\text{RST}}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{\text{RST}}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 22	33	$T_{cy(clk)} - t_{CLCX}$	33	-	ns
t_{CLCX}	clock LOW time	see Figure 22	33	$T_{cy(clk)} - t_{CHCX}$	33	-	ns
t_{CLCH}	clock rise time	see Figure 22	-	8	-	8	ns
t_{CHCL}	clock fall time	see Figure 22	-	8	-	8	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 21	$16T_{cy(clk)}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 21	$13T_{cy(clk)}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 21	-	$T_{cy(clk)}$ + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 21	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 21	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	2.0	MHz
	master		-	$^{CCLK}/_{4}$	-	3.0	MHz

11.2 PGA electrical characteristics

Table 15. PGA electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.
All limits valid for an external source impedance of less than 10 kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{s(PGA)}$	PGA settling time	within accuracy of ADC	-	-	1	µs
G_{PGA}	PGA gain	G = 1	0.95	1.00	1.05	V/V
		G = 2	1.87	1.97	2.07	V/V
		G = 4	3.70	3.89	4.08	V/V
		G = 8	7.22	7.60	7.98	V/V
		G = 16	14.38	15.14	15.90	V/V
$t_{startup}$	start-up time		-	-	2	µs
$V_{offset(O)(nom)}$	nominal output offset voltage		-	100	-	mV

14. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC9321 v.2	20101116	Product data sheet	-	P89LPC9321 v.1
Modifications:	• Table 9: Updated table. • Table 14: Updated I_{LI} max value. • Section 7.4: Added low speed oscillator information. • Section 7.28: Added low speed oscillator information. • Changed data sheet status to Product.			
P89LPC9321 v.1	20081209	Product data sheet	-	-