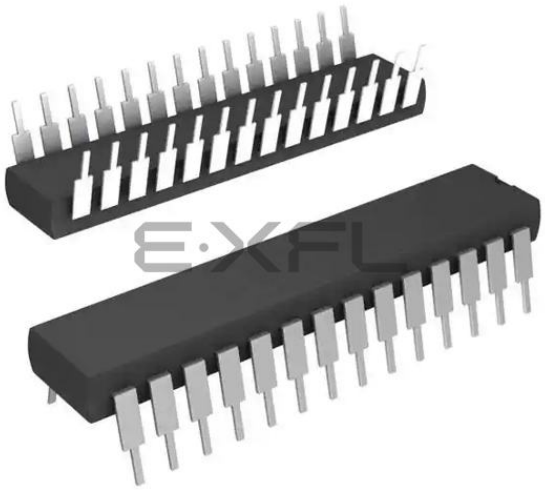

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc9321fn-112

4. Block diagram

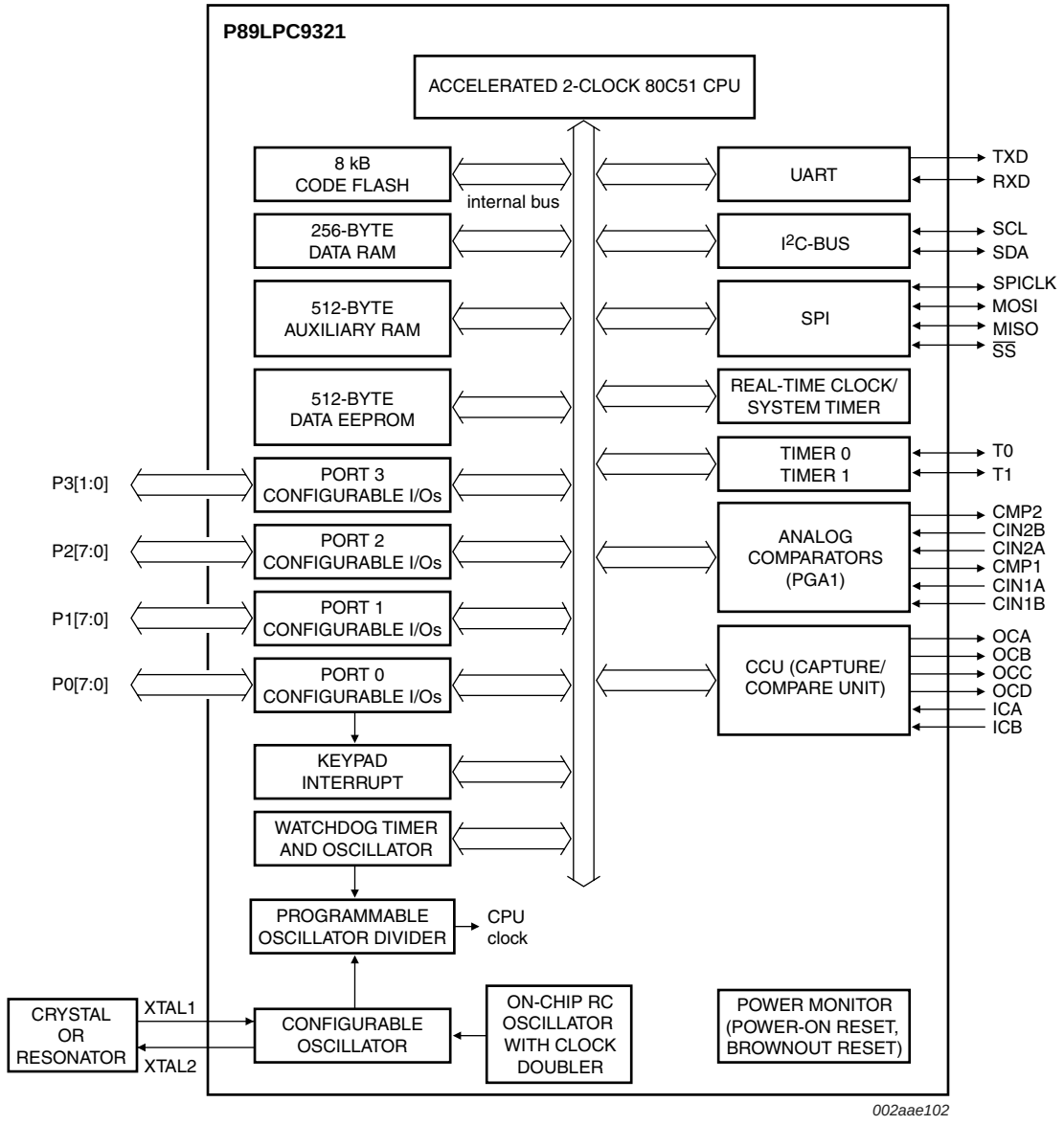


Fig 1. Block diagram

7. Functional description

Remark: Please refer to the P89LPC9321 *User manual* for a more detailed functional description.

7.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
DEEDAT	Data EEPROM data register	F2H									00	0000 0000
DEEADR	Data EEPROM address register	F3H									00	0000 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I^2C-bus slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
	Bit address		**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON*	I^2C-bus control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I^2C-bus data register	DAH										

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
P1*	Port 1	90H	OCC	OCB	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/SDA	T0/SCL	RXD	TXD	[1]	
	Bit address		**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**		
P2*	Port 2	A0H	ICA	OCA	SPICLK	$\overline{\text{SS}}$	MISO	MOSI	OCD	ICB	[1]	
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	[1]	
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[1]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[1]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[1]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[1]	00x0 xx00
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF[1]	1111 1111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00[1]	0000 0000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[1]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[1]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	-	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	DEEPD	VCPD	-	I2PD	SPPD	SPD	CCUPD	00[1]	0000 0000
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	BOIF	BOF	POF	R_BK	R_WD	R_SF	R_EX	[3]	
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1][6]	011x xx00

Table 5. Extended special function registers[1]

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
BODCFG	BOD configuration register	FFC8H	-	-	-	-	-	-	BOICFG1	BOICFG0	[2]	
CLKCON	CLOCK Control register	FFDEH	CLKOK	-	-	XTALWD	CLKDBL	FOSC2	FOSC1	FOSC0	[3]	1000 0100
PGACON1	PGA1 control register	FFE1H	ENPGA1	PGASEL11	PGASEL10	PGATRIM1	-	-	PGAG11	PGAG10	00	0000 0000
PGACON1B	PGA1 control register B	FFE4H	-	-	-	-	-	-	-	PGAENOFF1	00	0000 0000
PGA1TRIM8X16X	PGA1 trim register	FFE3H	16XTRIM3	16XTRIM2	16XTRIM1	16XTRIM0	8XTRIM3	8XTRIM2	8XTRIM1	8XTRIM0	[4]	
PGA1TRIM2X4X	PGA1 trim register	FFE2H	4XTRIM3	4XTRIM2	4XTRIM1	4XTRIM0	2XTRIM3	2XTRIM2	2XTRIM1	2XTRIM0	[4]	
RTCDATH	Real-time clock data register high	FFBFH									00	0000 0000
RTCDATL	Real-time clock data register low	FFBEH									00	0000 0000

[1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A,@DPTR and MOVX @DPTR,A instructions are used to access these extended SFRs.

[2] The BOICFG1/0 will be copied from UCFG1.5 and UCFG1.3 when power-on reset.

[3] CLKCON register reset value comes from UCFG1 and UCFG2. The reset value of CLKCON.2 to CLKCON.0 come from UCFG1.2 to UCFG1.0 and reset value of CLKDBL bit comes from UCFG2.7.

[4] On power-on reset and watchdog reset, the PGAxTRIM8X16X and PGAxTRIM2X4X registers are initialized with a factory preprogrammed value. Other resets will not cause initialization.

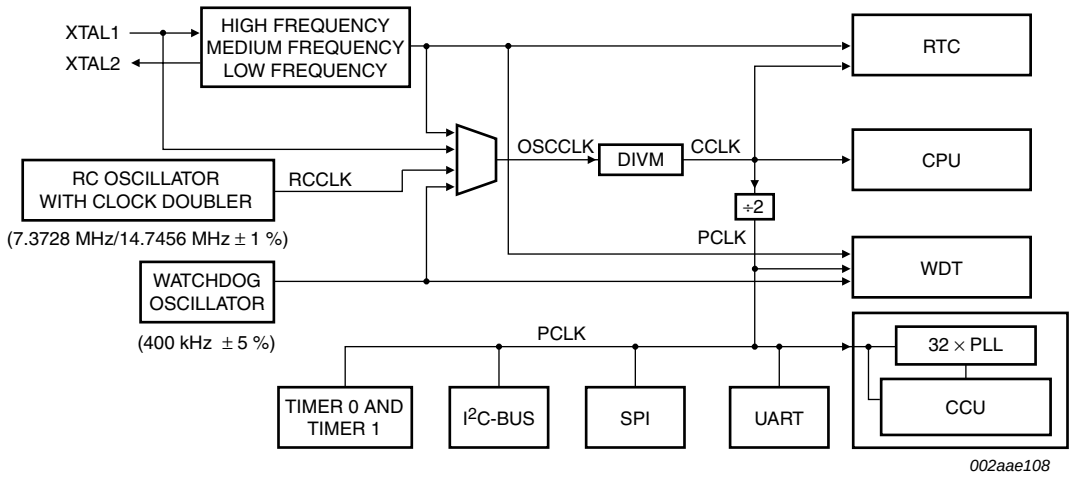


Fig 6. Block diagram of oscillator control

7.10 CCLK wake-up delay

The P89LPC9321 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 1024 OSCCLK cycles plus 60 μs to 100 μs. If the clock source is the internal RC oscillator, the delay is 200 μs to 300 μs. If the clock source is watchdog oscillator or external clock, the delay is 32 OSCCLK cycles.

7.11 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

7.12 Low power select

The P89LPC9321 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1 and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

7.15.1 External interrupt inputs

The P89LPC9321 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC9321 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 7.18 “Power reduction modes” for details.

When a reload occurs, the CCU Timer Overflow Interrupt Flag will be set, and an interrupt generated if enabled. The 16-bit CCU timer may also be used as an 8-bit up/down timer.

7.22.4 Output compare

There are four output compare channels: A, B, C and D. Each output compare channel needs to be enabled in order to operate and the user will have to set the associated I/O pin to the desired output mode to connect the pin. When the contents of the timer matches that of a capture compare control register, the Timer Output Compare Interrupt Flag (TOCFx) becomes set. An interrupt will occur if enabled.

7.22.5 Input capture

Input capture is always enabled. Each time a capture event occurs on one of the two input capture pins, the contents of the timer is transferred to the corresponding 16-bit input capture register. The capture event can be programmed to be either rising or falling edge triggered. A simple noise filter can be enabled on the input capture by enabling the Input Capture Noise Filter bit. If set, the capture logic needs to see four consecutive samples of the same value in order to recognize an edge as a capture event. An event counter can be set to delay a capture by a number of capture events.

7.22.6 PWM operation

PWM operation has two main modes, symmetrical and asymmetrical.

In asymmetrical PWM operation the CCU timer operates in down-counting mode regardless of the direction control bit.

In symmetrical mode, the timer counts up/down alternately. The main difference from basic timer operation is the operation of the compare module, which in PWM mode is used for PWM waveform generation.

As with basic timer operation, when the PWM (compare) pins are connected to the compare logic, their logic state remains unchanged. However, since bit FCO is used to hold the halt value, only a compare event can change the state of the pin.

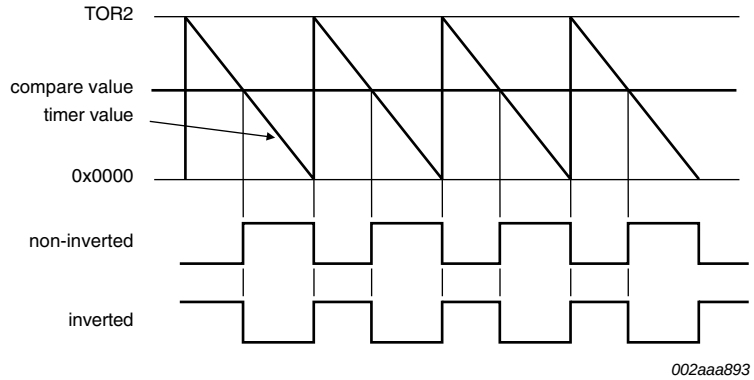


Fig 8. Asymmetrical PWM, down-counting

7.23.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

7.23.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SnBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

7.23.9 Transmit interrupts with double buffering enabled (modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the TI interrupt is generated when the double buffer is ready to receive new data.

7.23.10 The 9th bit (bit 8) in double buffering (modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the TI interrupt.

If double buffering is enabled, TB **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

7.24 I^{2}C-bus serial interface

The I^{2}C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I^{2}C-bus may be used for test and diagnostic purposes.

A typical I^{2}C-bus configuration is shown in Figure 13. The P89LPC9321 device provides a byte-oriented I^{2}C-bus interface that supports data transfers up to 400 kHz.

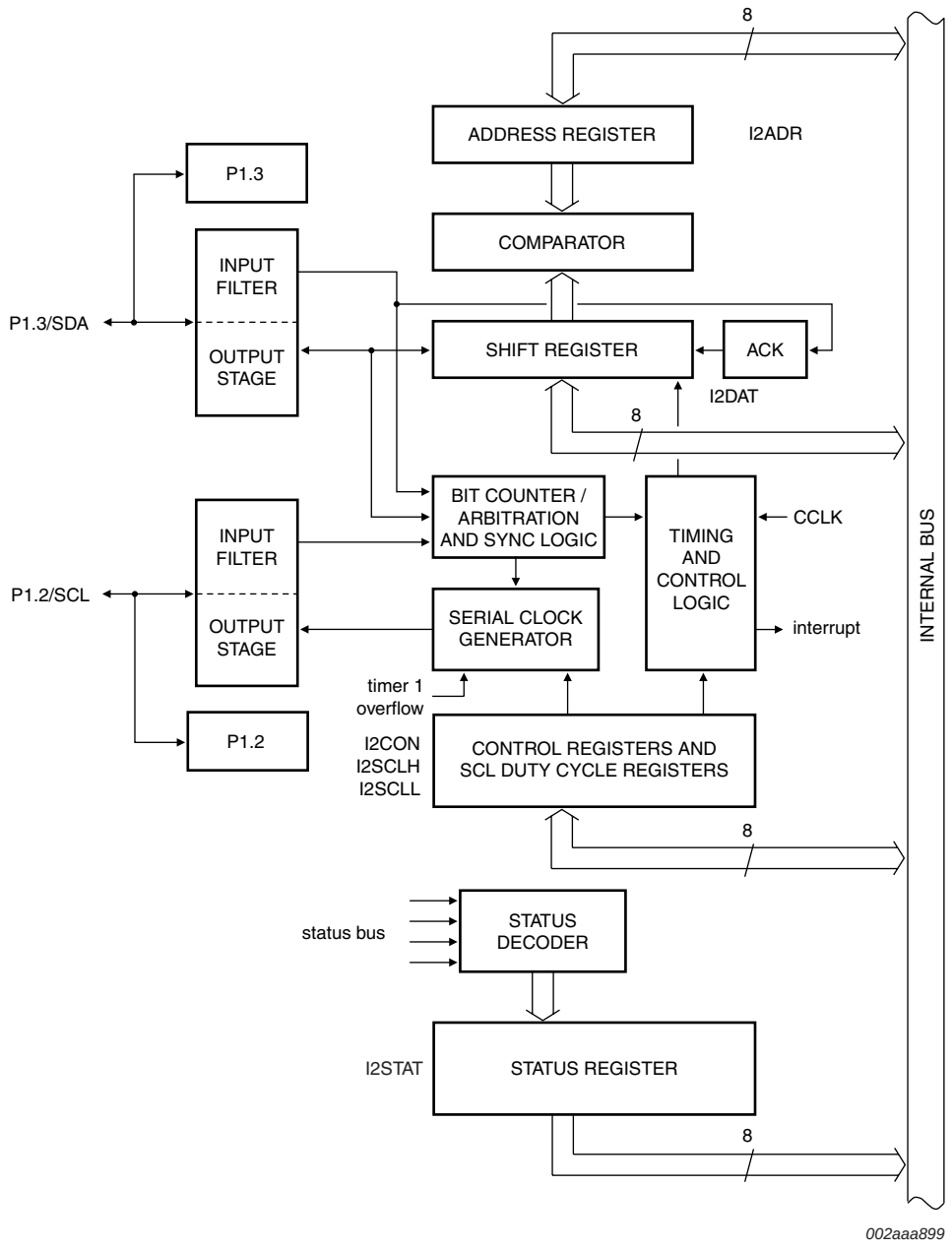
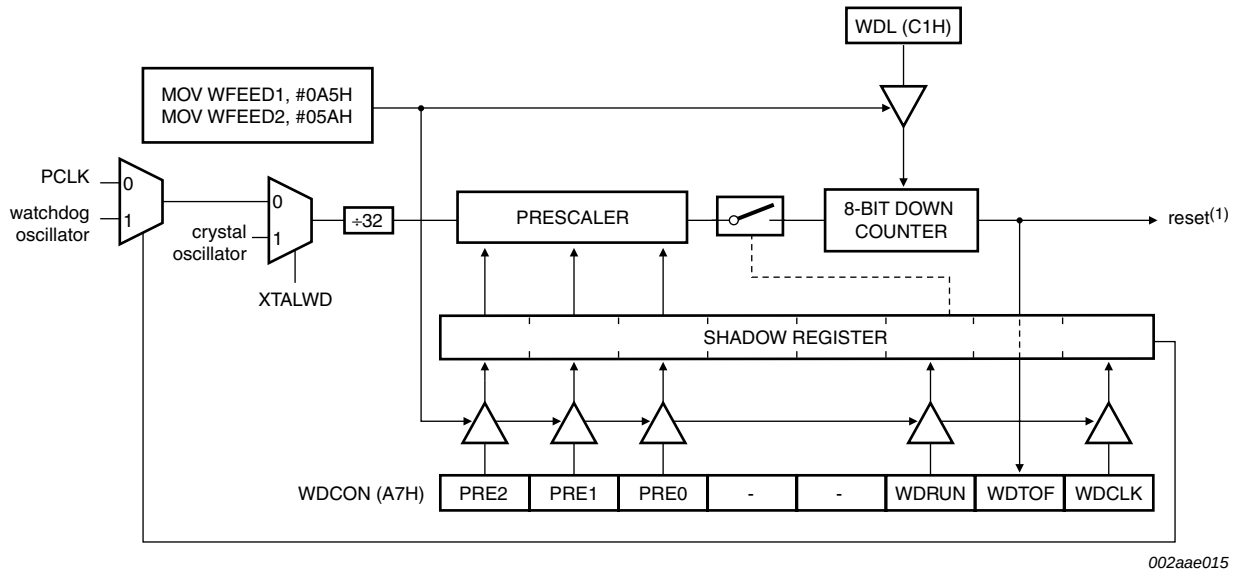


Fig 14. I²C-bus serial interface block diagram



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 20. Watchdog timer in Watchdog mode (WDTE = 1)

7.29 Additional features

7.29.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

7.29.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

7.29.3 Data EEPROM

The P89LPC9321 has 512 bytes of on-chip Data EEPROM. The Data EEPROM is SFR based, byte readable, byte writable, and erasable (via row fill and sector fill). The user can read, write and fill the memory via SFRs and one interrupt. This Data EEPROM provides 100,000 minimum erase/program cycles for each byte.

- Byte mode: In this mode, data can be read and written one byte at a time.
- Row fill: In this mode, the addressed row (64 bytes) is filled with a single value. The entire row can be erased by writing 00H.
- Sector fill: In this mode, all 512 bytes are filled with a single value. The entire sector can be erased by writing 00H.

7.30.8 ISP

ISP is performed without removing the microcontroller from the system. The ISP facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC9321 through the serial port. This firmware is provided by NXP and embedded within each P89LPC9321 device. The NXP ISP facility has made in-system programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

7.30.9 Power-on reset code execution

The P89LPC9321 contains two special flash elements: the Boot Vector and the Boot Status bit. Following reset, the P89LPC9321 examines the contents of the Boot Status bit. If the Boot Status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status bit is set to a value other than zero, the contents of the Boot Vector are used as the high byte of the execution address and the low byte is set to 00H.

Table 8 shows the factory default Boot Vector setting for these devices. A factory-provided boot loader is pre-programmed into the address space indicated and uses the indicated boot loader entry point to perform ISP functions. This code can be erased by the user.

Remark: Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector that contains this boot loader. Instead, the page erase function can be used to erase the first eight 64-byte pages located in this sector.

A custom boot loader can be written with the Boot Vector set to the custom boot loader, if desired.

Table 8. Default boot vector values and ISP entry points

Device	Default boot vector	Default boot loader entry point	Default boot loader code range	1 kB sector range
P89LPC9321	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH

7.30.10 Hardware activation of the boot loader

The boot loader can also be executed by forcing the device into ISP mode during a power-on sequence (see the P89LPC9321 *User manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the boot vector (1FH) is changed, it will no longer point to the factory pre-programmed ISP boot loader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

7.31 User configuration bytes

Some user-configurable features of the P89LPC9321 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1 and UCFG2. Please see the P89LPC9321 *User's Manual* for additional details.

7.32 User sector security bytes

There are eight User Sector Security Bytes on the P89LPC9321. Each byte corresponds to one sector. Please see the P89LPC9321 *User manual* for additional details.

7.33 PGA

Additional PGA module is integrated. The gain of PGA can be programmable to 2, 4, 8 and 16. Please refer to Table 10 “Static characteristics” for detailed specifications.

Register PGACON1 and PGACON1B are used to for PGA1 configuration. Register PGA1TRIM2X4X and PGA1TRIM8X16X provide trim value of PGA1 gain level. As power-on, default trim value for each gain setting is loaded into the PGA1 trim registers. For accurate measurements, offset calibration is required.

Please see the P89LPC9321 *User manual* for detail configuration, calibration, and usage information.

In Power-down mode or Total Power-down mode, the PGA1 does not function. If the PGAs, is enabled, it will consume power. Power can be reduced by disabling the PGA1.

9. Static characteristics

Table 10. Static characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	10	15	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	14	23	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	3.25	5	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	5	7	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 3.6 V; voltage comparators powered down	[2]	-	20	40	μA
$I_{DD(tpd)}$	total Power-down mode supply current	V_{DD} = 3.6 V	[3]	-	1	5	μA
$(dV/dt)_r$	rise rate	of V_{DD}		-	-	2	mV/μs
$(dV/dt)_f$	fall rate	of V_{DD}		-	-	50	mV/μs
V_{DDR}	data retention supply voltage			1.5	-	-	V
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only		−0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	port 1		-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA; V_{DD} = 2.4 V to 3.6 V all ports, all modes except high-Z	[4]	-	0.6	1.0	V
		I_{OL} = 3.2 mA; V_{DD} = 2.4 V to 3.6 V all ports, all modes except high-Z	[4]	-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = −20 μA; V_{DD} = 2.4 V to 3.6 V; all ports, quasi-bidirectional mode		V_{DD} − 0.3	V_{DD} − 0.2	-	V
		I_{OH} = −3.2 mA; V_{DD} = 2.4 V to 3.6 V; all ports, push-pull mode		V_{DD} − 0.7	V_{DD} − 0.4	-	V
		I_{OH} = −10 mA; V_{DD} = 2.4 V to 3.6 V; all ports, push-pull mode		-	3.2	-	V
V_{xtal}	crystal voltage	on XTAL1, XTAL2 pins; with respect to V_{SS}		−0.5	-	+4.0	V
V_n	voltage on any other pin	except XTAL1, XTAL2, V_{DD}; with respect to V_{SS}	[5]	−0.5	-	+5.5	V
C_{iss}	input capacitance		[6]	-	-	15	pF
I_{IL}	LOW-level input current	V_I = 0.4 V	[7]	-	-	−80	μA
I_{LI}	input leakage current	$V_I = V_{IL}$, V_{IH}, or $V_{th(HL)}$	[8]	-	-	±1	μA

Table 12. Dynamic characteristics (18 MHz) *…continued*
V_{DD} = 3.0 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$t_{SPILEAD}$	SPI enable lead time	see Figure 25, 26					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 25, 26					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 23, 24, 25, 26					
	slave		$^{3}/_{CCLK}$	-	167	-	ns
	master		$^{2}/_{CCLK}$	-	111	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 23, 24, 25, 26					
	slave		$^{3}/_{CCLK}$	-	167	-	ns
	master		$^{2}/_{CCLK}$	-	111	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 23, 24, 25, 26					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 23, 24, 25, 26					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 25, 26					
	slave		0	80	0	80	ns
t_{SPIDIS}	SPI disable time	see Figure 25, 26					
	slave		0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 23, 24, 25, 26					
	slave		-	160	-	160	ns
	master		-	111	-	111	ns
t_{SPIOH}	SPI output data hold time	see Figure 23, 24, 25, 26	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 23, 24, 25, 26					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 23, 24, 25, 26					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

11. Other characteristics

11.1 Comparator electrical characteristics

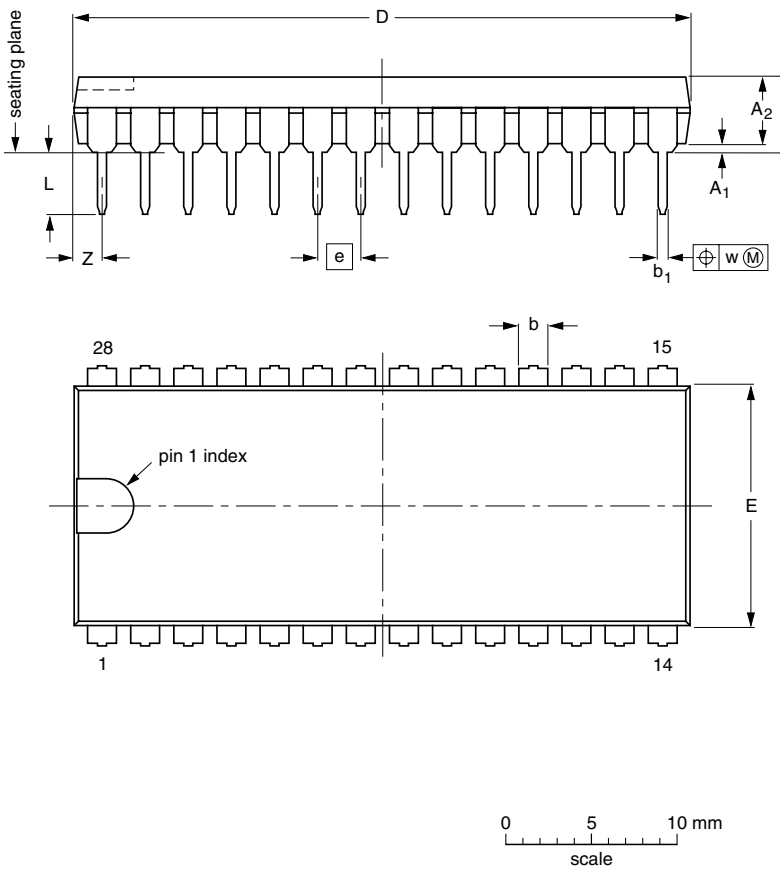
Table 14. Comparator electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IO}	input offset voltage			-	-	±20	mV
V_{IC}	common-mode input voltage			0	-	V_{DD} − 0.3	V
CMRR	common-mode rejection ratio		[1]	-	-	−50	dB
$t_{res(tot)}$	total response time			-	250	500	ns
$t_{(CE-OV)}$	chip enable to output valid time			-	-	10	μs
I_{LI}	input leakage current	0 V < V_I < V_{DD}		-	-	±1	μA

[1] This parameter is characterized, but not tested in production.

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4	1.7 1.3	0.53 0.38	0.32 0.23	36 35	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.2	0.02	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.1	0.6	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT117-1	051G05	MO-015	SC-510-28			~~99-12-27~~ 03-02-13

Fig 30. DIP28 package outline (SOT117-1)

13. Abbreviations

Table 16. Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
BOD	Brownout Detection
CPU	Central Processing Unit
CCU	Capture/Compare Unit
EPROM	Erasable Programmable Read-Only Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electro-Magnetic Interference
LSB	Least Significant Bit
MSB	Most Significant Bit
PGA	Programmable Gain Amplifier
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real-Time Clock
SCL	Serial Clock Line
SDA	Serial DAta Line
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

14. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC9321 v.2	20101116	Product data sheet	-	P89LPC9321 v.1
Modifications:	• Table 9: Updated table. • Table 14: Updated I_{LI} max value. • Section 7.4: Added low speed oscillator information. • Section 7.28: Added low speed oscillator information. • Changed data sheet status to Product.			
P89LPC9321 v.1	20081209	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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